Extreme optimization of 1200V SuperJunction IGBT, competing with SiC MOSFET

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***Abstract*—1200V SuperJunction IGBT (SJ-IGBT) are optimized independently for switching-off and -on, by using comprehensive TCAD simulations. We propose, for the first time, that the turn-off and turn-on losses can be significantly reduced by adopting wider pillar widths than previously expected, along with optimized pillar doping concentration. The optimized wider pillar SJ-IGBT exhibits extremely low switching losses that are competitive with SiC-MOSFETs and maintains good manufacturing reproducibility.**

Keywords—IGBT, SuperJunction, switching loss

I. Introduction

IGBTs have been continuously improved as medium-high voltage silicon power devices for over 40 years. SuperJunction IGBT (SJ-IGBT) is expected to be a candidate to achieve further loss reduction [1]. There have been several discussions about structural optimization for electrical properties [2-9]. However, the relationship between the structural parameters and switching behavior of SJ-IGBT has not yet been fully optimized [10].

Based on comprehensive TCAD simulations over a wide range of structural parameters, this paper optimizes 1200V SJ-IGBT structures, for the first time, independently for low switching-off and switching-on losses that can compete with SiC-MOSFETs. Based on the results, we propose a few optimized parameter sets of the pillar doping and width, considering the ease of fabrication.

II. SJ-IGBT Structure and Simulation Setup

For extensive simulations, we varied only the pitch of SJ pillars by 1um step and utilized the same multi-cell trench MOS structure. The doping concentration and width of the pillars are changed from $5.0x10^{14}$ to $2.0x10^{16}cm^{-3}$ and from 1 to 30um, respectively. The pillar depth was fixed and set to 90um. Conventional 1200V FS-IGBT and SiC trench MOSFET structures were used to compare electrical performance. The rated current density was set to $200A/cm^2$ for silicon devices and $400A/cm^2$ for SiC-MOSFET, respectively. Fig. 1 shows the simulated structures. The device structural parameters are summarized in Table 1.

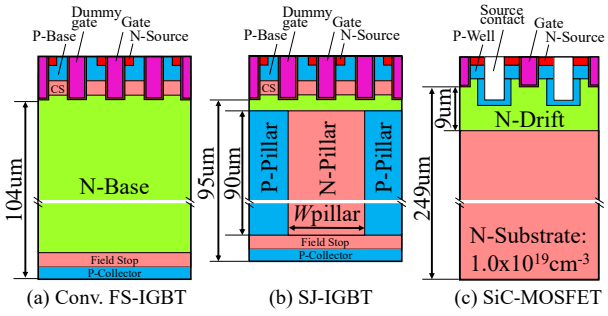

Fig. 1. Simulated structures. Doping concentration and width of the SJ pillars were varied.

Static and inductive load turn-off and turn-on characteristics were evaluated by TCAD Sentaurus simulations [12]. In order to improve simulation accuracy for considering the charge imbalance, 0.2nm of mesh size was used for the junction of P-pillar and N-pillar. For switching simulations, 30nH of stray inductance was set between high and low side. 1ohm of small gate resistance was applied to achieve fast turn-off. The Emitter electron current (MOSFET current) needs to be cut off before the fall-time. For turn-on simulations, typical silicon PiN diode and SiC-SBD were used as FWD.

Table 1. Device structural parameters.

	Conv. FS-IGBT	SJ-IGBT	SiC-MOSFET[11]
N-Base/N-Drift thickness	104um	90um	9um
Trench pitch	2.0um		3.0um
Mesa width	1.0um		-
Trench depth	6.0um		1.0um
Gate oxide thickness	0.1um		
P-Base/Well depth	2.4um		0.6-2.2um
CS depth	4.0um		-
N-Base/Drift doping conc.	$7.0x10^{13}cm^{-3}$		$5.0x10^{15}cm^{-3}$

III. Results and Discussion

A. Turn-off loss

Turn-off loss of SJ-IGBT strongly depends on the pillar doping concentration and width. The relationship is plotted in Fig. 2.

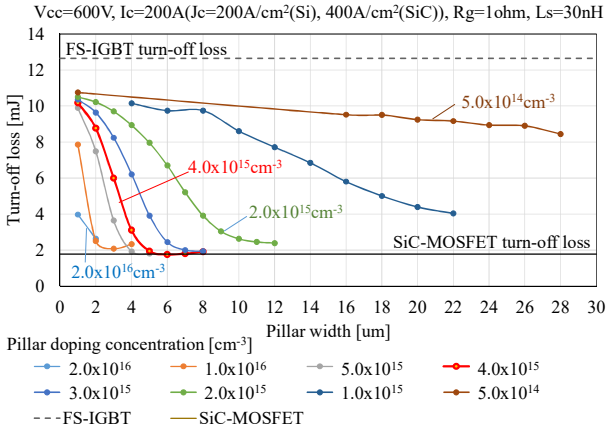

Fig. 2. Turn-off loss as a function of the pillar width.

From this figure, it is obvious that the turn-off loss of SJ-IGBTs significantly depends on the pillar width and achieves extremely low turn-off loss for the case of middle ($2.0x10^{15}cm^{-3}$) to high ($2.0x10^{16}cm^{-3}$) doping concentration of the pillar. For lower pillar concentration (less than $1.0x10^{15}cm^{-3}$), this tendency is weakened and the turn-off loss cannot be much improved. The maximum pillar width is determined by the breakdown voltage of the SJ-IGBT because the breakdown voltage reduces as the pillar width increases. It is shown that the optimum combination of the pillar doping and pillar width is $4.0x10^{15}cm^{-3}$ and 6um,

respectively. This achieves the minimized turn-off loss, 1.76mJ, which is even lower than the calculated value, 1.78mJ, of SiC-MOSFET under the same condition.

By observing the turn-off waveforms and carrier distribution transient phenomena, we found that there are significant differences in turn-off behavior, depending on the pillar width. Fig. 3 compares the waveforms of the SJ-IGBTs with two typical pillar widths and that of conventional FS-IGBT. The SJ-IGBT with narrow pillar shows smaller dV/dt, similar to conventional FS-IGBT. The dI/dt is also similarly slow in the beginning of the fall time, but then shows steep current fall. The SJ-IGBT with wide pillar has quite different waveforms of both voltage and current from them. It shows quite high dV/dt and high dI/dt, which is the same as SiC-MOSFET.

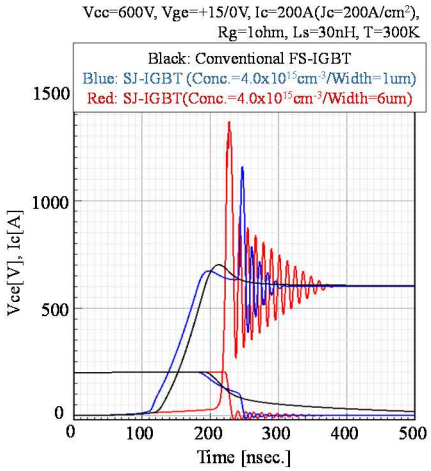

Fig. 3 Turn-off waveforms

These waveforms can be explained by observing the behavior of depletion region expansion. In the present paper, the depletion region is defined as the region where the majority carrier concentration is lower than the doping concentration. This means that unneutralized donors or acceptors are present in the defined depletion region. Fig. 4 shows carrier distribution transient phenomenon of narrow pillar SJ-IGBT. The white lines show the depletion region edge. Initially, top of the N-pillar is depleted by applied electric field. Then, the depletion layer expands vertically toward Field-stop layer. The vertical depletion follows the Vce voltage increase, resulting in the slow dV/dt. It takes about 100ns to complete depletion. This is similar behavior as conventional IGBTs.

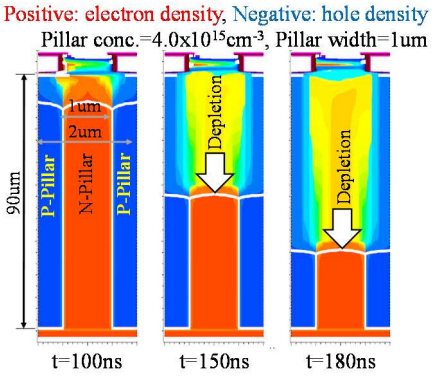

Fig. 4. Depletion region expansion during turn-off of a narrow pillar SJ-IGBT. An electric field is applied between the P-base and the SJ region. The depletion region expands vertically, just like in a conventional IGBT.

On the other hand, wide pillar SJ-IGBT has different internal behavior. Fig. 5 shows carrier distribution transient phenomenon of wide pillar SJ-IGBT. Initially, an electric field is applied to the junction of P-pillar and N-pillar, and the depletion layer develops laterally. Then, the remaining carriers, located in the center of the pillars, are extracted toward vertical direction. The vertical depletion is completed in quite short time period because the width of the un-depleted pillars are very narrow.

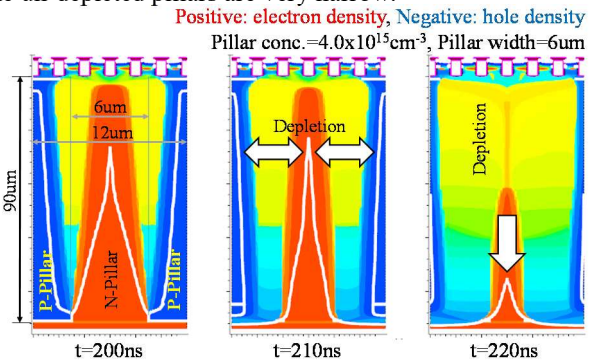

Fig. 5. Depletion region expansion of wide pillar SJ-IGBT. Electric field is applied between P-pillar and N-pillar. The depletion region expands laterally and excess carriers are swept out instantaneously.

B. Turn-on loss

The turn-on loss of SJ-IGBT also strongly depends on the width and the doping concentration of the pillar, as is similar to the case of turn-off loss. The relationship is plotted in Fig. 6.

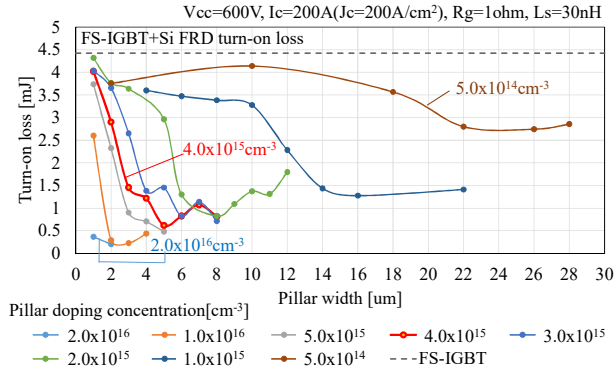

Fig. 6. Turn-on loss as a function of the pillar width.

It is shown that SJ-IGBTs with wide pillar achieve extremely low turn-on loss for the same middle to high doping concentration as is the case of turn-off loss. It is shown that the optimum combination of the pillar doping and pillar width of $2.0x10^{16}cm^{-3}$ and 2um achieves the minimum turn-on loss, 0.21mJ. The combination of the pillar doping and pillar width of $4.0x10^{15}cm^{-3}$ and 6um, which is optimum for switching-off, also achieves the turn-on loss of 0.82mJ.

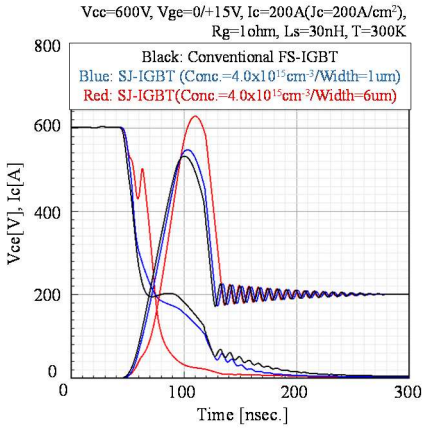

Fig. 7 Turn-on waveforms coupling with Si PiN diode.

The loss mainly depends on the voltage drop during the turn-on process. Fig. 7 compares the waveforms of the SJ-IGBTs with varied pillar width and conventional FS-IGBT. The narrow pillar SJ-IGBT shows similar waveforms to conventional FS-IGBT. On the other hand, the wide pillar SJ-IGBT shows steep voltage fall.

The difference of the voltage waveforms can be explained by carrier accumulation process. Fig. 8 shows carrier distributions of the narrow pillar SJ-IGBT during turn-on. The white line show the depletion region edge. During this period, the narrow pillars are almost completely depleted. It prevents from increasing carrier density toward the value of steady state, resulting in higher on-state voltage drop.

Fig. 9 shows carrier distribution transient phenomenon of the wide pillar SJ-IGBT. The carrier density becomes higher in the center of the pillar immediately after the turn-on. This is because the central portion of the pillar is not depleted any more when the applied voltage decreases. It leads steep decrease of the pillar resistance and resultant voltage fall.

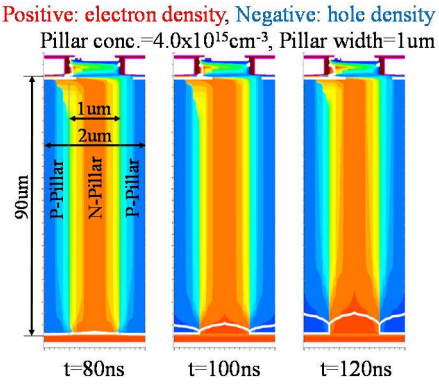

Fig. 8. Carrier accumulation process of narrow pillar SJ-IGBT during turn-on.

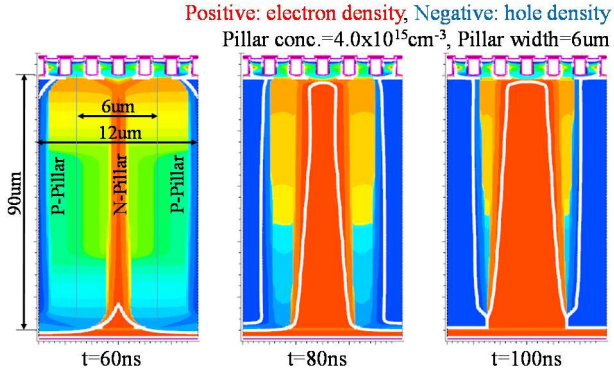

Fig. 9. Carrier accumulation process of wide pillar SJ-IGBT during turn-on.

C. *On-state voltage*

In the previous research, it was discussed that planar gate SJ-IGBT sometimes show unipolar like on-state behavior[2]. In contrast, in this research, the excess carrier density of all simulated SJ-IGBTs becomes much higher than the doping level and it forms conductivity modulation. It is because the trench gates supply enough electron current. Fig. 10 shows Ic-Vce characteristics. In the low current density region, highly doped SJ-IGBT shows lower voltage drop because of higher carrier density. However, the voltage drop becomes larger in the high current density region. It is because the mobility in the pillars is degraded by high doping concentration.

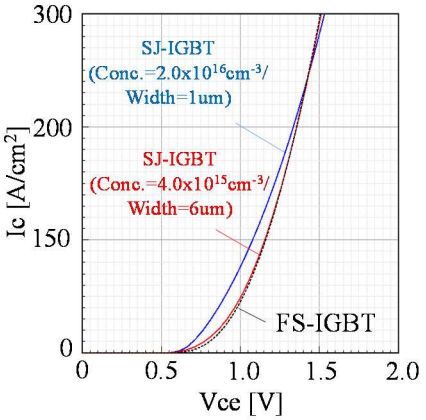

Fig. 10. Ic-Vce characteristics.

D. *Overll optimization of the structure*

In general, low doped pillar has an advantage for charge imbalance immunity. Fig. 11 shows the charge imbalance immunity. When the pillar doping is $4.0x10^{15}cm^{-3}$, and the width is 6um, less than 3% of charge imbalance is required to achieve the breakdown voltage over 1300V. When the pillar doping is reduced to $3.0x10^{15}cm^{-3}$ and the width is expanded to 7um, it can keep the breakdown voltage of 1300V even for 5% of charge imbalance.

A slightly higher pillar doping is better when we consider minimizing total power loss, including turn-on loss. However, the pillar doping and width described above are probably better to reduce manufacturing difficulties.

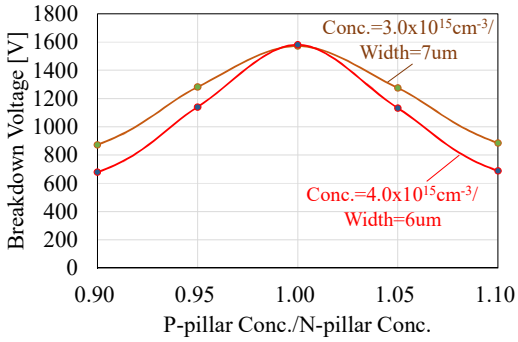

Fig. 11. Charge imbalance immunity.

Fig. 12 shows trade-off curves of on-state voltage drop and turn-off loss for 27degC(300K) and 150degC(423K). SJ-IGBT shows drastically improved trade-off relation compared with conventional FS-IGBT, and the switching speed is really competing with SiC-MOSFET. In room temperature, SJ-IGBT reduces 80% of turn-off loss from conventional FS-IGBT at the same on-state voltage drop. The turn-off loss is almost the same as that of typical SiC-MOSFET although the on-state voltage drop is 1.35V, which is higher than SiC-MOSFET by 0.2V.

In high temperature, reduced pillar doping ($3.0x10^{15}cm^{-3}$) SJ-IGBT shows slightly higher turn-off loss than optimum design ($4.0x10^{15}cm^{-3}$). However, it is still much better than conventional FS-IGBT. Thanks to lightly doped pillars, the on-state voltage drop is only 0.26V higher than that of room temperature. In contrast, SiC-MOSFET has 1.8 times higher on-resistance than room temperature.

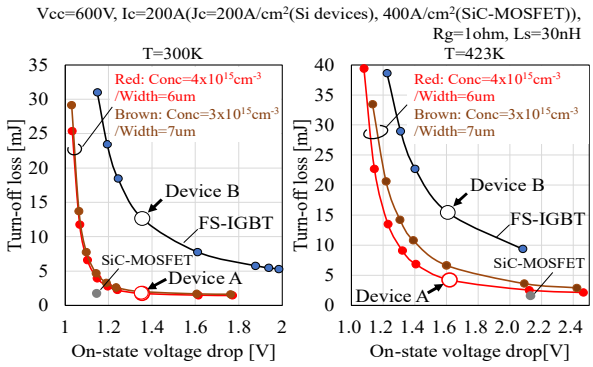

Fig. 12. Trade-off curves between on-state voltage drop and turn-off loss. The white circles show the locations of the devices A and B.

Fig. 13 shows turn-off loss and turn-off surge voltage as a function of gate resistance. It indicates that SJ-IGBT realizes moderately lower surge voltage and even lower turn-off loss compared with SiC-MOSFET if the gate resistance is less than 8 ohm. The waveforms with 10 ohm of gate resistance are compared in Fig. 14.

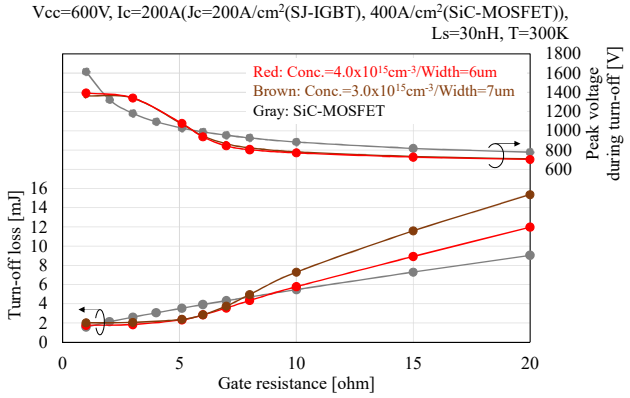

Fig. 13. Turn-off loss and surge voltage as functions of gate resistance. SJ-IGBT realizes lower surge voltage and lower turn-off loss compared with SiC-MOSFET if the gate resistance is less than 8 ohm.

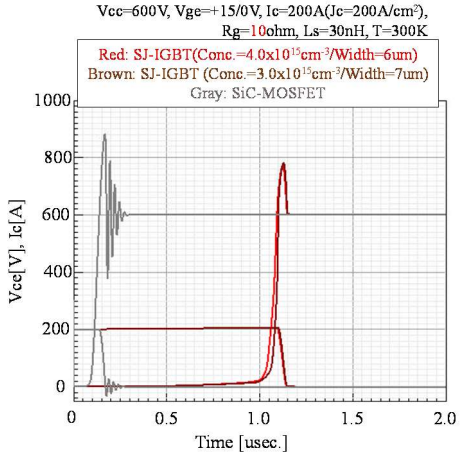

Fig. 14. Turn-off waveforms of SJ-IGBT and SiC-MOSFET with Rg=10ohm. SJ-IGBT realizes lower surge voltage and oscillation-free waveforms, compared with SiC-MOSFET.

The electrical characteristics of the optimized SJ-IGBT are summarized in Table II. The on-state voltage of SJ-IGBT is lower than SiC-MOSFET in 423K. The turn-off loss of SJ-IGBT becomes slightly higher in 423K, however, still greatly lower than FS-IGBT. The turn-on loss of SJ-IGBT is also sufficiently lower than FS-IGBT and is close to SiC-MOSFET. Further loss reduction can be achieved by coupling with SiC-SBD.

Table II. Comparison of the characteristics of optimized SJ-IGBT (Conc.=4.0x10^{15}cm^{-3}, width=6um) and SiC-MOSFET when Rg is 1ohm.

	300K			423K		
	FS-IGBT (Device B)	SJ-IGBT (Device A)	SiC-MOSFET	FS-IGBT (Device B)	SJ-IGBT (Device A)	SiC-MOSFET
BV[V]	1420	1580	1630	1770	1900	1730
On-state voltage [V]	1.36	1.36	1.15	1.61	1.62	2.13
Turn-off loss [mJ]	12.7	1.76	1.78	15.5	4.25	1.61
Turn-on loss with Silicon diode [mJ]	4.42	0.82	-	4.86	0.98	-
Turn-on loss with SiC-SBD [mJ]	1.88	0.78	0.26	2.15	0.78	0.28

IV. Conclusion

We found optimum design of SJ-IGBT by comprehensive TCAD simulations. SJ-IGBTs with proposed set of pillar impurity doping and width realizes extremely low switching loss, competing with SiC-MOSFET, and good manufacturing reproducibility.

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