A 15V operated Shallow Trench IGBT(ST-IGBT) fabricated by low temperature process and optimized for 12inch wafers

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***Abstract*—In this paper, we propose shallow trench IGBT (ST-IGBT) and its fabrication process. It is designed for 15V of gate operation, as is the same as conventional IGBTs. The cell is consist of shallow trench gate MOS structure and shallow doping layers, formed by ion implantation and RTA (Rapid Thermal Anneal). The edge termination structure is composed by many shallow FLRs. The optimized cell design reduces Vce(sat) by 0.2V, compared with conventional IGBTs.**

Keywords—IGBT, shallow trench, CMOS compatible process, 12inch wafer, edge termination.

I. INTRODUCTION

IGBTs are still widely used in the middle to high power semiconductor field. Recently, new generation vehicles such as HEV (Hybrid Electric Vehicle) and BEV (Battery Electric Vehicle) become popular. Many IGBT chips are installed in their traction inverters. Therefore, the demand of the chips increases and efficient mass production methodologies are strongly expected.

In order to meet the requirements, the "Scaled IGBT" was proposed and experimentally fabricated [1-5]. These devices were not compatible with conventional gate drive systems because of 5V gate drive. Heavy thermal processes were still used in the fabrication [5].

In this paper, we propose shallow trench IGBT (ST-IGBT), and its fabrication process. We demonstrate its superior electrical characteristics, compared with conventional IGBTs. In contrast to the scaled IGBT, our proposed ST-IGBT adopts the same 15V of gate voltage as conventional IGBTs. Its doping layers are produced only by ion implantation and RTA. This low thermal budget process is expected to improve the carrier lifetime, device characteristic variations [5] and manufacturability, and especially useful for 12 inch wafers because of CMOS-like shallow structure.

II. ST-IGBT

A. ST-IGBT structure and TCAD simulations

The proposed device structures are designed for 1200V class. The wafer thickness and the N-base doping concentration were set to 110um and 7.0e13cm^{-3}, respectively. The proposed cell structure is illustrated in Fig. 1. The structural parameters are summarized in Table 1. In order to improve the manufacturability and process uniformity, the trench depth was set to 2.0um and all diffusion layers were set to 2.5um or less. Approach to better Vce(sat)-Eoff trade off relationship with shallow trench, the narrow trench pitch of 0.6um, the thin wafer thickness of 110 um and carrier stored (CS) layer were utilized [6]. Especially, 0.1um of narrow segmented N+ source was introduced in order to prevent saturation current divergence (without CIBL) during short-circuit operation [7]. A part of the electrodes inside the trenches were connected to the emitter in order to reduce saturation current and gate capacitance.

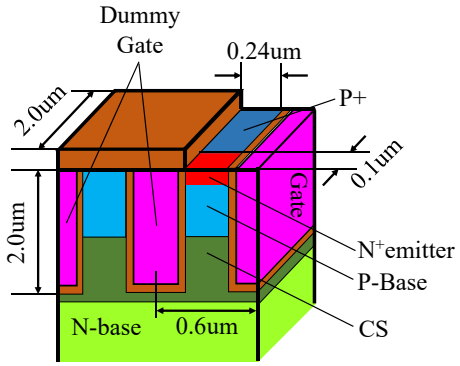

Fig. 1. Proposed ST-IGBT cell structure. The trench depth was set to 2.0um and all diffusion layers were set to 2.5um or less.

Table 1. Device structural parameters.

	ST-IGBT	Conventional IGBT with CS layer
Silicon thickness	110	110
Trench pitch	0.6	2.0
Mesa width	0.24	1.0
Trench depth	2.0	6.0
Gate oxide thickness	0.1	0.1
P-base depth	0.8	2.4
CS depth	2.5	7.0
N+ emitter width for depth direction	0.1	0.6
FLR depth	2.5	-

3D TCAD process-device simulations were performed to analyze ST-IGBT electrical performances. The fabrication process flow and conditions are shown in Fig. 2. Following to the FLR formation, 2.0um depth of trench gate structure was formed before CS and P-base doping introductions. The order of the process step prevents the segregation effect during gate oxidation and is expected to reduce the process variability. Then, the 2.5um depth of CS and 0.8um of P-base layers were formed by 1MeV of Phosphorus and 240keV of Boron implants, respectively. After that N+ source and P+ layers are formed with patterning.

In the process simulation, Monte Carlo ion implantation model were used to accurately reproduce these doping profiles because the complex trench structure is formed before the implant processes. A calibrated parameter set for CMOS processes [8] was used to accurately calculate dopant

activations and diffusions. RTA thermal sequence was optimized to eliminate dopant clusters completely, as shown in Fig. 2.

Wafer 60ohm-cm
- FLR Boron implant 1.0e13cm^{-2}/1MeV/7deg
- RTA
- Trench etching
- Gate oxidation 100nm
- Polysilicon depo
- Screen oxide formation 100nm
- CS implant Phosphorus 7.0e12cm^{-2}/1MeV/7deg
- RTA
- P-Base implant Boron1.5e13cm^{-2}/240keV/7deg
- RTA
- Strip screen oxide
- Source implant Arsenic 1.0e15cm^{-2}/30keV/7deg
- P+ implant BF2 1.0e15cm^{-2}/30keV/7deg
- RTA
- BPSG deposition and anneal 900degC/60min
- Contact hole formation
- Metallization
- Backside processing

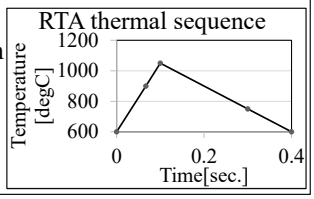

Fig. 2. ST-IGBT process flow. All doping layers are produced only by ion implantation and RTA. The optimized thermal sequence of RTA is shown together.

B. ST-IGBT simulation results and discussion

Fig. 3 shows the process simulated ST-IGBT structure. The process simulator predicts that implanted ions are almost completely activated as donors or acceptors by RTA as shown in Fig. 4.

Fig. 5 shows Ic-Vc characteristics. Vce(sat) of ST-IGBT is 1.22V and is 0.2V lower than that of conventional IGBT with CS layer. Fig. 6 shows on state carrier distribution profiles. The carrier profiles in the N-Base of ST-IGBT are almost the same as those of conventional IGBT. It indicates that the ST-IGBT realizes the same electron injection efficiency from the emitter side as that of conventional IGBT, in spite of shallow trench cell structure. It is shown in Fig. 7 that the voltage drop inside the trench of ST-IGBT is lower than that of conventional IGBT by 0.2V. The improvement is largely attributed to the effect of shallow trench. Fig. 8 shows electron quasi-fermi potential along the MOS channels. It reveals that the Vce(sat) improvement of 0.2V comes mostly from the effect of the short channel. ST-IGBT has only 0.1V or less of voltage drop inside the channel, although that of conventional IGBT is 0.28V. The improvement is 0.18V.

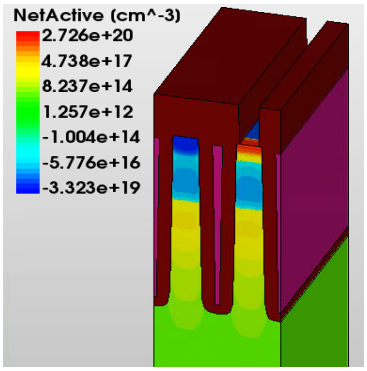

Fig. 3. Process simulated ST-IGBT cell structure.

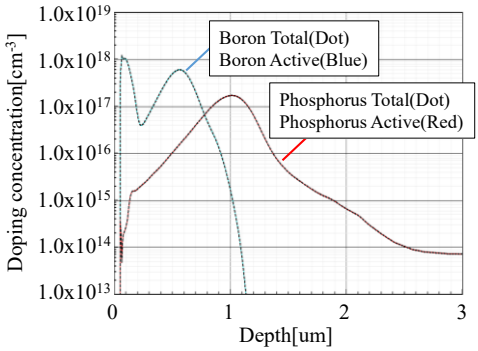

Fig. 4. Total and active concentration profiles of P-Base and CS layers. Implanted ions in the P-Base and CS are completely activated by RTA.

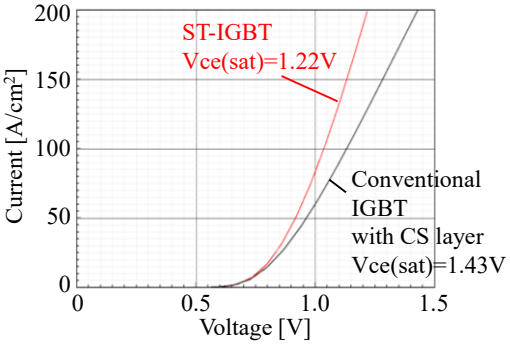

Fig. 5. Ic-Vc characteristics of ST-IGBT and conventional IGBT with CS layer. ST-IGBT reduces 0.2V of Vce(sat) in comparison with conventional IGBT.

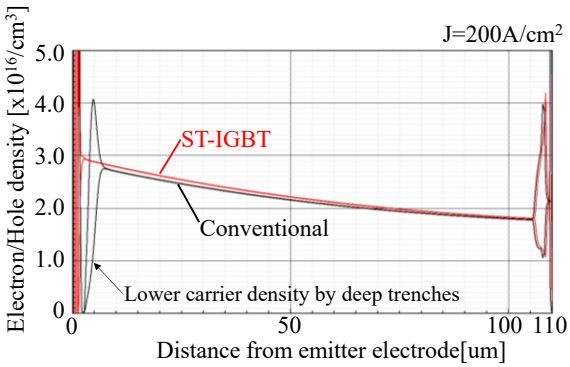

Fig. 6. On-state carrier distribution profiles. The carrier profiles in the N-Base of ST-IGBT are the same as those of conventional IGBT with CS layer.

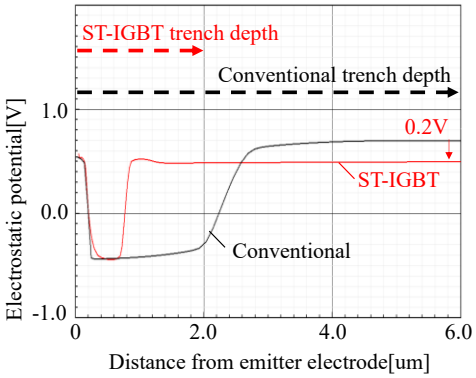

Fig. 7 Comparison of potential distributions in the mesa region inside the trenches. The voltage drop inside the trench of ST-IGBT is lower than that of conv. IGBT by 0.2V.

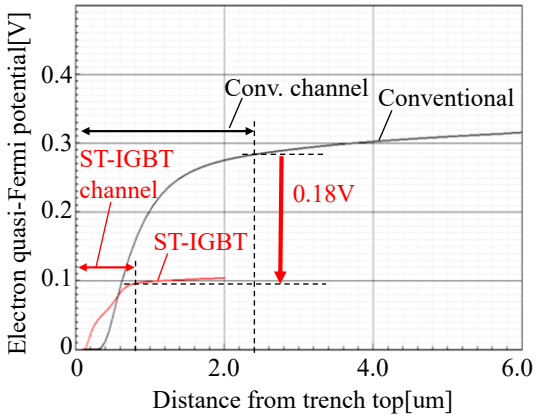

Fig. 8. Electron quasi-Fermi potential along the MOS channels. ST-IGBT has only 0.1V or less of voltage drop inside the channel, although that of conventional IGBT is 0.28V. The improvement is 0.18V.

Fig. 9 compares C-Vce characteristics between ST-IGBT and conventional CSTBT. ST-IGBT has lower inflection points of Coes and Cres. This is because the mesa of ST-IGBT is narrower than conventional CSTBT. The gate electrodes act as field plates and force to deplete mesa region in lower Vce.

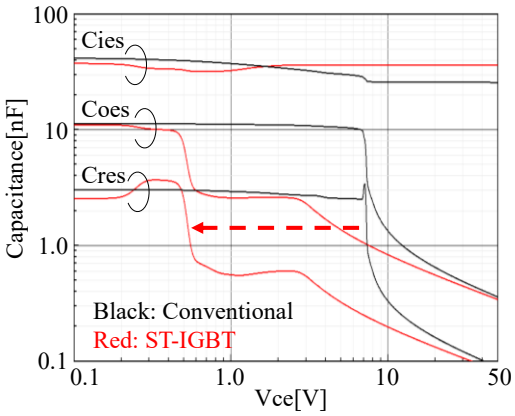

Fig. 9. C-Vce characteristics. The inflection point of ST-IGBT is lower than conventional IGBT because of narrow mesa.

Fig. 10 and Fig. 11 shows turn-off and turn-on waveforms, respectively. In the turn-off, ST-IGBT has shorter delay time because of the lower inflection point of Cres. Nevertheless, almost the equal di/dt and dv/dt are obtained because of the same N-Base carrier distribution. Fig. 12 compares the trade-off relation of Vce(sat)-Eoff between ST-IGBT and conventional IGBT. ST-IGBT reduces 0.2V of Vce(sat). It is shown in Fig. 13 that the saturation current of ST-IGBT was set at less than 900A/cm^2 during the short-circuit operation. This is because when the current density of the present IGBTs exceeds 1000A/cm^2, the device operates in the MOSFET-mode, and current filaments may appear and they lead device destruction [9].

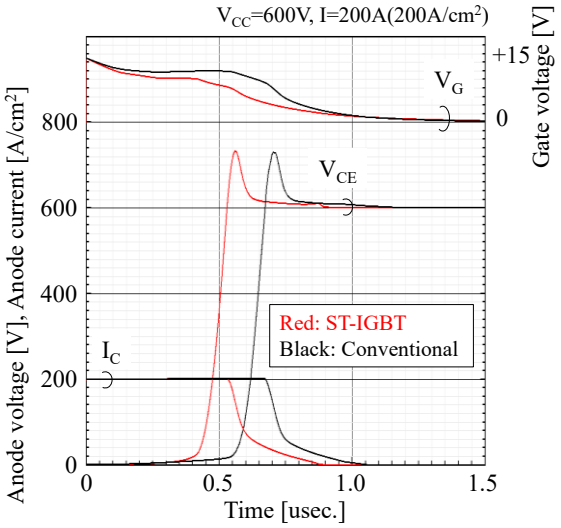

Fig. 10. Turn-off waveforms. The delay time of ST-IGBT is shorter than conventional IGBT because of smaller reverse transfer capacitance (Cres) in the low voltage region.

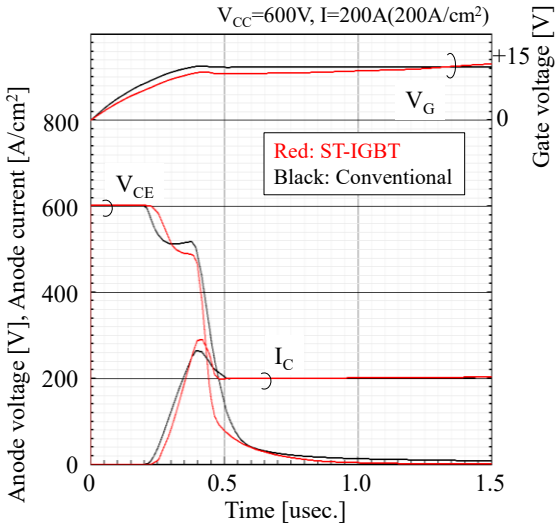

Fig. 11. Turn-on waveforms.

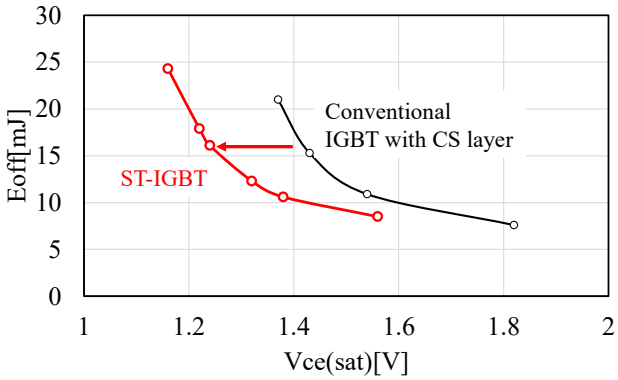

Fig. 12. Vce(sat)-Eoff trade-off. ST-IGBT reduces 0.2V of Vce(sat).

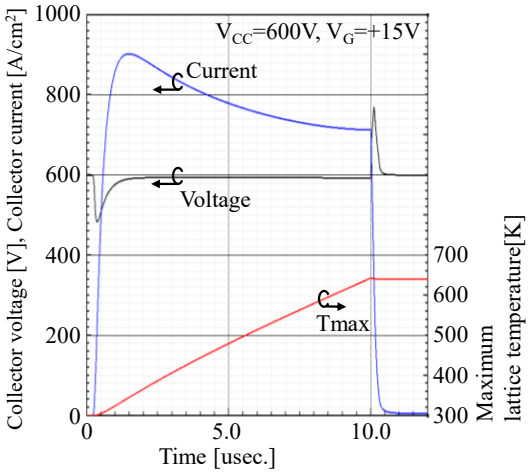

Fig. 13. Short-circuit waveforms of ST-IGBT. The saturation current was set at less than 900A/cm^2 to prevent current filamentation.

III. Edge Termination

The proposed edge termination structure is illustrated in Fig. 14. The structure consists of many buried P layers. The P layers are formed at the location under the trench bottom by 1MeV of Boron implant. Peak doping concentration of the P layers was set to 2.0x10^{17}cm^{-3}.

Bayesian Optimization was performed to find the design which maximizes the breakdown voltage and minimizes the electric field at Silicon-Oxide interface as well as termination length. It is shown in Fig. 15 that the optimum termination length was found as 370um, the structure achieves 1623V of breakdown voltage, and its maximum electric field is 0.12MV/cm. The number of the FLRs is 58. Fig. 16 shows breakdown waveforms of cell and edge termination structures. Sufficiently high breakdown voltage is achieved by optimized FLR pattern. Fig. 16 shows electric field distribution along Silicon-Oxide interface.

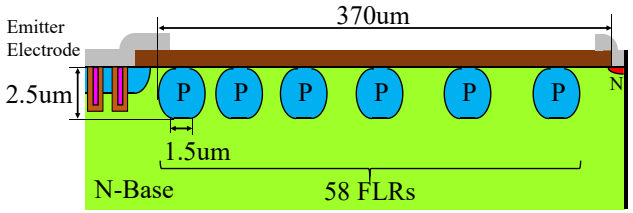

Fig. 14. Proposed edge termination structure.

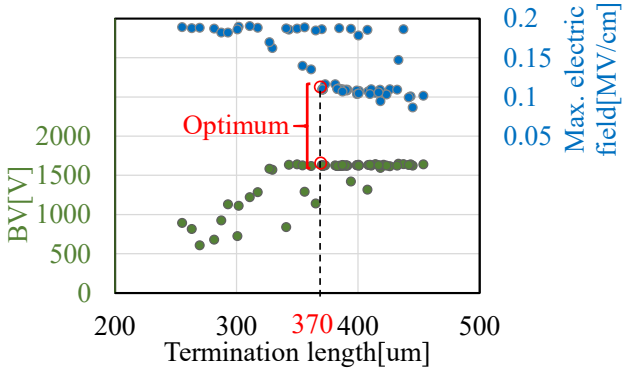

Fig. 15. Scatter plot of the termination length vs. breakdown voltage and peak electric field at Silicon-Oxide interface during optimization. Optimum design was found efficiently.

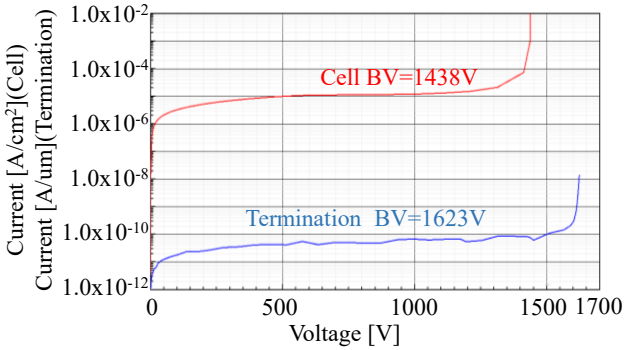

Fig. 15. Breakdown waveforms. Sufficiently high breakdown voltage is achieved by fine cell pitch and optimized FLR pattern.

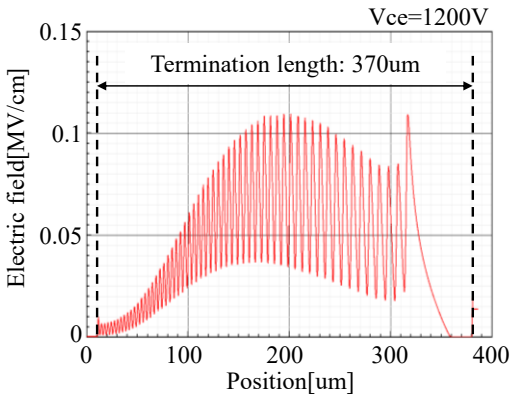

Fig. 16. Electric field distribution along Silicon-Oxide interface. The electric field is suppressed 0.12MV/cm or less.

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