Design Optimization of 500V Lateral SOI High Speed Diodes

A. Nakagawa, H. Funaki, Y. Yamaguchi and K. Hirayama
Advanced Semiconductor Devices Research Laboratories, Toshiba Corporation
1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 210, Japan
Phone: +81-44-549-2139 Fax: +81-44-520-1501
E-mail: akio.nakagawa@toshiba.co.jp

Abstract

First recovery SOI diodes have been developed for 500V 1A 1 chip inverter IC application, adopting reduced emitter efficiency. Since lifetime control process is not adopted the diode fabrication process is completely compatible with those of conventional LSIs. It was found that the ruggedness depends on the anode structure. The largest current controllability was achieved for the diodes, where the anode emitter consists of merged p-schottky and p+ ohmic contact and ,for the cathode emitter, p+ diffusions are formed in the n-type cathode layer.

The developed 1A rated diode controls 4 ampere current and achieves 300nsec reverse recovery time under the condition of 13A/μs di/dt and 300V applied voltage.

1. Introduction

Combination of SOI structure and trench isolation have been paid great attention because it realizes high voltage power ICs exceeding 500V in a reasonable cost. One of the good applications is one chip inverter ICs for DC brushless motors. Key devices for 500V inverter ICs are high voltage lateral IGBTs and first recovery diodes (FRD). Many papers have been published on the development of LIGBTs and its improvement. Difficulties in the development of lateral devices is that high operating current density, flowing laterally in the thin SOI layers, is required to reduce chip size and resultant chip cost. Typical operating current density in the SOI layers is 5 or 10 times as high as that of vertical devices. Recently, we reported the successful development of rugged 500V LIGBTs[1].

High voltage lateral first recovery diodes (FRDs) are another important devices to reduce total power loss in 1 chip inverter ICs. The device area of the FRDs is required to be sufficiently smaller than that of lateral IGBTs fabricated on the same chip. The maximum controllable current is one of the main factors which determine the required device size of FRDs.

Several high speed diode structures have already been proposed [2,3] to improve reverse recovery characteristics by reducing emitter injection efficiency. High speed and robustness are the main concern in the development of SOI diodes. However, no papers have discussed the ruggedness of the injection efficiency controlled lateral SOI diodes. The present paper compares, for the first time, the maximum controllable current, or SOA of three different diode structures with low efficiency emitters.

2. SOI diode (FRD) design and fabrication

High speed switching can be realized either by reducing carrier lifetime or by reducing emitter injection efficiency. Lifetime control process greatly affects the electrical characteristics of low voltage BiCMOS logic and analog devices. Thus, emitter injection efficiency controlled diodes are desirable, if they achieve sufficiently good electrical characteristics.

SOI diode switching characteristics are deeply related to SOI layer thickness as well as

drift layer length. A high speed diode is automatically realized by simply using relatively thin SOI layer. This is because the total depletion layer volume becomes smaller and the amount of stored charges reduce, as the SOI layer becomes thinner. Figure 1 shows the reverse recovery characteristics of three SOI diodes, fabricated in three different SOI layers with thickness of 10μm, 5μm and 2μm. The drift layer length is the same as 30μm for the three devices. The observed breakdown voltages were 250 to 280V, depending on the SOI layer thickness. It is seen that the switching speed is greatly improved by reducing SOI layer thickness. Thus, thinnest possible SOI layers should be adopted for power ICs.

Figure 2 shows cross sections of three typical injection efficiency controlled diode, examined in this paper. Figure 2(a) shows an anode emitter structure, where additional n^+ diffusion layers were formed in a p-type-diffusion layer together with p^+ ohmic contact diffusions. Diodes with this kind of anode emitter are referred as n^+/p^+ diodes in the present paper. In the structure of Fig.2(b), schottky contacts are introduced with p^+ ohmic contact diffusions. This kind of diodes are referred as p^-/p^+ diodes. Figure 2(c) shows another anode structure, where shallow p-diffusion layers were adopted to reduce injection efficiency. Combination of low dose shallow p^- diffusions and shallow p^+ diffusions were adopted for a low efficiency anode emitter. For the shallow emitter diodes, the p^+-diffusion area ratio over the total p-emitter area was varied and its influence on the maximum controllable current was examined. This kind of diodes are referred as shallow p/p^+ diodes. For the cathode structure, p^+ diffusion layers were formed in an n-type diffsion layer to reduce emitter injection efficiency. The same cathode structure was adopted for all the examined diodes.

All the diodes in the present paper were fabricated on a 15μm thick n-layer over 3μm thick buried oxide, and the obtained breakdown voltage was 520V. The dimensions of the diodes are 1mm in length 0.25mm in width. The anode cathode distance (n- drift layer length) is 50μm.

3. Evaluation for robust 500V SOI diodes

In this section, injection efficiency controlled diode designs are examined in the view-point of maximum controllable current.

Maximum controllable current were compared among the fabricated diodes which have almost the same forward voltages and reverse recovery characteristics by adjusting the emitter efficiency of the three different emitter structures.

Figure 3 shows the measured typical current-voltage curves for the p^-/p^+ diode at 25°C and 200°C. Figure 4 shows the measured typical reverse recovery waveforms at 25°C and 200°C. The temperature dependence of reverse recovery characteristics is very small since the injection efficiency does not significantly depend on temperature.

Reverse recovery measurement was carried out at 150°C, using the circuit shown in Fig. 5, which simulates actual inverter circuits. In the measurements, the MOSFET is turned-on to store energy in the inductor. Then, the MOSFET is turned-off , and the stored energy discharges through the diode under test. The diode is then turned-off by switching-on, again, the MOSFET. The magnitude of the diode current is adjusted by the MOSFET on-state duration.

The typical reverse recovery waveforms of p^-/p^+ diodes are shown in Fig. 6. The reverse recovery current had two peaks when a large reverse bias was applied. The first peak appears when the diode is initially reverse biased. The second peak is caused by a rapid dV/dt recovery

and is often accompanied by impact ionization.

It was found that n^+/p^+ diode easily destroyed in the reverse recovery transient at high temperature of 150°C because of a parasitic npn transistor action. The best optimization was found in p^-/p^+ diodes. The 1 ampere rated p^-/p^+ diodes have a capability of 4 ampere current turn-off, as seen in Fig.7, where the applied dI/dt and dV/dt was 13A/μs and 3kV/μs.

Figure 8 shows the maximum controllable current of shallow p/p^+ diodes as a function of p^+ contact diffusion ratio over total p-emitter area. The measured maximum controllable current of the n^+/p^+ diode and the p^-/p^+ diodes are shown together in the figure. Shallow p/p^+ diodes exhibited the same ruggedness, if the dose of shallow p layer was optimized, and p^+ contact diffusion was eliminated.

Figure 9 compares the measured trade-off curves between reverse recovery time, t_{rr} and forward voltage for p^-/p^+ diodes and n^+/p^+ diodes. Although the n^+/p^+ diodes have poor current capability, their trade-off curve was slightly better than that of p^-/p^+ diodes.

3-phase inverter ICs were fabricated using six 1A rated lateral IGBTs and p^-/p^+ diodes. We successfully demonstrated the operation of DC motor control at 200°C ambient temperature.

References:

[1] H.Funaki, T. Matsudai, A. Nakagawa, N. Yasuhara and Y. Yamaguchi, Proc. of 9th ISPSD, 1997, p.33

[2] A.Nakagawa, Proc. of 3rd ISPSD, 1991, p.16

[3] R. Sunkavalli and B.J. Baliga, Proc. of 7th ISPSD, 1995, p.385.

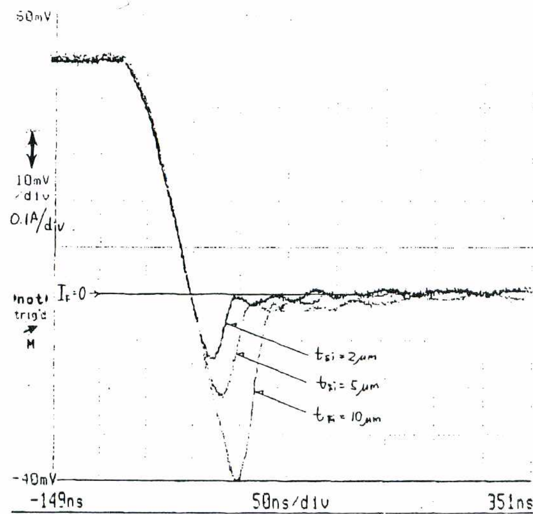

Fig.1 Reverse recovery waveforms for diodes with three different SOI layer thicknesses of 2μm, 5μm and 10μm.

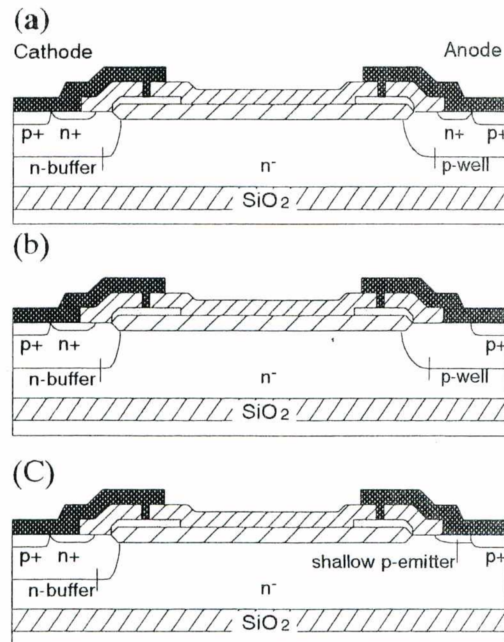

Fig.2 Cross sectional views of (a) n^+ / p^+, (b) p^- / p^+ and (c) shallow p / p^+ anode diodes on SOI.

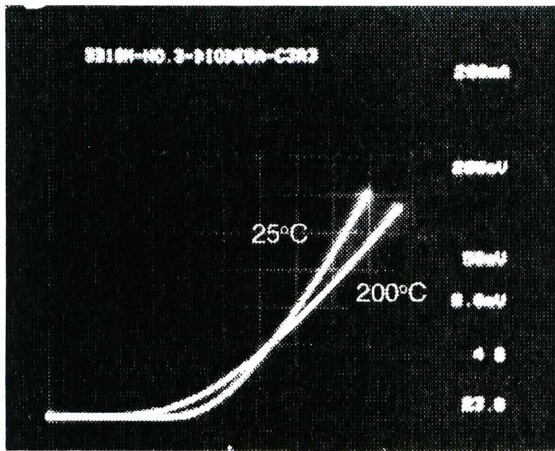

Fig.3 Experimentally obtained current-voltage curves for the p- / p+ diode at 25°C and 200°C.

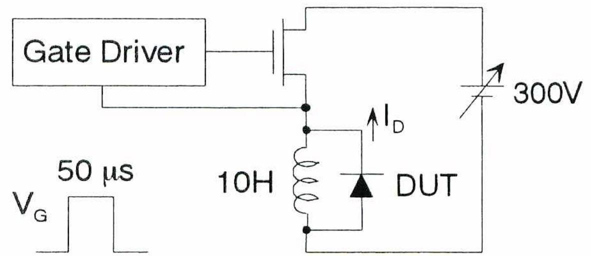

Fig.5Circuit configuration for the measurement of maximum controllable current in reverse recovery transient.

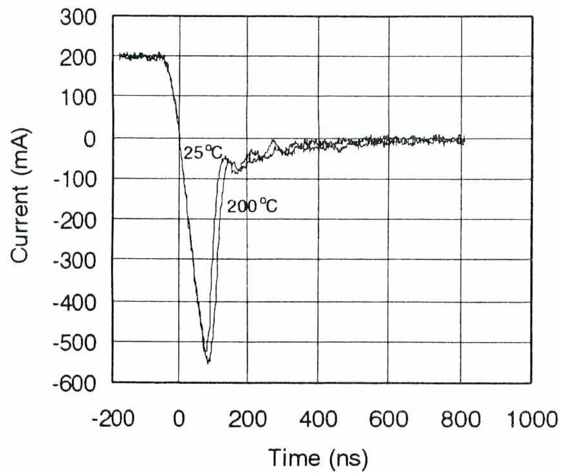

Fig.4 Measured reverse recovery waveforms for the p- / p+ diodes at 25°C and 200°C. Applied reverse bias was 40V for the measurements.

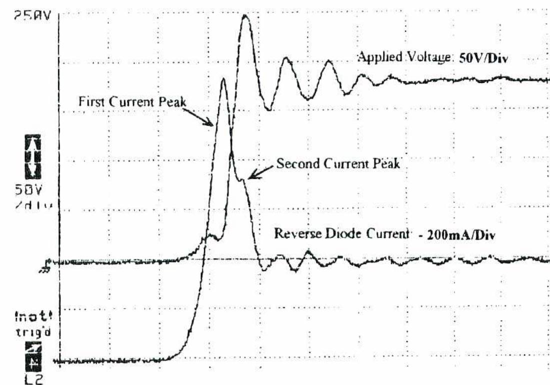

Fig.6 Typical Diode recovery waveform. In diode current waveform, downward shows positive current.

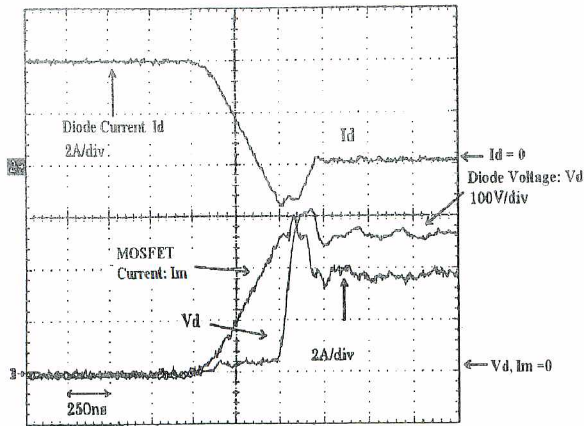

Fig.7 4 ampere turn-off waveforms of a p-/p+ diode in the circuit shown in Fig.5. Applied voltage was 300V.

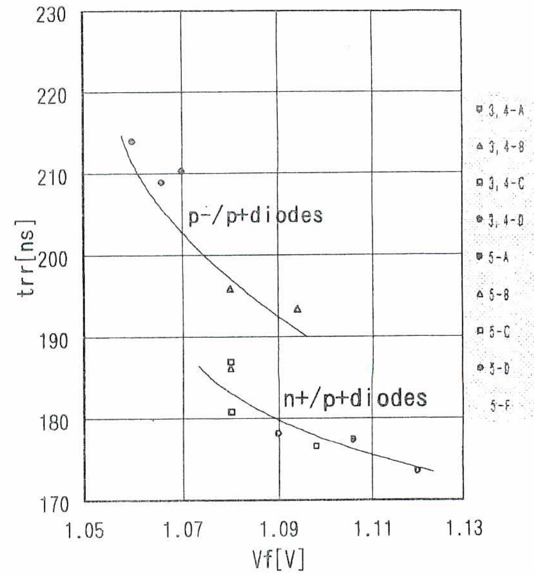

Fig.9 Comparison in trade-off relation between t_{rr} and forward voltage for n+/p+ diodes and p-/p+ diodes.

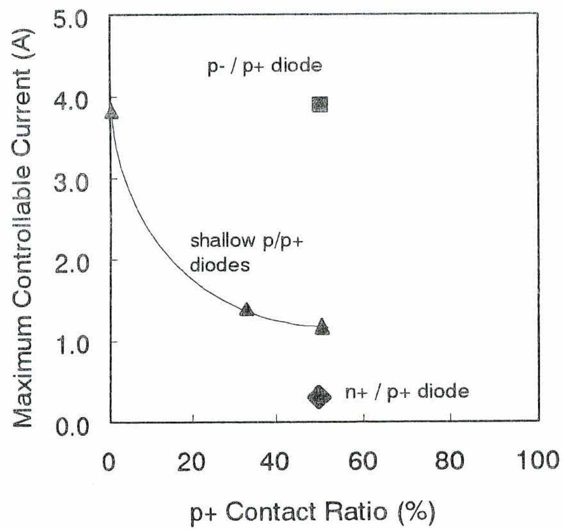

Fig.8 Maximum controllable current as a function of p+ contact ratio over total p-emitter area. Maximum controllable current of n+/p+ diodes and p-/p+ diodes are shown together.