Achieving Material Limit Characteristics in Silicon Power Devices

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Abstract: The present paper predicts the silicon limit characteristics of IGBTs, and proposes a novel device structure to achieve the limit. For power MOSFETs, the electrical characteristics have been sufficiently improved, so that the peripheral circuits are required to be improved for faster switching. The authors propose an ideal gate drive to realize the ultimate high speed switching of power MOSFETs. Integration of power devices and the gate drive circuits in a single chip is considered to be an ideal solution. The authors propose 1 chip solution and demonstrate 12V 10A 1chip DCDC converters. The authors also propose a new FOM for switching speed comparison of power devices.

I. EVOLUTION OF POWER DEVICES

Power devices have evolved so rapidly that 3.3kV IGBTs have even replaced 4.5kV GTOs, which was developed in the late 80's for traction control of bullet trains. Figure 1 and 2 show application fields of power devices in 1997 and 2005, respectively[1]. The distinguished difference between the two figures is that most of the applications of GTO and BTr have been occupied by IGBT and the module.

MOS gate devices are predominantly used in almost all of the application fields, including LDMOS in power ICs, MOSFETs for low voltage and medium voltage applications and IGBTs for high power applications.

Super junction devices were first developed and reported in 1998[2]. They broke through the so-called silicon unipolar device limit in the voltage range from 200V to 700V and significantly enhanced the potential of silicon devices.

Another recent remarkable advancements are seen in high speed trench power MOSFETs, intelligent power module(IPM) and power IC technologies. Trench MOSFET switching speed has been greatly improved since 1999 in order to meet the requirement of high efficiency and high di/dt of Voltage Regulator Modules for CPUs. The details are described in Section III. Progress in IPM was already reviewed in Ref.[3]. Power IC technologies are classified into two categories. One is high voltage SOI power ICs[4] for monolithic DC motor control and PDP flat panel display drive. The other is low voltage power ICs for motor control and power supplies[5]. We have developed the world first 500V 1 and 3 Ampere one chip inverter ICs for DC motor control in 1994 and 1999[4].

Recently, it has been often pointed out that silicon devices face the material limit. It is important to make clear the limit characteristics of silicon devices and the future potential of silicon devices to be exploited. The author also proposes new FOM[6] in order to facilitate achieving the limit characteristics of high speed MOSFET.

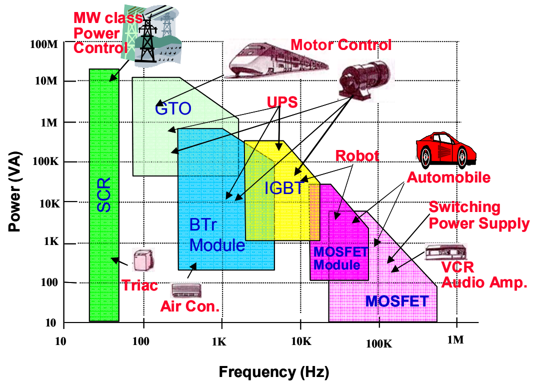

Fig.1 Application fields of power devices in 1997.

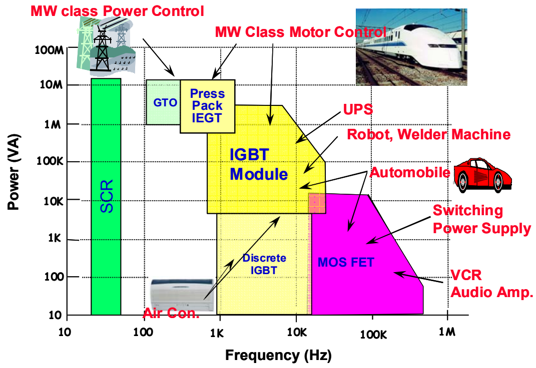

Fig.2 Application fields of power devices in 2005.

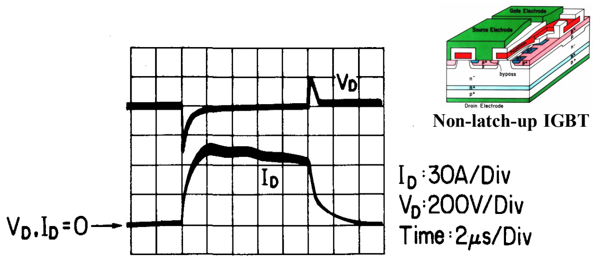

Fig.3 World first demonstration of short-circuit-withstanding capability of no-latch-up IGBT in 1984 (Ref.[11,12]).

II. IGBTs

A. Brief History of IGBT

Concept of IGBTs was first described in the patent by Becke et al[7]. The first challenge for IGBT was reported by Baliga et al. in 1982[8]. Since then, numerous papers were published to improve the device characteristics such as first switching speed[9,10] and large current capability[11].

In early development stage, IGBTs suffered from the latch-up of the parasitic thyristors and the poor current capability. First real IGBTs, or Non-latch-up IGBTs,

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satisfying the concept of Becke, were developed, for the first time, by the authors' group in 1984[11,12]. Figure 3 shows the world first demonstration of load-short-circuit capability of non-latch-up IGBTs.

The electrical characteristic of IGBTs have been steadily improved since the advent of the first IGBT product. However, the theoretical limit of IGBTs has not been discussed yet. In the present paper, the authors present the theory for the silicon limit of IGBT[13].

B. Theory for silicon limit of IGBTs

This section proposes a theory to achieve the lowest forward voltage drop in IGBTs and proposes a new trench gate IEGT/IGBT, realizing the theoretical limit.

The adopted assumption is asymmetrical conduction: "all of the current flows by electrons." Holes contribute only to the conductivity modulation. From the assumption of no hole current flow, the following equations are valid under the high injection condition:

$$J_p = qD_p \frac{\partial p}{\partial x} - q\mu pE = 0 \qquad \text{-----Eq.(1)},$$

$$J_n = J_{Total} = 2 \times qD_n \frac{\partial n}{\partial x} \qquad \text{----Eq.(2)}$$

$$E = \frac{kT}{q}\frac{1}{n}\frac{\partial n}{\partial x} \qquad \text{------Eq.(3)}$$

The situation is satisfied by assuming that the carrier density distribution is approximately a linearly decreasing function from cathode to anode. The current density(J) – voltage(V_F) relation of the silicon limit IGBT can be derived by integrating Eq.(2) with boundary values n_0 and n_W, and using the equations shown below [13,14]:

$$D_n = \frac{a}{n+b}, \quad J=qD_E n_0^2/Q, \quad V_F = V_i + V_{diff},$$

$$V_i = (kT/q)\ln(n_w/n_0), \quad V_{diff} = (kT/q)\ln(n_0 n_w/n_i^2)$$

$$V_F = \frac{2kT}{q}\ln\left[\frac{1}{n_i}\left\{\left(\sqrt{\frac{QJ}{qD_n}} + b\right)\exp\left(\frac{JW_n}{2qa}\right) - b\right\}\right] + R_{ch}J, \qquad \text{...... Eq.(4)}$$

where R_{ch}, Q and W_N denote the channel resistance, the p-emitter dose and n-base width, respectively. n_o and n_W denote the electron densities at the both ends of the n-base. a and b are constants. (see Ref.[13] for details.)

Equation (4) predicts that one order of magnitude improvement in the current-voltage relation is possible, compared with those of conventional IGBTs. Fig.4(a) compares the predicted V-I curve and that of conventional 600V IGBT.

In order to realize an ideal IGBT, the author proposes a new IGBT structure, as shown in Fig.4(b), which realizes a very high electron injection efficiency in MOS gate structure. If the trench to trench distance (mesa width) is as thin as the thickness of the inversion layer, the two inversion channel layers on the both trench side walls merge and constitute a high concentration N-type layer in the narrow mesa, serving as a barrier for holes. For example, if the mesa width is less than 40nm, the induced electron density is greater than 5×10^{17} cm^{-3}, and effectively blocks the hole current flow in the mesa, realizing electron injection efficiency of more than 0.9. The proposed narrow mesa IGBT realizes a low forward voltage even with the p-emitter of very low injection efficiency. The details are described in [13].

Figure 5 compares the on-resistance of the theoretical IGBT limit with state of the art devices. Silicon IGBTs will realize low on-resistance even below SiC limit for over 1.5kV range.

The author will also predict a more practical silicon limit in Ref.[19] using the flat carrier profile in the N-base.

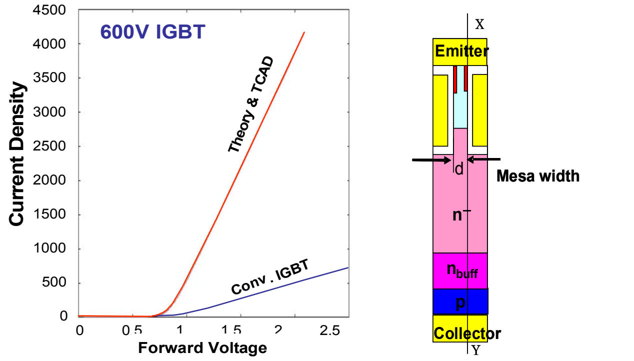


Fig.4(a) Fig.4 (b)

Fig.4(a) V-I curve comparison between proposed theory and conventional 600V IGBTs. Fig.4(b) Proposed IGBTs with narrow mesa structure. Typical silicon mesa width, d, is 20-40 nm

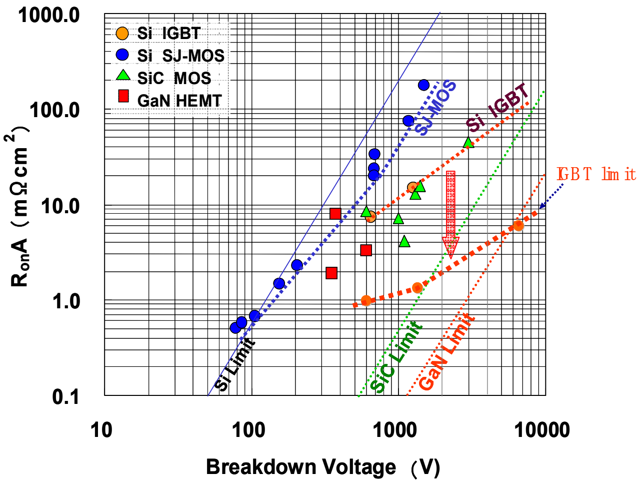


Fig.5 The proposed IGBT, denoted as "IGBT limit," is compared with other devices. Predicted IGBT limit surpasses so called SiC limit for over 1.5kV range.

III. POWER MOSFET

A. Recent advancement in MOSFET

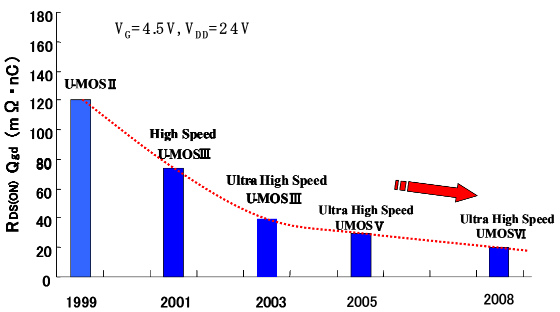


Fig.6 Toshiba's roadmap for high speed MOSFETs

Since 1999, switching speed of power MOSFETs has been greatly improved for the application of VRM (Voltage Regulator Module) for CPUs. The FOM of $R_{on}Q_{gd}$ is conventionally adopted for high speed MOSFETs as a design guide.

Figure 6 shows the Toshiba's roadmap of 30V power MOSFET. $R_{on}Q_{gd}$ was improved from 120mΩnC in 1999 to 30mΩnC in 2005. The buck converter efficiency was improved from 85.5% in 2000 to 90% in 2004.

B. Multi-chip Module

If one try to pursue higher efficiency of synchronous buck converters, it is recognized that the following three items are equally important in addition to the improvement of MOSFETs: (1)reduction in parasitic inductances of the power stage circuits, (2) prevention of self-turn-on of low-side MOSFET, and (3) dead-time optimization.

Figure 7 shows the influence of each parasitic inductance on buck converter efficiency[15]. Each parasitic inductance is defined in the circuit in Fig. 7. The most influential one is the high side MOSFET source inductance, L_{HS}. If the MOSFET is turned-on, the drain current increase rate, dI_D/dt, induces the voltage drop in the parasitic inductance L_{HS}. The induced voltage drop reduces the actually applied gate-source voltage, resulting in the delayed turn-on. In order to realize the first switching-on, the parasitic source inductance should be minimized.

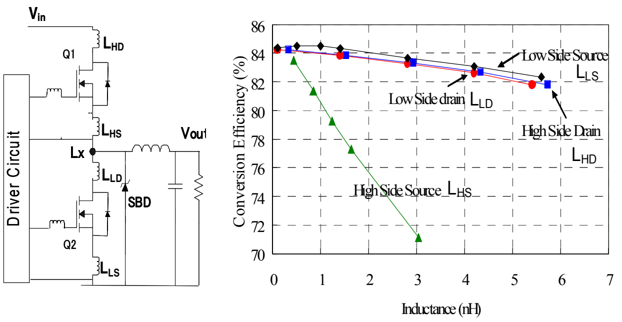


Fig.7 The left figure shows analyzed circuit of buck converter. The right figure shows influence of parasitic inductances on converter efficiency

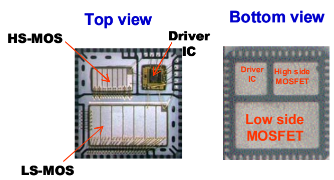


Fig.8 MCM (DrMOS)

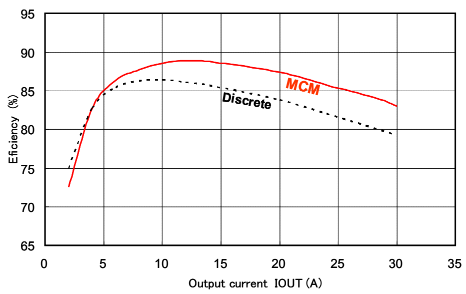


Fig.9 Comparison of converter efficiency between MCM and discrete solution (Input volt:12V, Output volt:1.3V, Switching Freq:1MHz)

The other parasitic inductances increase the voltage spike in the switching transients of high side MOSFET and increase the power loss. The parasitic inductances include the ones inside the package and the ones in the PCB board. In order to reduce the parasitic inductances and resistances, multi-chip module (MCM) was developed.

Figure 8 shows MCM, called DrMOS, proposed by Intel. Three chips of high-side and low-side MOSFETs and the driver circuit are mounted in the single package, thus minimizing the parasitic impedances. DrMOS improves converter efficiency by 4% as shown in Fig.9, even if the same rated MOSFET chips are used.

C. Future technology for Multi-Chip-Module[1]

In the conventional gate drive circuit, switching speed is determined by Q_{gd}/I_g. The total power loss is expressed as follows:

$$P_{loss} = R_{on} I_D + I_D V_D \frac{Q_{gd}}{I_g} f + \frac{1}{3} Q_{ds} V_D f + Q_G V_G f, \quad ..... \quad \text{Eq.(5)}$$

where the 1st, 2nd, 3rd and the 4th terms show on-state loss, switching loss, main junction capacitance loss and gate charge loss, respectively. The main junction capacitance loss is assumed as $Q_{ds}V_D/3$, where Q_{ds} denotes the output charge, Q_{oss}. The coefficient is 1/3, not 1/2. The reason is described in Appendix.

If the power loss is determined by the first two terms in Eq.(5), the product of R_{on} and Q_{gd} can be used reasonably as a figure of merit (FOM) for MOSFETs.

If the gate drive circuit impedance is assumed to be very low and if the value of Q_{gd}/I_G is negligibly small, the 2nd term in Eq.(5) disappears. The switching loss is determined only by the main junction capacitance loss as shown in Eq.(6).

$$P_{loss} = R_{on} I_D + \frac{1}{3} Q_{ds} V_D f + Q_G V_G f \qquad \text{-----Eq.(6)}$$

Again, if the gate loss assumed to be small compared with the first two terms, $R_{on}Q_{ds}$ is regarded reasonably as a new FOM[6], which is discussed in detail in the next Section.

In Fig. 10, it is confirmed by TCAD that 30V MOSFETs can be switched-off in 2nsec if a very low impedance gate drive is used. If the gate and the source is shunted with, for example, a 1mΩ resistor, when turned-off, there is no plateau in the gate voltage waveform, originating from Q_{gd}/I_G[16].

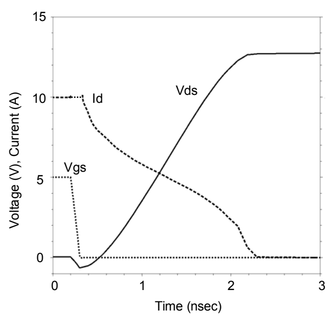


Fig.10 TCAD results of MOSFET Turn-off with ideal gate drive circuit. The turn-off time is 2 ns.

The low impedance gate drive is especially effective for MCM with low voltage MOSFETs or monolithic solution, because low impedance gate circuits can be easily implemented.

It should be noted that the switching-off loss, $Q_{ds}V_D/3$, does not depend on the magnitude of the drain current. This is the distinguished difference from the conventional switching, whose switching loss depends on the Q_{gd} value and the drain current.

Figure 11 compares the efficiency of DCDC converters for the two gate drive conditions of conventional gate drive circuit and the low impedance (0.4Ω) gate drive circuit. For the low impedance gate drive condition, the efficiency will improve and achieve more than 90% at 30A output current even if the same MOSFETs are used. These results imply that the efficiency in DC-DC converters is still expected to be improved in future. In fact, it is predicted that more than 95% conversion efficiency is expected even for 30A output current, as seen in Fig.11, if we can develop ultimate MOSFETs with the silicon limit specific on-resistance of 5mΩmm^2 with retaining low Qgd value of 0.67nCmm^{-2}.

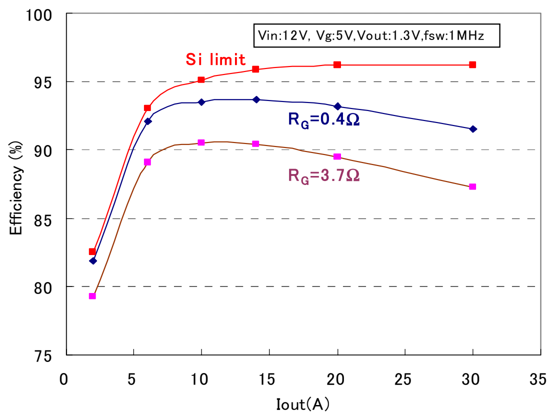


Fig.11 Dependence of efficiency on gate circuit resistance, R_G.
The line "Si limit" shows the efficiency obtained with silicon limit MOSFET of 5mΩmm^2 Ron described in the text.

D. New FOM [1, 6]

In this section, we introduce a new figure of merit, NFOM, based on Equation(6).

NFOM = $R_{on}Q_{str} = T_{sw}V_F$ -------Eq.(7)

, where Q_{str} is stored carrier quantity between the drain and the source terminals. For MOSFETs, Q_{str} is equivalent to Q_{ds}. Switching time, T_{sw}, and forward voltage, V_F, are expressed as follows:

$$T_{sw} = \frac{Q_{str}}{I_D},\ V_F = R_{on} I_D \qquad \text{-------Eq.(8)}$$

The maximum switching frequency of a specific device is directly related to NFOM through Eq.(6).

Q_{str} and R_{on} are represented by the following equations, if ideal R_{on} of Eq.(10) is assumed and if the applied voltage is approximately the same as the breakdown voltage of the device:

$Q_{str}=\varepsilon E_C$ ------Eq.(9)

$R_{on}=4V_{BD}^2/\varepsilon\mu E_C^3$ ------Eq.(10)

Then, the NFOM is expressed as follows for the case of the ideal silicon device:

NFOM=$4V_{BD}^2/\mu Ec^2 = 4V_{BD}^2$/BHFOM ---Eq.(11)

The NFOM value is closely related to the BHFOM under the special assumptions. NFOM can be defined for each device, including bipolar devices.

It should be noted that Q_{str} depends on the operating condition just like Q_{gd}. Equation (9) assumes that the applied voltage is almost the same as the breakdown voltage.

As for 30V silicon MOSFET, device simulation shows that the turn-off time is expected to be 2 nsec by ideal gate drive as shown in Fig.10. This value coincides with the one calculated from Q_{str}/I_D.

Figure 12 shows comparison of NFOM among various devices. NFOM of IGBTs depends on the design of the devices. The squares show the NFOM of the IGBTs proposed in Section II. The circles show high speed IGBTs, having flat carrier density distribution. Super-junction MOSFETs indicated by circles show the ideal simulation results. SiC MOSFETs are plotted, using the product of the reported on-resistance values. NFOM value of GaN FETs is calculated by multiplying the reported on-resistance and two-dimensional electron gas density of 1x10^{13}cm^{-2}.

Reported SiC MOSFETs are not far better than silicon super junction MOSFETs because the currently available on-resistance is not sufficiently low from the view point of NFOM.

For less then 100V range, conventional silicon MOSFETs are superior, and are expected to be even better than new material devices.

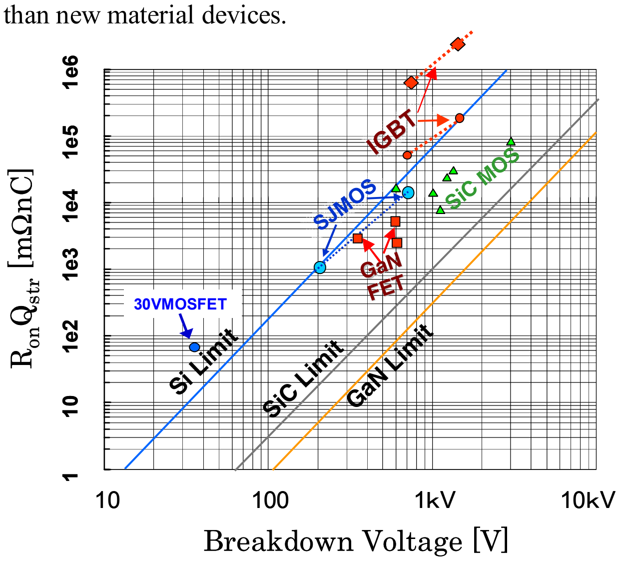
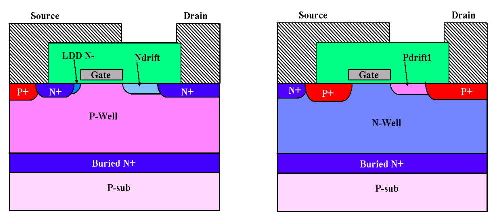


Fig.12 $R_{on}Q_{str}$ as function of breakdown voltage



(a)Nch LDMOS (b)Pch LDMOS
Fig.13 Cross-sectional view of 20V output power devices.

IV. 12V 10A ONE CHIP DCDC CONVERTER

A good method to realize the ideal gate drive circuit of very low impedance is to integrate the driver circuits with the power MOSFETs. This can be easily realized using lateral MOSFET and BCD power IC technology. It is highly expected that high speed switching can be realized in the integrated solution. In this chapter, we demonstrate 10A operation and high speed switching in the integrated solution.

A. Device Structure

Figure 13 shows a cross-sectional view of 20V output LDMOS devices based on 0.6µm BiCD process. The buried N$^+$ layer is electrically connected to the source electrode to reduce the coupling between the drain and the substrate. Three metal layers with a 3µm thick top metal layer are utilized. We adopted Pch LDMOS as the high side switch in our chip.

For the optimized Nch LDMOS, the typical breakdown voltage, the threshold voltage and the specific on-resistance are 25.0V, 0.85V and 23.1mΩmm^2, respectively.

B. Bump Technology

It is generally true that the specific on-resistance of lateral MOSFETs deteriorates considerably with increase in device size due to the increased interconnection resistance. In order to reduce the interconnect resistance, bumping technology was adopted.

Figure 14 shows the simplified images for the layout pattern of the top metal of the chip and the Cu pattern on a printed circuit board (PCB). The chip is attached to the PCB board through bump balls.

The thick Cu metal layers in the PCB can be used as interconnection wires and electrically connect the drain and source bumps. This method significantly reduces the interconnection resistances of lateral MOSFETs.

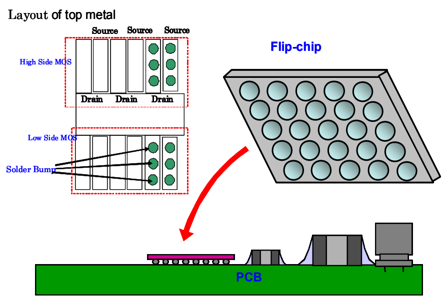


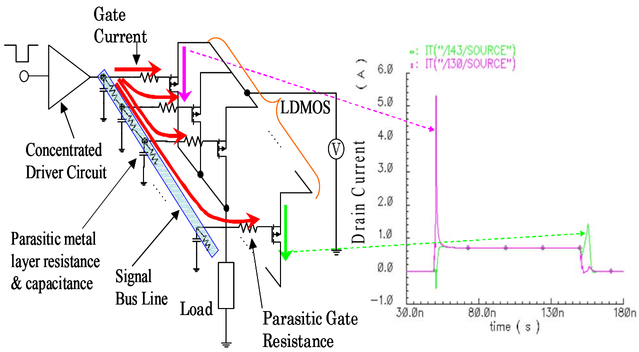
Fig.14 Assembled image of chip in PCB. The drain and the source bumps are electrically connected by parallel running thick Cu metals in the PCB

C. Distributed Driver Layout

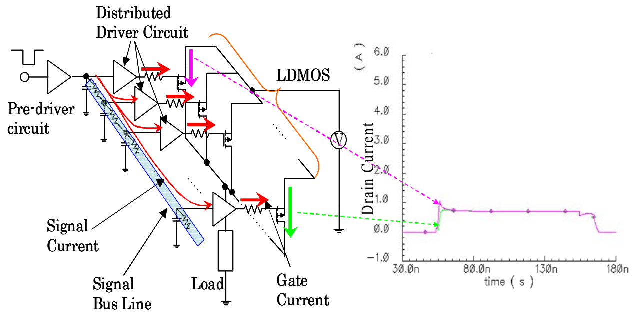
When the area of LDMOS is large, the gate current becomes increasingly large. The whole LDMOS device doesn't uniformly turn-on or -off because the gate drive delay may occur within the large LDMOS device area due to the parasitic resistances and the capacitances of the interconnection metal layers. Especially in the turn-off period, the gate delay may cause significant non-uniform switching. We propose "distributed driver circuit layout" to overcome the problem[17]

Figure 15 compares the distributed driver circuit layout and the conventional concentrated driver circuit layout. In the concentrated driver circuit layout (a), large gate current causes non-uniform gate voltage distribution. In the distributed driver circuit layout (b), a number of gate drivers are formed in the local regions nearest to the LDMOS device segments. The length between the each driver and the each segmented LDMOS is made as short as possible. The current magnitude in the signal bus line electrically connecting the pre-driver and the gate drivers is small, and does not cause the gate signal delay.

We compared the switching of LDMOS's between the distributed driver circuit and the concentrated driver circuit when the input voltage, the load resistance and switching frequency are 12V, 1.2Ω and 780kHz, respectively. Figure 15(a) and (b) compares the simulated transient characteristics of the drain current for the nearest segment LDMOS and the farthest segment LDMOS. The whole LDMOS devices can be uniformly turned-on and -off for the distributed driver case. The LDMOS turn-off loss with distributed driver circuit can be reduced to 54% of that with concentrated driver circuit.



(a) Concentrated driver circuit layout



(b) Distributed driver circuit layout

Fig. 15 Comparison of distributed driver circuit with concentrated driver circuit. Inserted figures show simulated transient waveforms.

D. Experimental Results

Figure 16 shows the micrograph of the fabricated chip based on the low cost 0.6µm process. The chip size is 20.3mm^2. A number of driver circuits are placed between N-ch and P-ch LDMOS.

Figure 17 shows the measured output characteristics of a large area Nch LDMOS (the effective area 3.6mm^2). The on resistance is 9.7mΩ (@drain current=5A, gate voltage=5V).

Figure 18 shows the switching characteristics of the fabricated chip at the condition of an inductance of 2µH. Vi(HighSide), Vi(LowSide) and V(sw) indicate the input gate signals for P-ch LDMOS and N-ch LDMOS and the drain voltage of the P-ch and the N-ch LDMOS devices, respectively. The rise time of V(sw) is 3ns. The fabricated device in the one-chip DC/DC converter exhibited high speed and high current switching capability of 10A.

Figure 19 shows the measured dependence of efficiency on the switching frequency when the input voltage and the output voltage is 12V and 1.3V, respectively. The difference of maximum efficiency is only 1.1% when the switching frequency is changed from 487kHz to 980kHz.

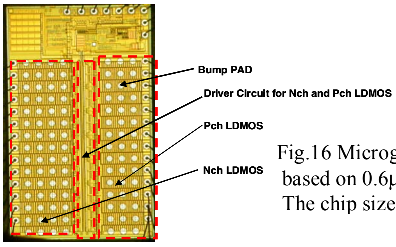


Fig.16 Micrograph of fabricated chip based on 0.6μm process. The chip size is 20.3mm^2

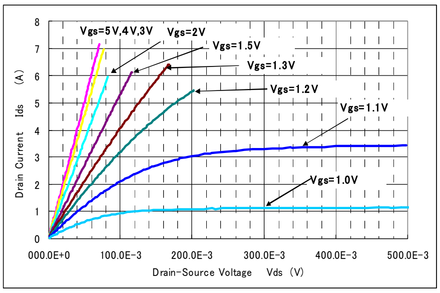


Fig.17 Output characteristics of a large area device with bump technology(the effective area 3.6mm^2).

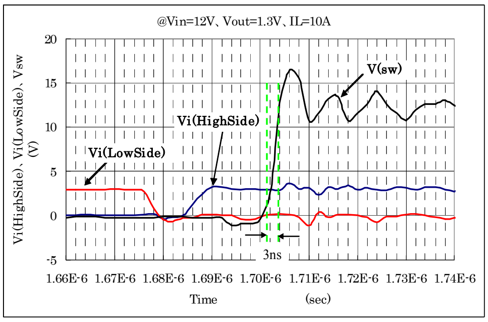


Fig.18 The switching characteristics of the fabricated chip at the condition of an inductance 2uH. The rise time of switching node is 3ns.

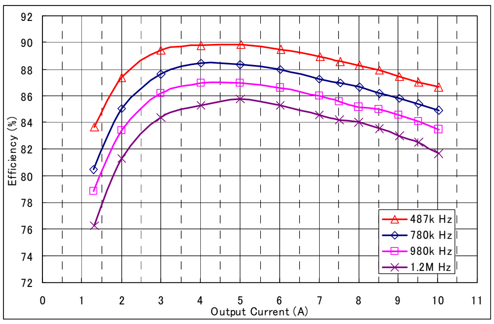


Fig.19 Measured efficiency vs. output current with switching frequency as parameter. (@input voltage=12V, output voltage=1.3V)

Appendix for Section III D

The stored energy in the main junction, P_{str}, in the turn-off transient can be calculated, assuming step junction approximation and inductive load, where the drain current, I_D, keeps in the same value within the turn-off transient. Using the voltage, V, as a function of depletion layer width, d, the final result is easily derived in the following.

$$V=\frac{qN_D}{2\varepsilon}d^2,\quad I_D\delta t=qN_D\delta d, V=\frac{I_D^2}{2\varepsilon qN_D}t^2,\quad V_D=\frac{I_D^2}{2\varepsilon qN_D}t_s^2,$$

,where t_s denotes the switching time.

$$Q_{ds}=I_Dt_s=(2\varepsilon qN_DV_D)^{\frac{1}{2}}\quad P_{loss}=\int_0^{t_S}VI_Ddt=\frac{I_D^3}{6\varepsilon qN_D}t_s^3=\frac{1}{3}Q_{ds}V_D$$

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