Silicon Limit Electrical Characteristics of Power Devices and ICs

Akio Nakagawa, Yusuke Kawaguchi and Kazutoshi Nakamura
Toshiba Corporation, Semiconductor Company
580-1, Horikawa-Cho, Saiwai-Ku, Kawasaki, 212-8520, Japan;
E-mail:akio.nakagawa@toshiba.co.jp

Abstract

The present paper predicts the silicon limit characteristics of IGBTs, and proposes a novel device structure to achieve the limit. Power MOSFETs have been greatly improved for DC-DC converter applications. It is shown that achieving higher efficiency in the converters necessitates the integration of power MOSFETs and the peripheral circuits in a single package. The authors propose an ideal gate drive to realize the ultimate high speed switching of power MOSFETs. Monolithic Integration of power devices and the gate drive circuit is considered to be an ideal solution. The authors report the development of 12V 10A 1chip DC-DC converters. The authors also propose a new FOM for switching speed comparison of various power devices.

Keyword: IGBT, Silicon Limit, MOSFET, MCM, Low impedance gate drive, DC-DC Converter

I. EVOLUTION OF POWER DEVICES

Power devices have evolved so rapidly that 3.3kV IGBTs have displaced 4.5kV GTOs, which were developed in the late 80's for traction control of bullet trains. Figure 1 and 2 compare application fields of power devices in 1997 and 2005, respectively[1]. The distinguished difference between the two figures is that most of the applications of GTO and BTr have been replaced by those of IGBT and the module.

MOS gate devices are predominantly used in most of the application fields, including LDMOS in power ICs, MOSFETs for low voltage and medium voltage applications and IGBTs for high power applications.

Super junction MOSFETs were developed and reported in 1998[2]. They broke through the so-called silicon unipolar device limit in the voltage range from 200V to 900V and significantly enhanced the potential of silicon devices.

Another recent remarkable advancements are seen in high speed trench power MOSFETs and power IC technologies. Switching speed of trench MOSFETs has been greatly improved since 1999 in order to meet the requirement of high efficiency and high di/dt of Voltage Regulator Modules for CPUs. The details are described in Section III. Power IC technologies are classified into two categories. One is high voltage SOI power ICs[3,4] for monolithic DC motor control and PDP flat panel display drive. The other is low voltage power ICs for motor control and power supplies[5]. We developed the world first 500V one chip inverter ICs for DC motor control in 1994[4]. In the present paper, We demonstrate 10A operation of 1 chip DC-DC converters in Section IV.

Recently, it has been often pointed out that silicon devices face the material limit. It is important to make clear the limit characteristics of silicon devices and the future potential to be exploited. The authors also propose new FOM[6] in order to compare the potential of various power devices.

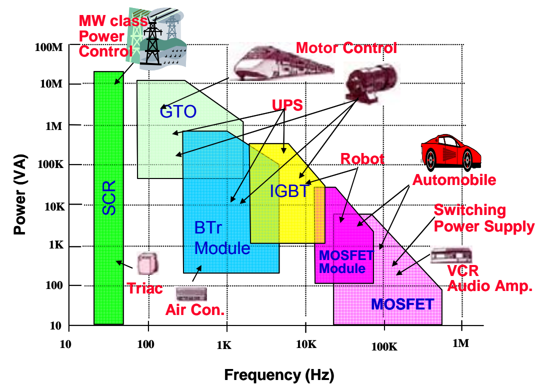


Fig.1 Application fields of power devices in 1997.

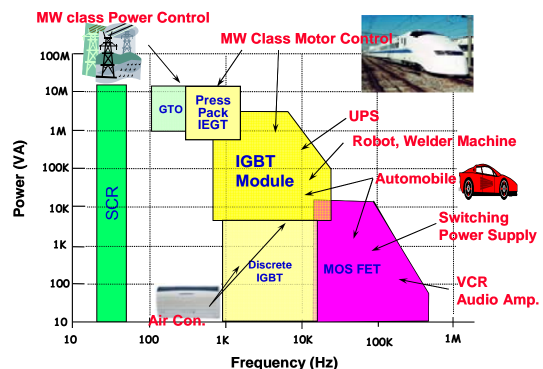


Fig.2 Application fields of power devices in 2005.

II. IGBTs

A. Brief History of IGBT

The concept of IGBTs was first described in the patent by Becke et al[7]. The first challenge for IGBT was reported by Baliga et al. in 1982[8]. Since then, numerous papers were published to improve the device characteristics such as first switching speed[9,10] and large current capability[11].

In the early development stages, IGBTs suffered from the latch-up of the parasitic thyristors and the poor current capability. First real IGBTs, or Non-latch-up IGBTs, completely suppressing the parasitic thyristor action, were developed by the authors' group in 1984[11,12]. It was revealed that the non-latch-up IGBTs exhibited an extraordinarily large safe operating area so that they achieved so-called short-circuit-withstanding capability, for the first time[11], in the IGBT history.

The electrical characteristics of IGBTs have been greatly improved since the advent of the first IGBT products from Toshiba in 1985. However, the theoretical limit of IGBTs has not been discussed yet. In the present paper, the authors present the theory for the silicon limit of IGBT[13].

B. Theory for Silicon Limit of IGBTs

This section proposes a theory of the lowest forward voltage drop in IGBTs and also proposes a new trench gate IGBT, realizing the theoretical limit[13].

The adopted assumption is asymmetrical conduction: "all of the current flows by electrons." Holes contribute only to the conductivity modulation. From the assumption of no hole current flow, the following three equations are valid under the high injection condition:

$$J_p = -qD_p \frac{\partial p}{\partial x} + q\mu_p pE = 0 \qquad \text{-----Eq.(1),}$$

$$J_n = J = 2 \times qD_n \frac{\partial n}{\partial x} \qquad \text{----Eq.(2)}$$

$$E = \frac{kT}{q}\frac{1}{n}\frac{\partial n}{\partial x} \qquad \text{-----Eq.(3)}$$

The above three equations are satisfied by the carrier density distribution which is approximately a linearly decreasing function from cathode to anode as shown in Fig.3. The electron density, n, is assumed to be equal to the hole density, p. The final current density - voltage relation of Eq.(9) can be derived by integrating Eq.(2) with the boundary values n_0 and n_W, defined in Fig.3, together with Eqs.(5-8). The electron diffusion coefficient, D_n, is approximated by

$$D_n = \frac{a}{n+b}, \qquad \text{--------Eq.(4)}$$

where a and b are constants (a=3.7e18, b=9.39e16). The total current, J, is equal to the electron diffusion current flowing into the p-emitter and is given by

$$J = qD_{pe}n_0^2/Q\ , \qquad \text{------Eq.(5)}$$

where Q and D_{pe} denote the total dose of the p-emitter and the electron diffusion coefficient in the p-emitter.

The forward voltage, V_F, is given by the summation of the voltage drop in the n-base, V_i, and the diffusion voltage for the carriers in the n-base, V_{diff}.

$$V_F = V_i + V_{diff}. \qquad \text{------Eq.(6)}$$

$$V_i = (kT/q)\ln(n_w/n_0). \qquad \text{-------Eq.(7)}$$

$$V_{diff} = (kT/q)\ln(n_0 n_w/n_i^2). \qquad \text{-------Eq.(8)}$$

The final current voltage relation is given by Eq.(9).

$$V_F = \frac{2kT}{q}\ln[\frac{1}{n_i}\{(\sqrt{\frac{QJ}{qD_{pe}}} + b)\exp(\frac{JW_i}{2qa}) - b\}] + R_{ch}J. \qquad \text{......... Eq.(9)}$$

In the equation, W_i and R_{ch} denote the n-base width and the channel resistance, respectively.

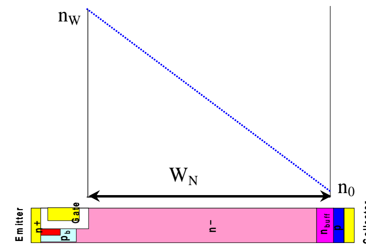


Fig.3 Linearly graded carrier distribution in N-base

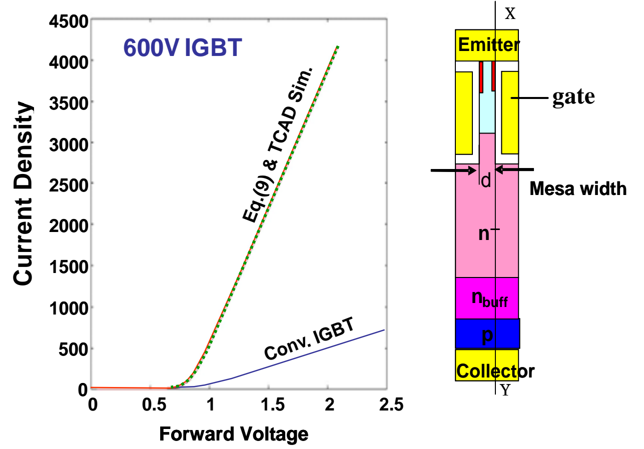


Fig.4(a) Fig.4 (b)

Fig.4(a) Eq.(9) is plotted and compared with conventional 600V IGBTs. The TCAD simulation result of the proposed structure Fig.4(b) exactly coincides with the Eq.(9).

Fig.4(b) Proposed IGBTs with narrow mesa structure. The silicon mesa width, d, is 40 nm and the trench depth is 2µm.

Fig.4(a) compares Eq.(9) and the current-voltage curve of conventional 600V IGBT. Equation (9) predicts that one order of magnitude improvement in the current-voltage relation is possible, compared with those of conventional IGBTs.

In order to realize the silicon limit characteristics, the author proposes a new IGBT structure[13], as shown in Fig.4(b). If the trench to trench distance (mesa width) is as narrow as the thickness of the inversion layer, the two inversion channel layers on the both trench side walls merge with each other and the whole mesa region

becomes an inversion layer. For example, if the mesa width is less than 40nm, the induced electron density is greater than $5\times10^{17}cm^{-3}$. The inversion layer effectively blocks the hole current flow in the mesa, realizing the situation that most of the current flows by electrons. The calculated current voltage curve of the proposed narrow mesa IGBT exactly agrees with the current voltage relation of Eq.(9), as shown in Fig.4(a).

C. Practical IGBT Limit

The current-voltage curve significantly depends on the mesa width as seen in Fig.5. Practically speaking, the forward voltage is substantially low if the mesa width is below 0.5μm. In this section, we propose "practical silicon limit" of IGBTs, using an assumption: flat carrier profile in the n-base. The current flows in the n-base only by drift under the assumption, and the electron density, n, is assumed to be equal to the hole density. The total current is given by

$$J = J_n + J_p = q(\mu_n + \mu_p)nE. \qquad \text{------Eq.(10)}$$

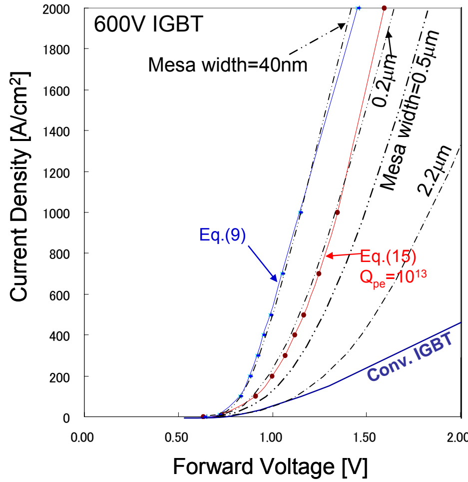


Fig.5 Calculated V-I curves of 600V IGBT by TCAD are shown with mesa width as a parameter. Eqs.(9) and (15) are also plotted and compared with calculated results.

The current-voltage relation, Eq.(15), for the practical limit can be derived using Eqs.(10-14).

$$E = \frac{V_i}{W_i}, \qquad \text{------Eq.(11)}$$

$$V_{diff} = \frac{2kT}{q}\ln\left(\frac{n}{n_i}\right) \qquad \text{---------Eq.(12)}$$

$$V_F = V_{diff} + V_i, \qquad \text{---------Eq.(13)}$$

$$J_n = qD_{pe}\frac{n^2}{Q} \qquad \text{---------Eq.(14)}$$

$$V_F = \frac{kT}{q}\ln\frac{\mu_n Q J}{qD_{pe}n_i^2(\mu_n+\mu_p)} + W_i\sqrt{\frac{D_{pe}J}{q\mu_n(\mu_n+\mu_p)Q}} + \frac{\mu_n R_{ch}}{\mu_n+\mu_p}J \qquad \text{-----Eq.(15)}$$

In the above equations, V_i V_{diff} W_i, Q, R_{ch} and D_{pe} are defined in the same way as before.

In Fig.5, Eq.(15) is also plotted, assuming R_{ch}=0 and Q_{pe} $=10^{13}cm^{-3}$ for 600V IGBTs. The practical limit current-voltage curve, Eq.(15), agrees with the current-voltage curve of IGBT with 0.2μm mesa. It should be noted that the practical limit can be achieved by IGBTs with moderately narrow mesa and its on-resistance is still very close to the ideal limit as shown in Fig.6.

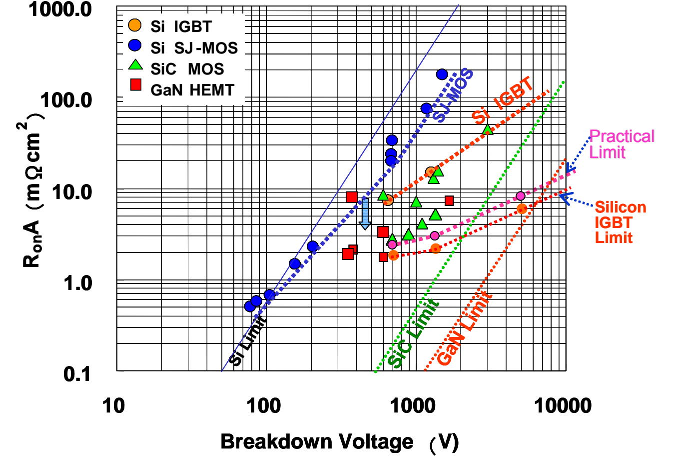


Fig.6 The proposed silicon IGBT limit is compared with other state of the art devices. Theoretically predicted "practical IGBT limit" is shown together. Practical limit is very close to the ideal limit. IGBT theoretical limit even exceed so-called SiC limit for over 2kV region. The figure also shows the reported on-resistances of Super-Junction MOSFETs and new material devices.

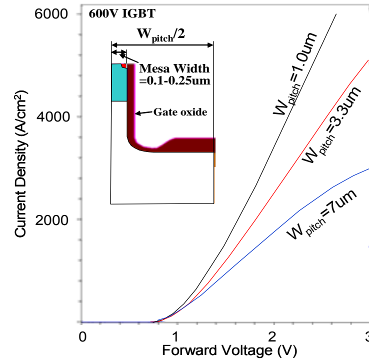


Fig. 7 I-V curves are shown with device cell pitch (W_{pitch}) as a parameter under the condition that flat carrier profile is maintained. Forward voltage is large for IGBT with W_{pitch} of 7μm because the channel resistance is large in spite of a narrow mesa of 0.5μm.

D. Improving IGBT Characteristics

Figure 6 compares the on-resistance of the theoretical IGBT limit with state of the art devices. Silicon limit IGBT will realize a low on-resistance, which is even below the SiC limit for over 2.0kV range.

Higher operating current density is often demanded for an application of hybrid electric vehicles. Chip shrink or an operating current density exceeding $500A/cm^2$ will be realized in IGBTs, if the issue of short-circuit-withstanding capability is properly handled. Figure 7 shows how the current-voltage relation changes as the cell pitch increases under the condition that a flat

carrier density distribution is maintained in the n-base by keeping the mesa width as narrow as between 0.2μm and 0.5μm. As the cell pitch increases, the total channel width decreases and, hence, the saturation current values generally decreases. However, the forward voltage increases inevitably for a higher current density region such as 500A/cm^2.

III. POWER MOSFET

A. Recent Advancement in MOSFET

Fig.8 Toshiba's roadmap for high speed MOSFETs

Since 1999, switching speed of power MOSFETs has been greatly improved for the application of VRM (Voltage Regulator Module) for CPUs. The FOM, $R_{on}Q_{gd}$, is conventionally adopted for high speed MOSFETs as a design guide.

Figure 8 shows the Toshiba's roadmap of 30V power MOSFET. $R_{on}Q_{gd}$ was improved from 120mΩnC in 1999 to 30mΩnC in 2005. The buck converter efficiency was improved from 85.5% in 2000 to 90% in 2004.

B. Optimization of Power Stage in DC-DC Converter

If one try to pursue higher efficiency of synchronous buck converters, it is recognized that the following three items are equally important in addition to the improvement of MOSFETs: (1)optimization in parasitic inductances of the power stage circuits, (2) prevention of self-turn-on of the low-side MOSFET, and (3) dead-time optimization.

Figure 9 shows the influence of each parasitic inductance on buck converter efficiency[15]. Each parasitic inductance is defined in the circuit in Fig. 9. The most influential one is the high side MOSFET source inductance, L_{HS}. If the MOSFET is turned-on, the rapid drain current increase rate, dI_D/dt, induces the voltage drop in the parasitic inductance L_{HS}. The induced voltage drop reduces the actually applied gate-source voltage, resulting in the delayed turn-on. In order to realize the first switching-on, the parasitic source inductance should be minimized.

The other parasitic inductances increase the voltage spike in the switching transients of high side MOSFET and increase the power loss. The parasitic inductances include the ones inside the package and the ones in the PCB board.

In order to reduce the parasitic inductances and resistances, multi-chip module (MCM) was developed.

Figure 10 shows MCM, called DrMOS, proposed by Intel. Three chips of high-side and low-side MOSFETs and the driver circuit are mounted in a QFN56 package, thus minimizing the parasitic impedances. DrMOS improves the converter efficiency by 2% compared with the discrete MOSFET solution as shown in Fig.11.

Fig.9 The left figure shows analyzed circuit of buck converter. The right figure shows influence of parasitic inductances on converter efficiency

Fig.10 MCM (DrMOS) integrates high-side and low-side MOSFETs and the driver circuit in a QFN56 package.

Fig.11 Comparison of converter efficiency between MCM and discrete MOSFET solution (Input volt:12V, Output volt:1.3V, Switching Freq:1MHz)

Figure 12 Dependence of power loss on total parasitic inductance, L_S (=L_{HS}+L_{HD}+L_{LS}+L_{LD}), in the power stage circuit is shown with gate circuit impedance as a parameter. The gate circuit impedance, R_g+R_{driver}, includes the circuit impedance and the gate resistance of the chip. The total power loss does not decrease monotonically as the parasitic inductance decrease.

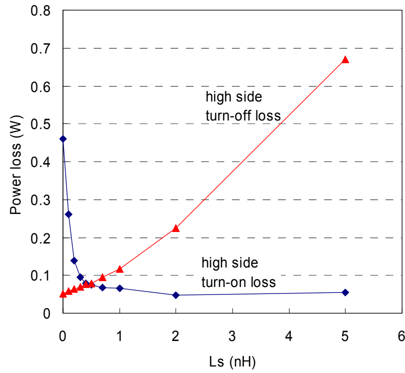
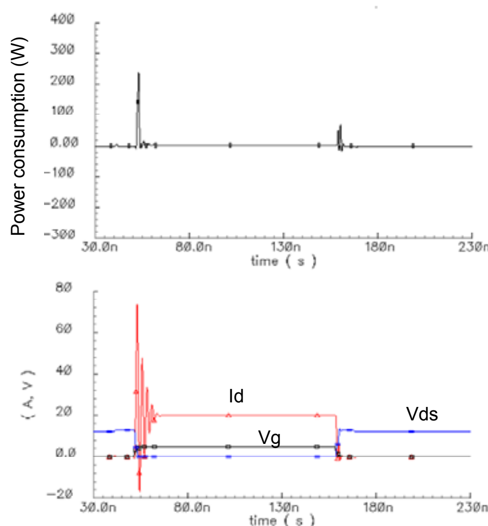
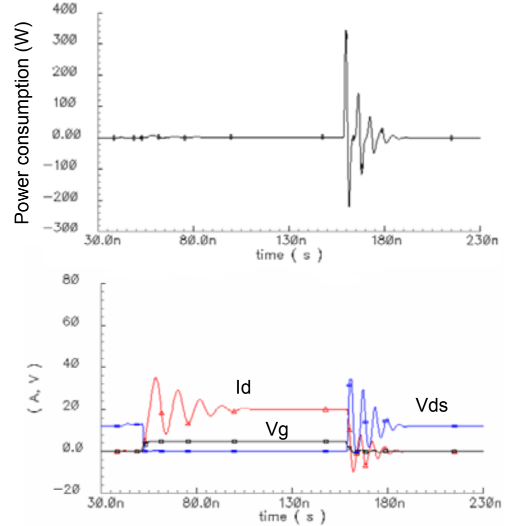


Figure 13 Dependence of high side MOSFET turn-on and turn-off loss on total parasitic inductance, L_S, (= $L_{HS}+L_{HD}+L_{LS}+L_{LD}$.) High side MOSFET turn-on loss increase rapidly as the parasitic inductance (Ls) decreases. The turn-off loss decreases as Ls decrease.

In the following, the optimum parasitic inductance values are further examined by using the sub-circuit model developed and optimized for the power MOSFETs. Fig. 12 shows the dependence of power loss on the total parasitic inductance, L_S ($=L_{HS}+L_{HD}+L_{LS}+L_{LD}$.) The parameter in the figure is the total resistance value of the gate driver circuit. The total resistance includes the gate circuit impedance and the gate resistance of the MOSFET chip. It is found that there is an optimum inductance value that minimizes the total power loss. This is because the turn-on loss of the high side MOSFET increases rapidly as the parasitic inductance value is excessively decreased, as shown in Fig. 13. When the total resistance value of the gate driver circuit reduces from 3.66Ω to 0.4Ω, both the optimum inductance value and the total power loss decrease simultaneously as shown in Fig.12.



(a) Waveforms for Ls=0.1nH



(b) Waveforms for Ls=2.0nH

Figure 14 Calculated waveforms of High side MOSFET during turn-on and turn-off period are shown for the two cases of (a) Ls=0.1nH and (b) Ls=2.0nH in the condition of total gate circuit resistance = 0.4 Ω. In the case of L=0.1 nH, a large power loss occurs during turn-on period. In the case of L=2.0 nH, high side MOSFET drain-source voltage rapidly decreases because a voltage of L di/dt is applied to the parasitic inductance, and high side MOSFET turn-on loss is reduced.

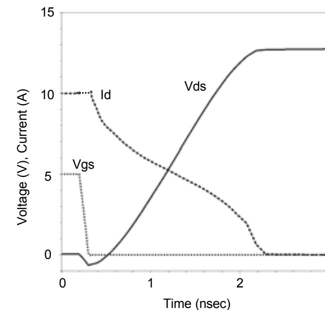


Fig.15 TCAD results of MOSFET Turn-off with ideal gate drive circuit. The turn-off time is 2 ns.

Figure 14 (a) and (b) show the turn-on and turn off waveforms of the MOSFET for the two cases of the total inductance value, Ls, 0.1nH and 2nH, respectively. In the case of Ls=0.1nH, a large power loss occurs in the high side MOSFET during the period of the high side MOSFET turn-on, because a large reverse recovery current of the body diode of the low side MOSFET flows in a short time period. A large voltage drop occurs across the high side MOSFET, because the parasitic inductance is too small to restrict the di/dt. In the case of L=2.0 nH, a large di/dt is prevented by the parasitic inductance of 2nH and the turn-on loss of high side MOSFET is reduced.

It should be noted that the total parasitic inductance in the main current path for the developed MCM module is chosen to be the optimum value.

C. Future Technology for Multi-Chip-Module[1]

In the conventional gate drive circuit, switching speed is determined by Q_{gd}/I_g. The total power loss is expressed as follows:

$$P_{loss} = R_{on} I_D + I_D V_D \frac{Q_{gd}}{I_g} f + \frac{1}{3} Q_{ds} V_D f + Q_G V_G f \,, \quad ..... \quad \text{Eq.(16)}$$

where the 1st, 2nd, 3rd and the 4th terms show the on-state loss, the switching loss, the main junction capacitance loss and the gate charge loss, respectively. The main junction capacitance loss is assumed as $Q_{ds}V_D/3$, where Q_{ds} denotes the output charge, Q_{oss}. The coefficient is 1/3, not 1/2. The reason is described in Appendix.

If the power loss is determined by the first two terms in Eq.(16), the product of R_{on} and Q_{gd} can be used reasonably as a figure of merit (FOM) for MOSFETs.

If the gate drive circuit impedance is assumed to be very low and if the value of Q_{gd}/I_G is negligibly small, the 2nd term in Eq.(16) disappears. The switching loss is determined only by the main junction capacitance loss as shown in Eq.(17).

$$P_{loss} = R_{on} I_D + \frac{1}{3} Q_{ds} V_D f + Q_G V_G f \quad \text{-----Eq.(17)}$$

$$\geq 2\sqrt{R_{on} Q_{ds} \frac{1}{3} I_D{}^2 V_A f} + Q_G V_G f$$

In the above inequality equation, the equality holds if the first and the second terms are equal to each other. Then, the power loss depends on $R_{on}Q_{ds}$. Again, if the third term is assumed to be small compared with the first two terms, $R_{on}Q_{ds}$ is regarded reasonably as a new FOM[6], which is discussed in detail in the next Section.

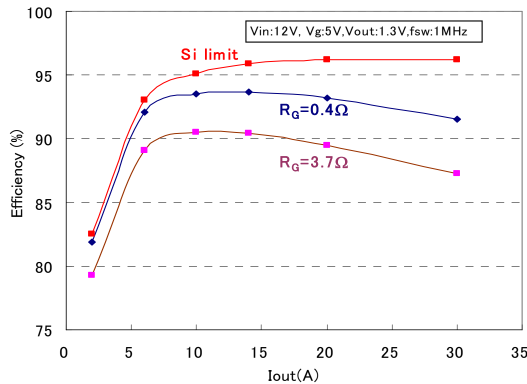


Fig.16 Dependence of converter efficiency on total gate circuit resistance, R_G. The line "Si limit" shows the efficiency obtained with silicon limit MOSFET of 5mΩmm^2 Ron, as described in the text.

In Fig. 15, it is confirmed by TCAD that 30V MOSFETs can be switched-off in 2nsec if a very low impedance (1mΩ) gate drive is used and a sufficiently large gate current is supplied. There is no plateau in the gate voltage waveform, originating from Q_{gd}/I_G[16].

It should be noted that the switching-off loss, $Q_{ds}V_D/3$, does not depend on the magnitude of the drain current. This is the distinguished difference from the conventional switching, whose switching loss depends on the Q_{gd} value and the drain current.

Figure 16 compares the efficiency of DC-DC converters for the gate drive conditions of conventional gate drive circuit and the low impedance (0.4Ω) gate drive circuit. For the low impedance gate drive condition, it is predicted that the efficiency will improve and achieve more than 90% at 30A output current even if the same MOSFETs are used. These results imply that the efficiency in DC-DC converters is still expected to be improved in future. It is also predicted that more than 95% conversion efficiency is expected even for 30A output current, as seen in Fig.16, if we can develop ultimate MOSFETs with the silicon limit specific on-resistance of 5mΩmm^2 with retaining low Qgd value of 0.67nCmm^{-2}.

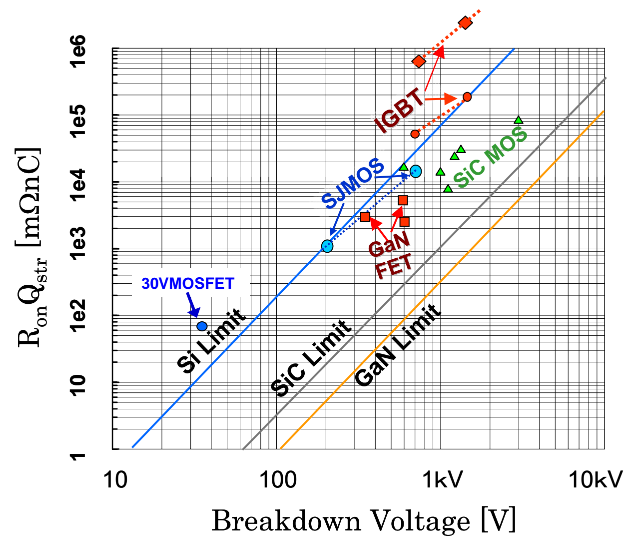


Fig.17 $R_{on}Q_{str}$ as function of breakdown voltage

D. New FOM [1, 6]

In this section, we introduce a new figure of merit, NFOM, based on Equation(17).

$$\text{NFOM} = R_{on}Q_{str} = T_{sw}V_F \,, \quad \text{-------Eq.(18)}$$

where switching time, T_{sw}, and forward voltage, V_F, are expressed as follows:

$$T_{sw} = \frac{Q_{str}}{I_D}, \; V_F = R_{on} I_D \quad \text{-------Eq.(19)}$$

Q_{str} denotes the stored carrier quantity between the drain and the source terminals. For MOSFETs, Q_{str} is equivalent to Q_{ds} (=Q_{oss}).

In the following, NFOM is compared with Baliga's FOM. Q_{str} and R_{on} are represented by the following equations for ideal MOSFETs:

$Q_{str}=\varepsilon E_C$ ------Eq.(20)

$R_{on}=4V_{BD}{}^2/\varepsilon\mu E_C{}^3$ ------Eq.(21)

Then, the NFOM is expressed as follows for the case of the ideal silicon MOSFETs.

$\text{NFOM}=4V_{BD}{}^2/\mu Ec^2 =4V_{BD}{}^2/\text{BHFOM}$ ---Eq.(22)

The NFOM value is closely related to the BHFOM only if the ideal MOSFET is assumed. Equation (20) assumes that the applied voltage is the same as the breakdown voltage.

NFOM can be defined for various devices, including bipolar devices. It should be noted that Q_{str} depends on the operating conditions just like Q_{gd}.

Figure 17 compares NFOM among various devices. NFOM of IGBTs depends on the design of the devices. The squares show the NFOM of the IGBTs proposed in Section IIB. The circles show high speed IGBTs, having flat carrier density distribution. Super-junction MOSFETs indicated by circles show the ideal simulation results. SiC MOSFETs are plotted, using the reported on-resistance values. NFOM value of GaN FETs is calculated by multiplying the reported on-resistance and two-dimensional electron gas density of $1x10^{13}cm^{-2}$.

For less than 100V range, conventional silicon MOSFETs are superior, and the values of their NFOM are lower than those of the new material devices.

IV 12V 10A SINGLE CHIP DC-DC CONVERTER

Figure 18 shows the technology advancement in power ICs. The design rule of power ICs keeps scaling down, following the CMOS learning curve. The reason is shown in Fig.19, where DMOS specific on-resistance is shown as a function of the design rule. Lateral DMOS are frequently used as output power devices in power ICs. The specific on-resistance simply decreases as the design rule becomes small, and thus, chip shrink is possible. This is the main force why we migrate toward finer design.

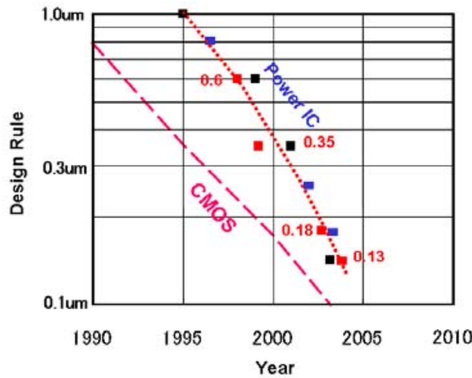


Fig.18 Technology advancement in power ICs

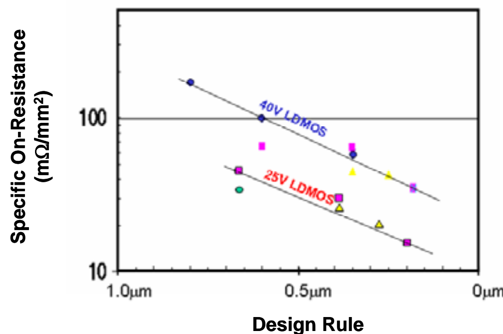
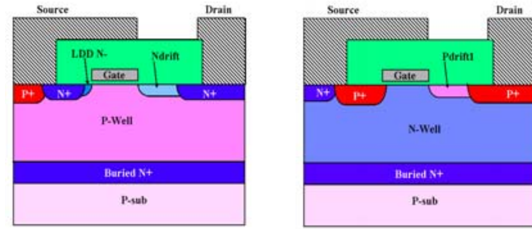


Fig.19 Lateral DMOS on-resistance vs. design rule.



(a)Nch LDMOS (b)Pch LDMOS

Fig.20 Cross-sectional view of 25V output power devices.

A good method to realize a low impedance gate drive circuit is to integrate the driver circuits with the power MOSFETs. This can be easily realized using lateral DMOSFET (LDMOS) and BCD power IC technology. In this chapter, we show the development of 10A 1 chip DC-DC converters and their high speed switching capability.

A. Device Structure

Figure 20 shows a cross-sectional view of 20V output LDMOS devices based on 0.6μm BiCD process. The buried N^+ layer is electrically connected to the source electrode to reduce the coupling between the drain and the substrate. Three metal layers with a 3μm thick top metal layer are utilized.

For the optimized Nch LDMOS, the typical breakdown voltage, the threshold voltage and the specific on-resistance are 25.0V, 0.85V and 23.1mΩmm^2, respectively.

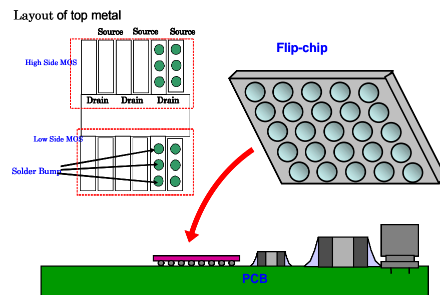


Fig.21 Assembled image of chip on PCB. The drain and the source bumps are electrically connected by thick Cu metal wires in the PCB

B. Bump Technology

It is generally true that the specific on-resistance of lateral DMOS deteriorates considerably with increase in the device size due to the increased interconnection resistance. In order to reduce the interconnection resistance, we adopted the bump technology.

Figure 21 shows the simplified images for the layout pattern of the top metal of the chip and the Cu pattern on a printed circuit board (PCB). The chip is attached to the PCB board through bump balls.

The thick Cu metal layers in the PCB can be used as interconnection wires and electrically connect the drain

and source bumps. This method significantly reduces the interconnection resistances of lateral MOSFETs.

C. Distributed Gate Driver Layout

When the area of LDMOS is large, the gate current becomes increasingly large. The whole LDMOS device doesn't uniformly turn-on or -off because the gate drive delay may occur within the large LDMOS device due to the resistances and the parasitic capacitances of the interconnection metal layers. Especially in the turn-off period, the gate delay may cause significant non-uniform switching. We propose "distributed gate driver circuit layout" to overcome the problem[17]

Figure 22 compares the distributed gate driver circuit layout and the conventional concentrated gate driver circuit layout. In the concentrated gate driver circuit layout (a), large gate current causes non-uniform gate voltage distribution. In the distributed driver circuit layout (b), a number of gate drivers are formed in the local regions nearest to the segmented LDMOS devices. The length between the each driver and the each segmented LDMOS is made as short as possible. The current magnitude in the signal bus line electrically connecting the pre-driver and the local gate drivers is small, and does not cause the gate signal delay.

Figure 22(a) and (b) compares the simulated transient characteristics of the drain currents for the nearest segment LDMOS and the farthest segment LDMOS. The simulation condition is 12V of the applied voltage and 1.2Ω of the load resistance. The whole LDMOS devices can be uniformly turned-on and -off for the distributed driver case. The LDMOS turn-off loss with distributed driver circuit can be reduced to 54% of the LDMOS with concentrated driver circuit.

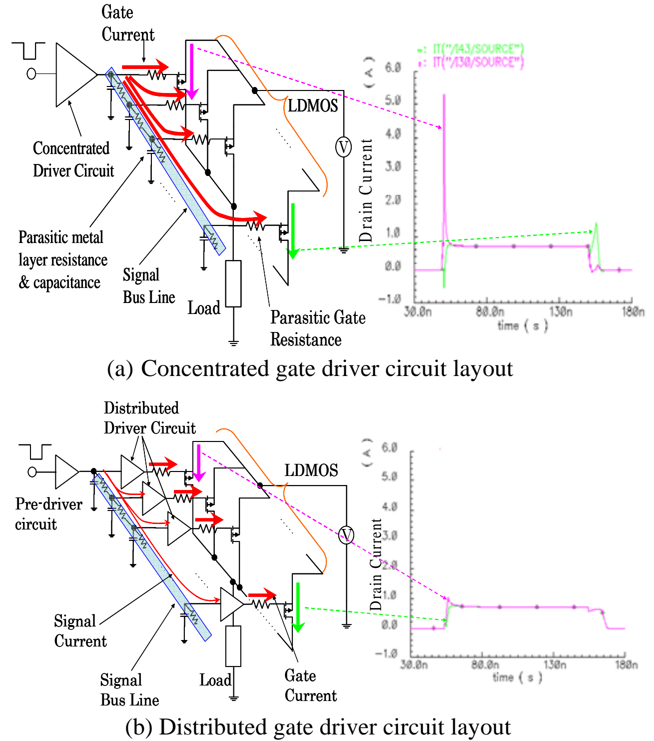
D. Experimental Results

Figure 23 shows the micrograph of the fabricated chip based on the 0.6μm BiCD process. The chip size is 20.3mm^2. A number of local gate driver circuits for segmented LDMOS are placed between N-ch and P-ch LDMOS.

Figure 24 shows the measured output characteristics of a large area Nch LDMOS (the effective area 3.6mm^2). The on resistance is 9.7mΩ (@drain current=5A, gate voltage=5V).

Figure 25 shows the switching characteristics of the fabricated chip at the condition of an inductance of 2μH. Vi(HighSide), Vi(LowSide) and V(sw) indicate the input gate signals for P-ch LDMOS and N-ch LDMOS and the drain terminal voltage of the P-ch and the N-ch LDMOS devices, respectively. The rise time of V(sw) is 3ns. The fabricated device in the one-chip DC-DC converter exhibited high speed and high current switching capability of 10A.

Figure 26 shows the measured efficiency vs. output current when the input voltage and the output voltage is 12V and 1.3V, respectively, and the switching frequency is 780kHz. The measured maximum efficiency is 89% at 5A of current.



(a) Concentrated gate driver circuit layout

(b) Distributed gate driver circuit layout

Fig. 22 Comparison of distributed gate driver circuit and concentrated gate driver circuit. The right hand side figures show the simulated transient waveforms of the drain currents of the nearest and farthest segmented LDMOS's.

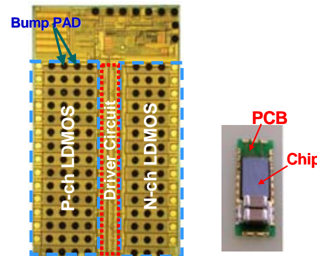


Fig.23 Micrograph of fabricated chip based on 0.6μm process. The chip size is 20.3mm^2

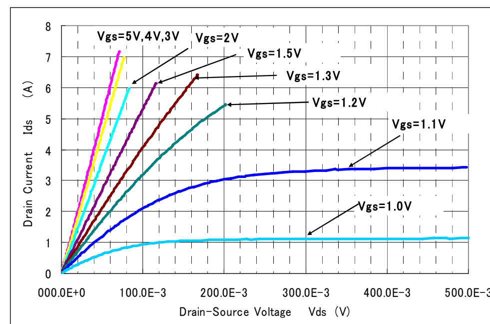


Fig.24 Output characteristics of a large area device with bump technology(the effective area 3.6mm^2).

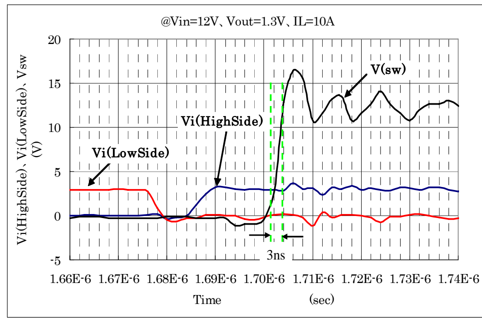


Fig.25 The switching characteristics of the fabricated chip at the condition of an inductance 2uH. The rise time of switching node is 3ns.

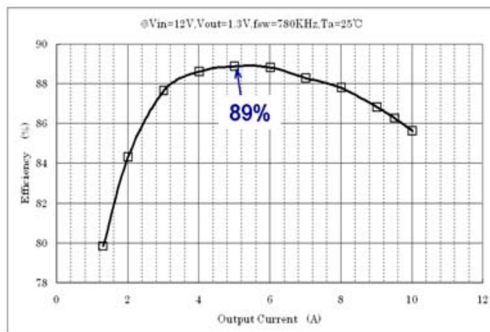


Fig.26 Measured efficiency vs. output current with switching frequency as parameter. (@input voltage=12V, output voltage=1.3V)

APPENDIX for SECTION IIIC

The stored energy in the main junction, P_{str}, in the turn-off transient can be calculated, assuming step junction approximation and inductive load, where the drain current, I_D, keeps in the same value within the turn-off transient. Using the voltage, V, as a function of depletion layer width, d, the final result is easily derived in the following.

$$V = \frac{qN_D}{2\varepsilon} d^2, \quad I_D \delta t = qN_D \delta d, V = \frac{I_D^2}{2\varepsilon q N_D} t^2, \quad V_D = \frac{I_D^2}{2\varepsilon q N_D} t_s^2,$$

,where t_s denotes the switching time.

$$Q_{ds} = I_D t_s = (2\varepsilon q N_D V_D)^{\frac{1}{2}} \quad P_{loss} = \int_0^{t_S} V I_D dt = \frac{I_D^3}{6\varepsilon q N_D} t_s^3 = \frac{1}{3} Q_{ds} V_D$$

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