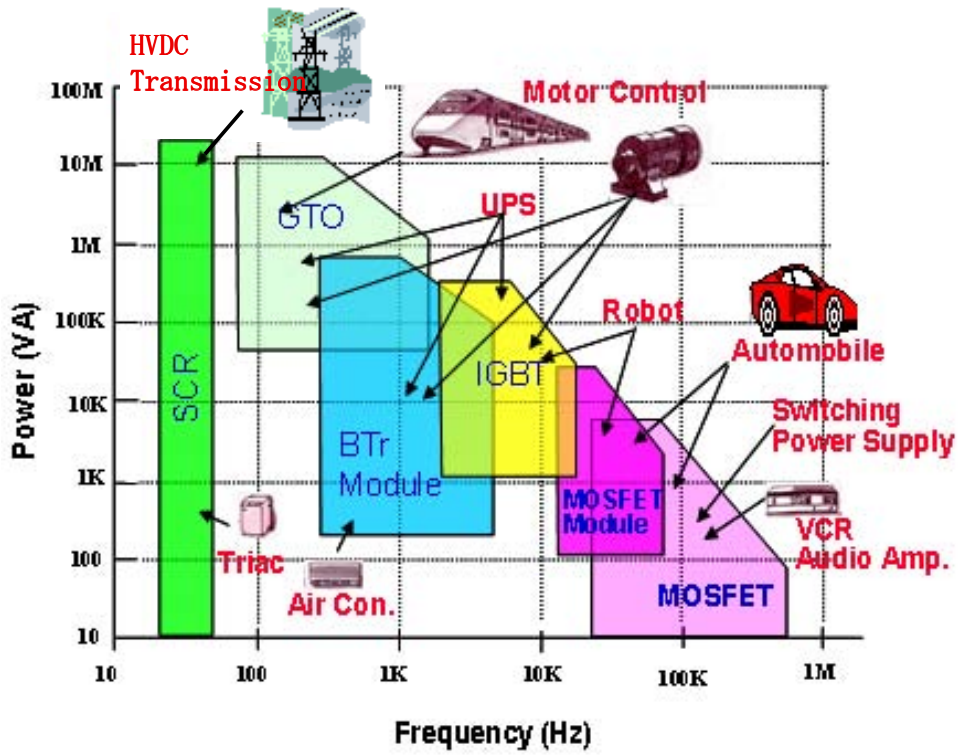
世界を動かすシリコンパワー半導体
ー ー発展の経緯と未来

中川 明夫
中川コンサルティング事務所

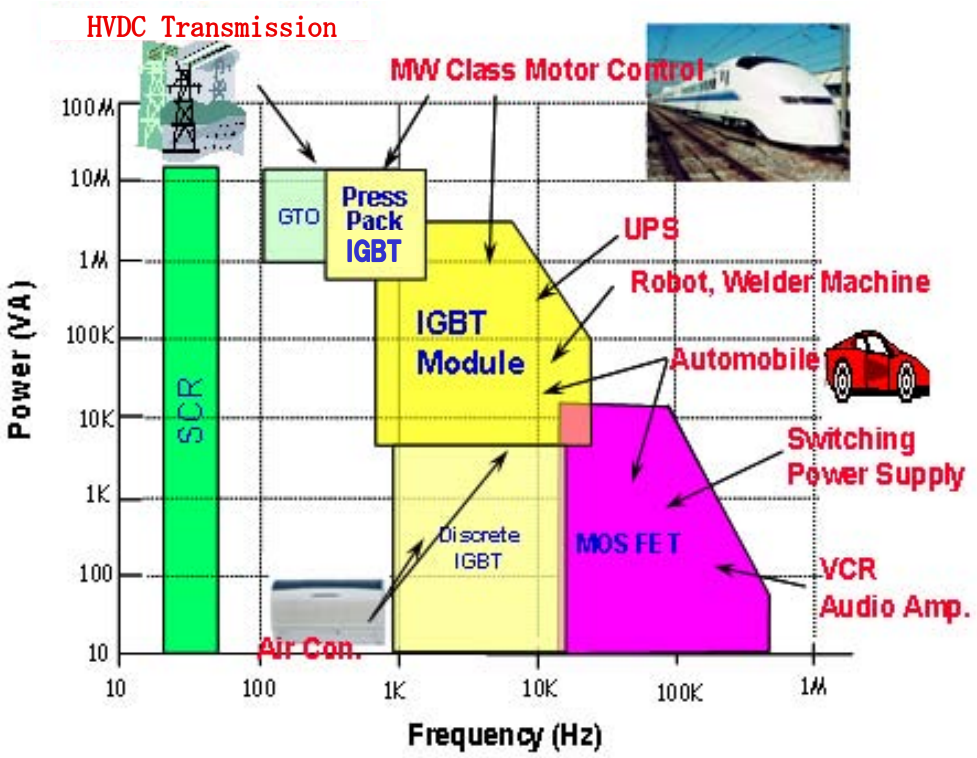

ペトラ遺跡

Application fields of Power Devices

1997

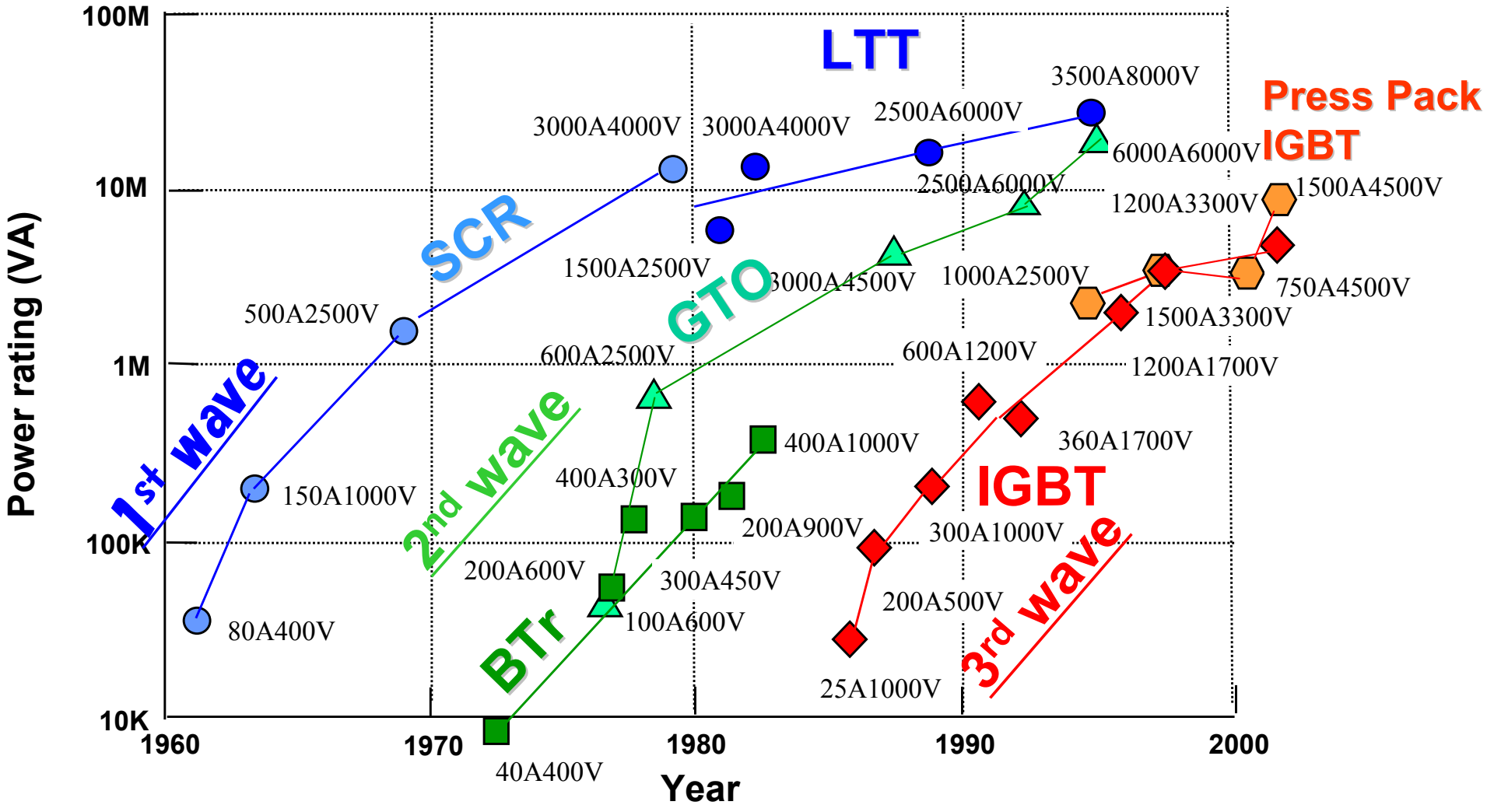


2005



Evolution of high power devices in Toshiba

Three waves in device development



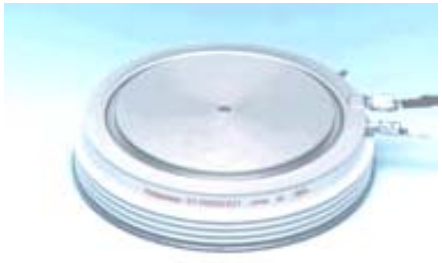
IGBT replaced GTO in Shinkansen (Super Express Train)

Inverter control improves energy efficiency in motor control

9 years

Model 300 (1990)

GTO inverter



SG3000GXH24

Model 700 (1999,2002)

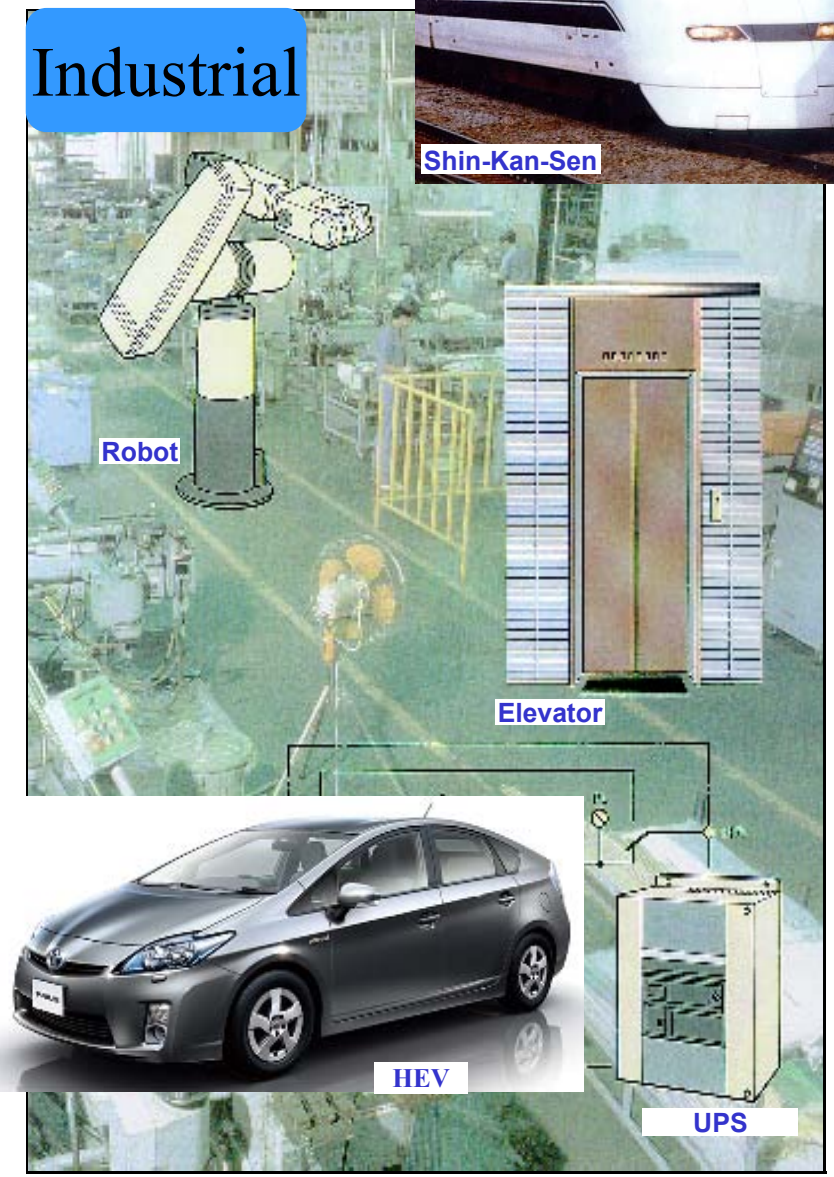
IGBT inverter

ST1000EX21

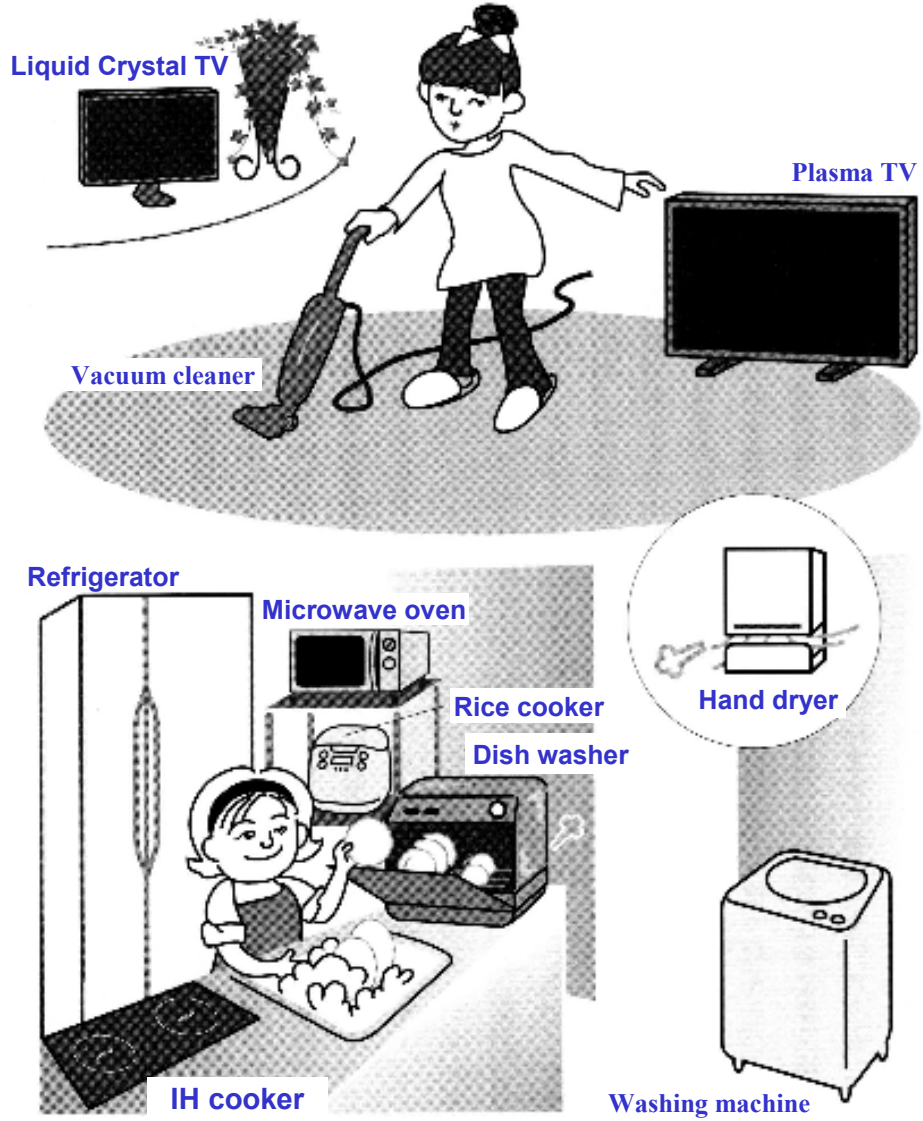
MG1200FXF1US53

IGBTの応用

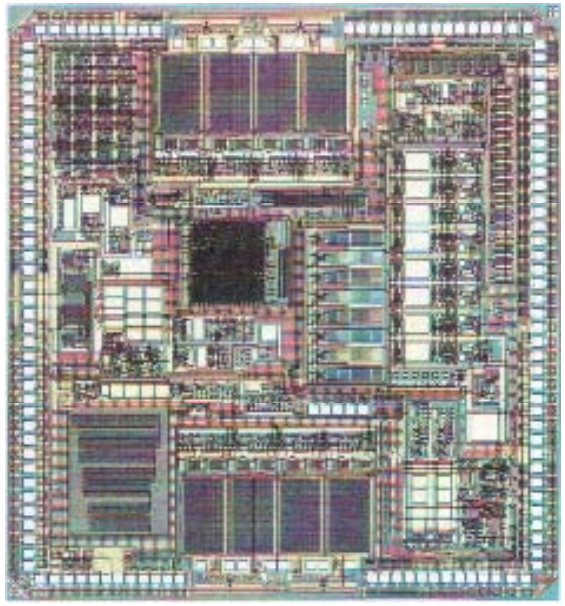
Industrial



Home Appliances

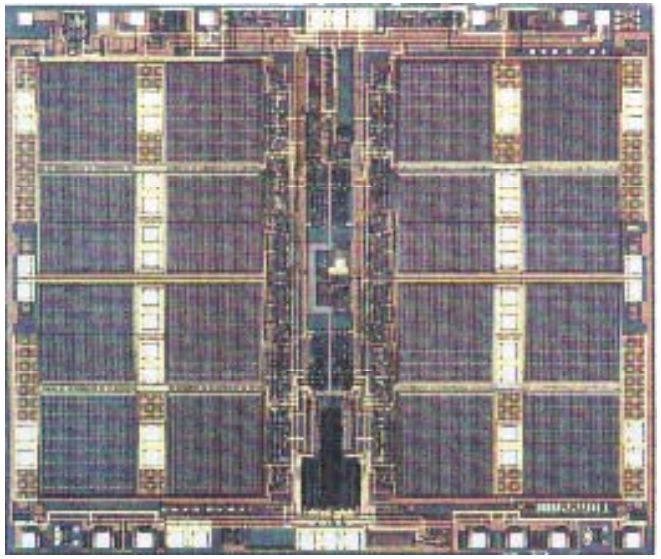


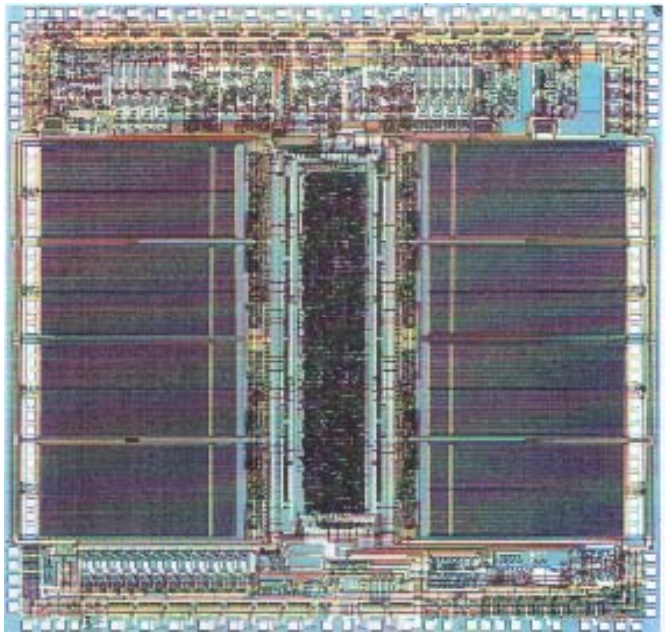
低耐圧パワーIC（BiCD）



Engine control

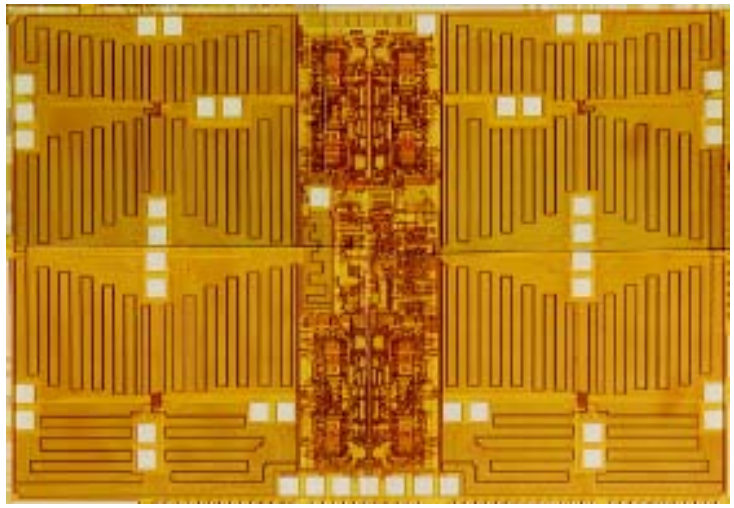
Stepping motor driver





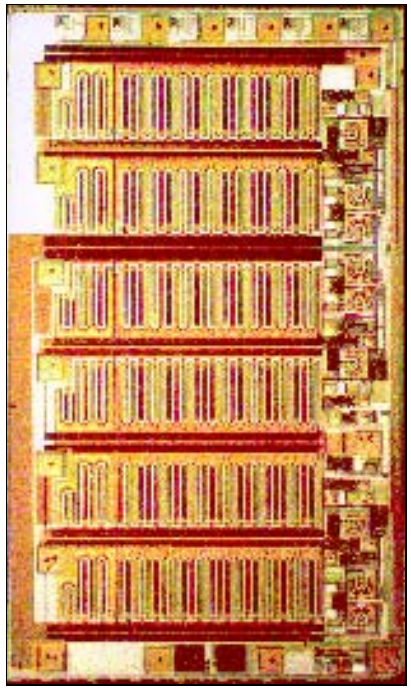
ABS

40W Audio amplifier



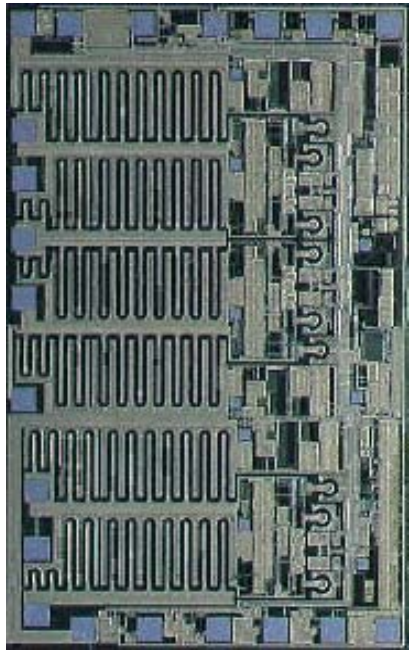
高耐圧パワーIC　インバータを1チップ化

500V,1A(1994)
Toshiba



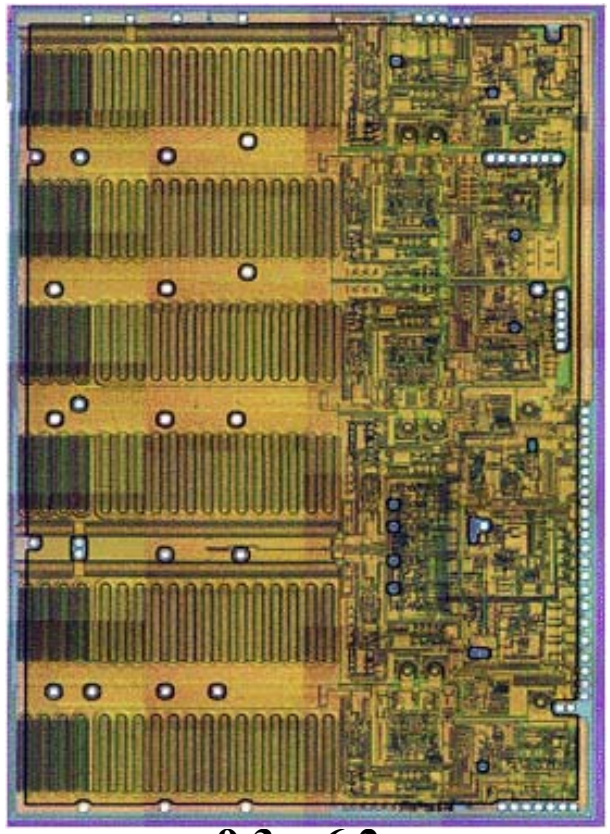
7 x 4.2
15μmSOI,
Trench Isolation,
1.5μm 5V BiCMOS

500V, 1A(2002)
Toshiba



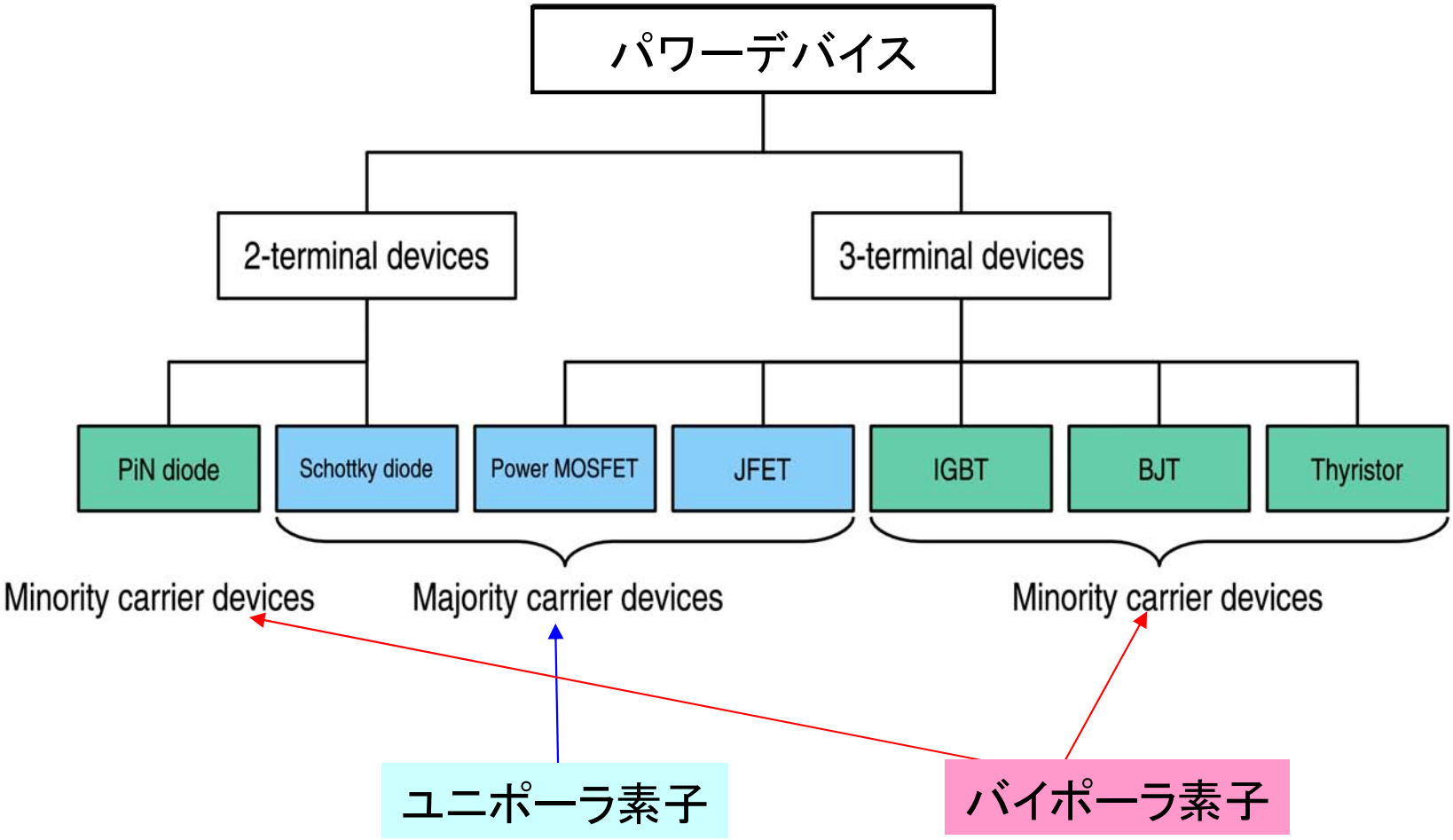
6.6 x 4.1
15μmSOI
Trench Isolation,
2μm 30V CMOS Analog

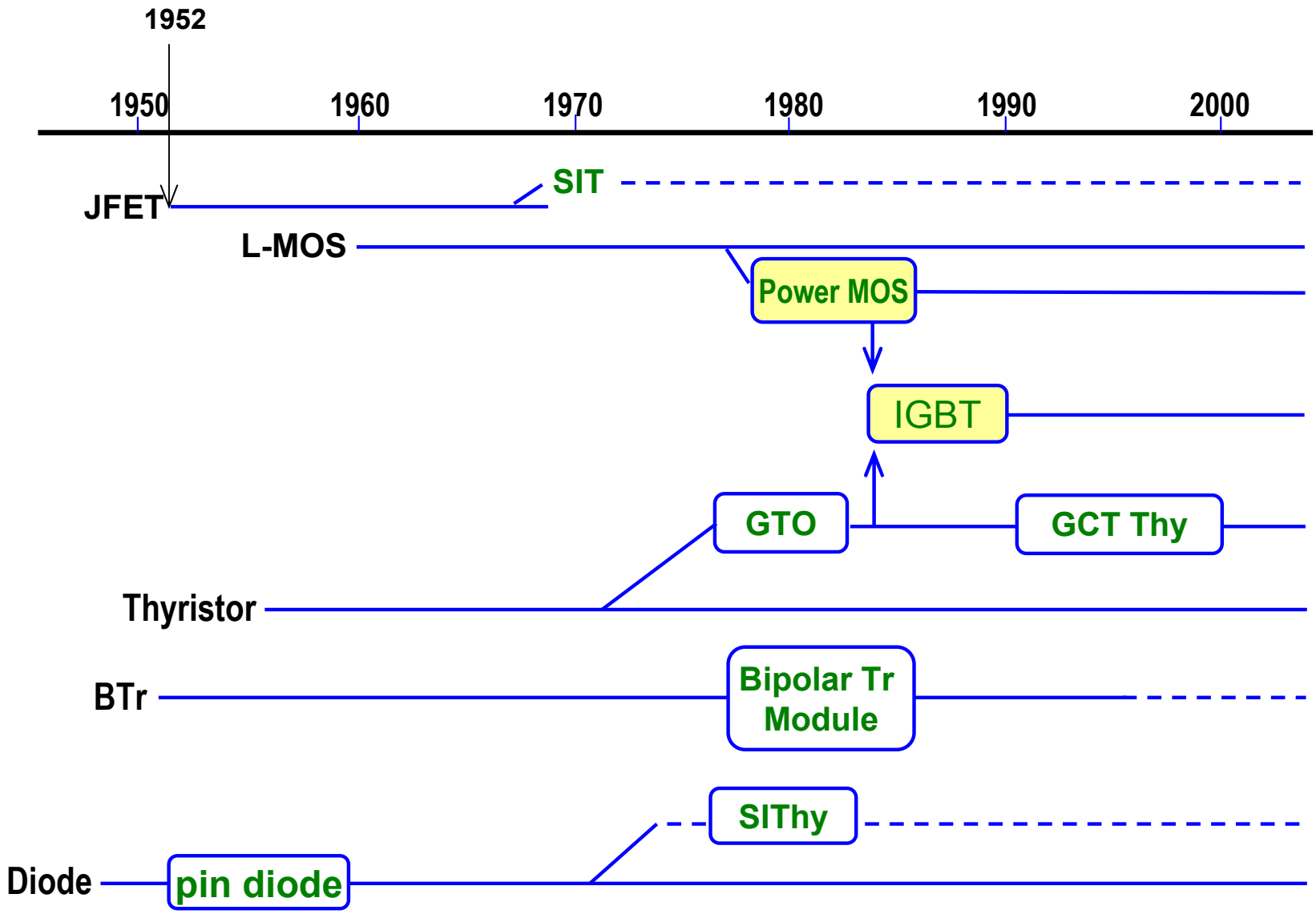
750V, 4.5A(2011)
Denso



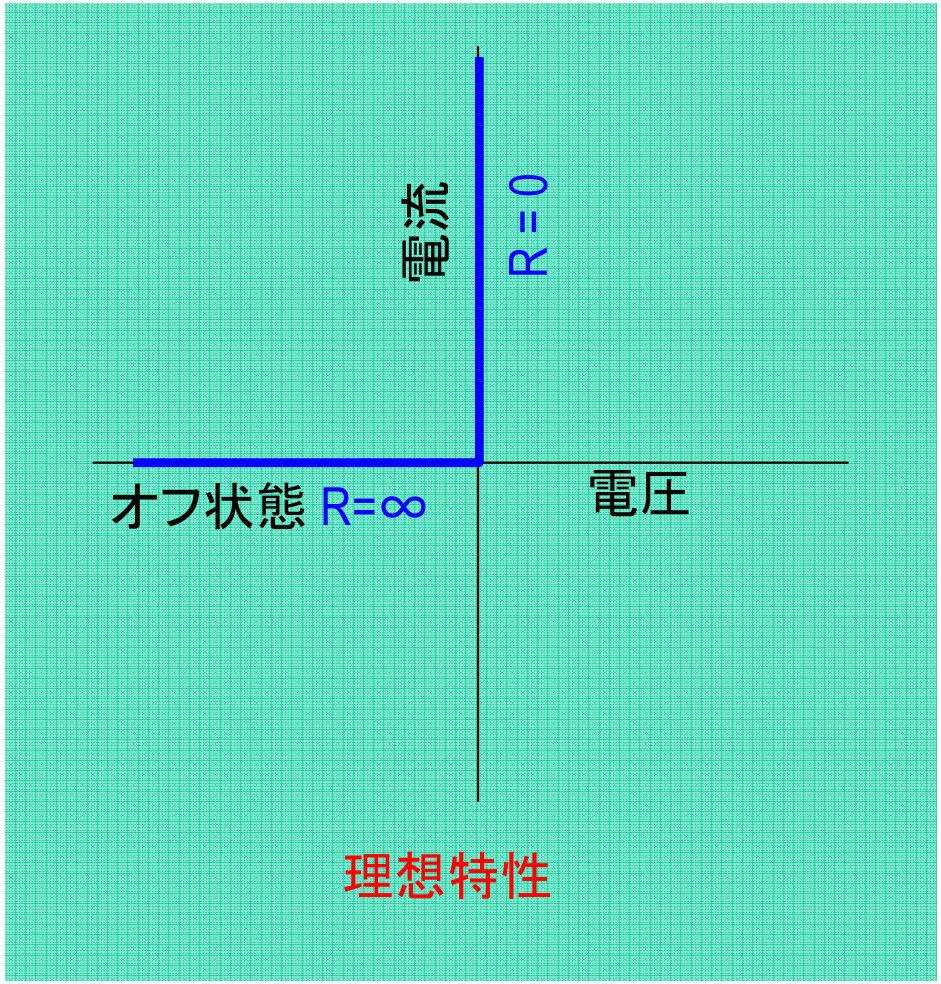
9.3 x 6.2
15μmSOI,
Trench Isolation,
0.6μm 5V BiCMOS

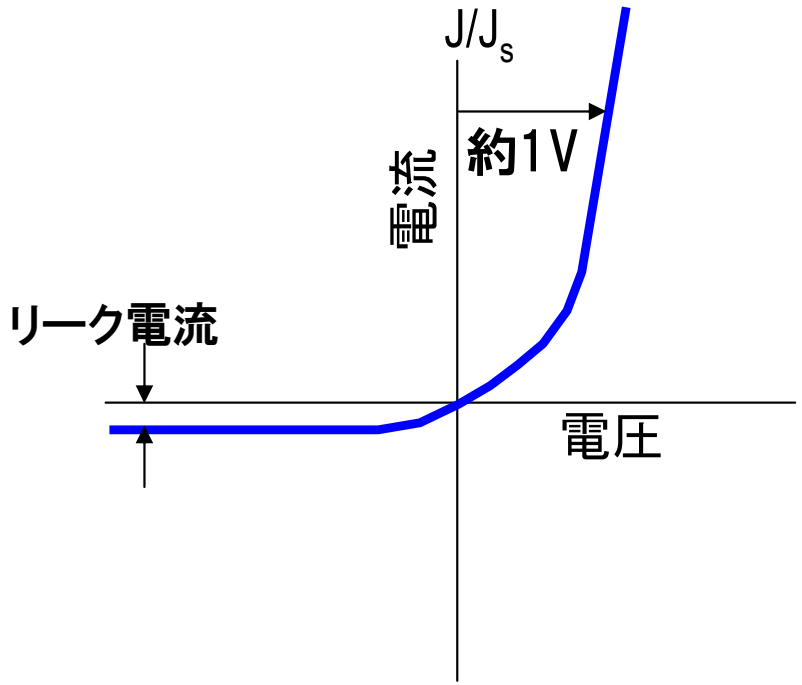
主たるパワー素子


パワーデバイス
2-terminal devices
3-terminal devices
PiN diode
Schottky diode
Power MOSFET
JFET
IGBT
BJT
Thyristor
Minority carrier devices
Majority carrier devices
Minority carrier devices
ユニポーラ素子
バイポーラ素子

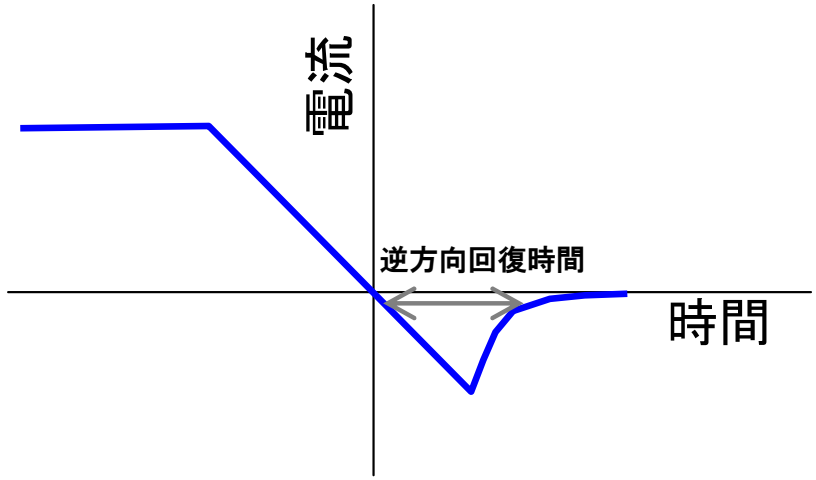

1952
1950
1960
1970
1980
1990
2000
JFET
SIT
L-MOS
Power MOS
IGBT
GTO
GCT Thy
Thyristor
BTr
Bipolar Tr
Module
SIThy
Diode
pin diode

Diode特性





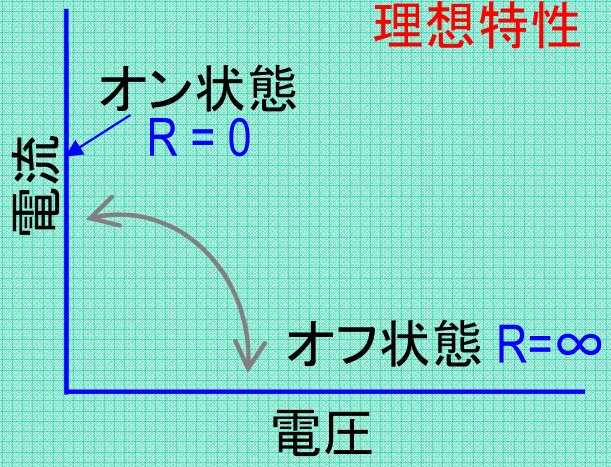
電流電圧特性

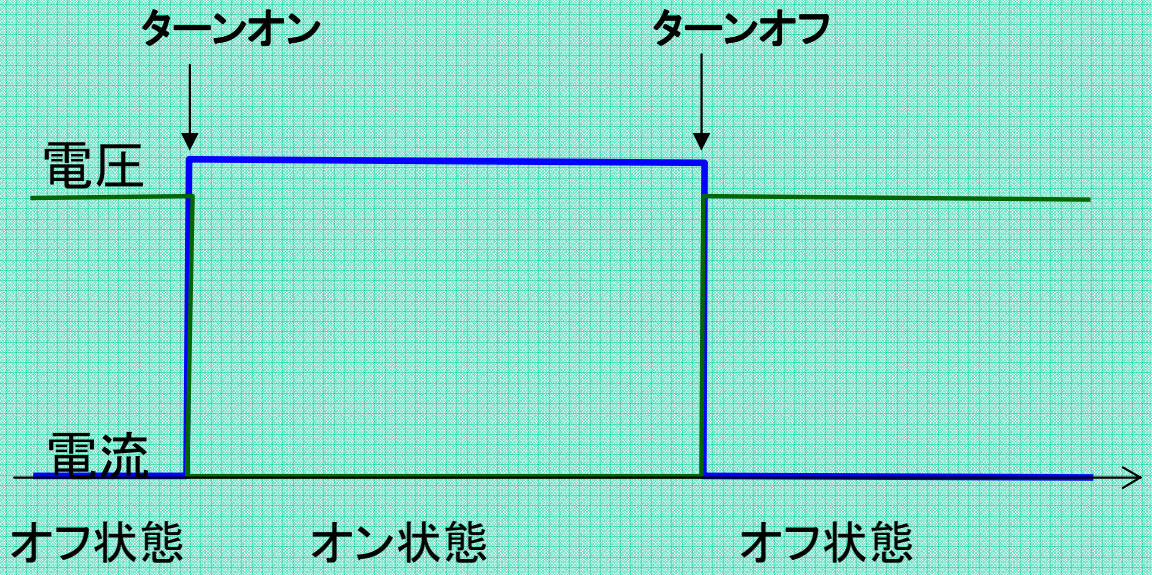


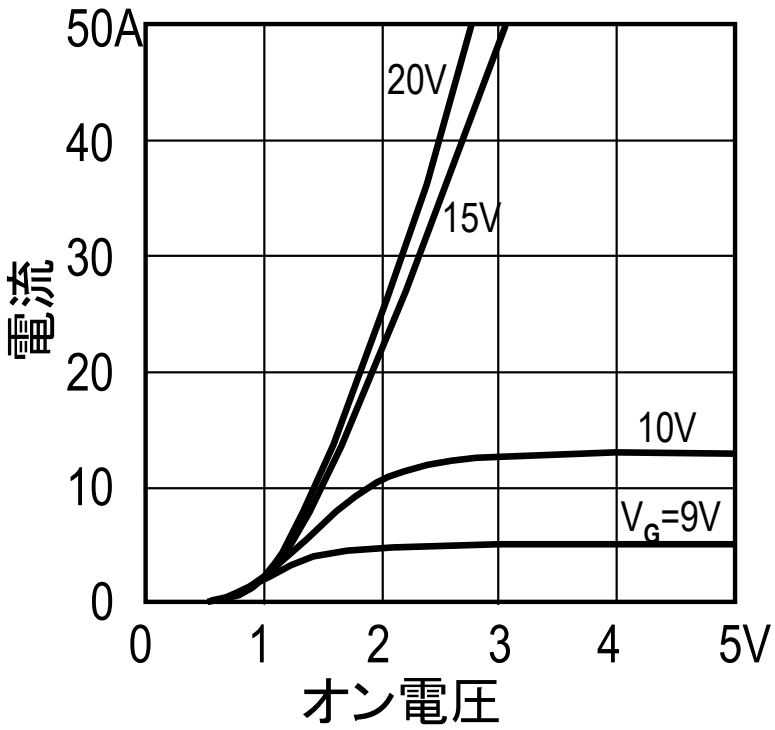
スイッチング特性

IGBT特性：スイッチ

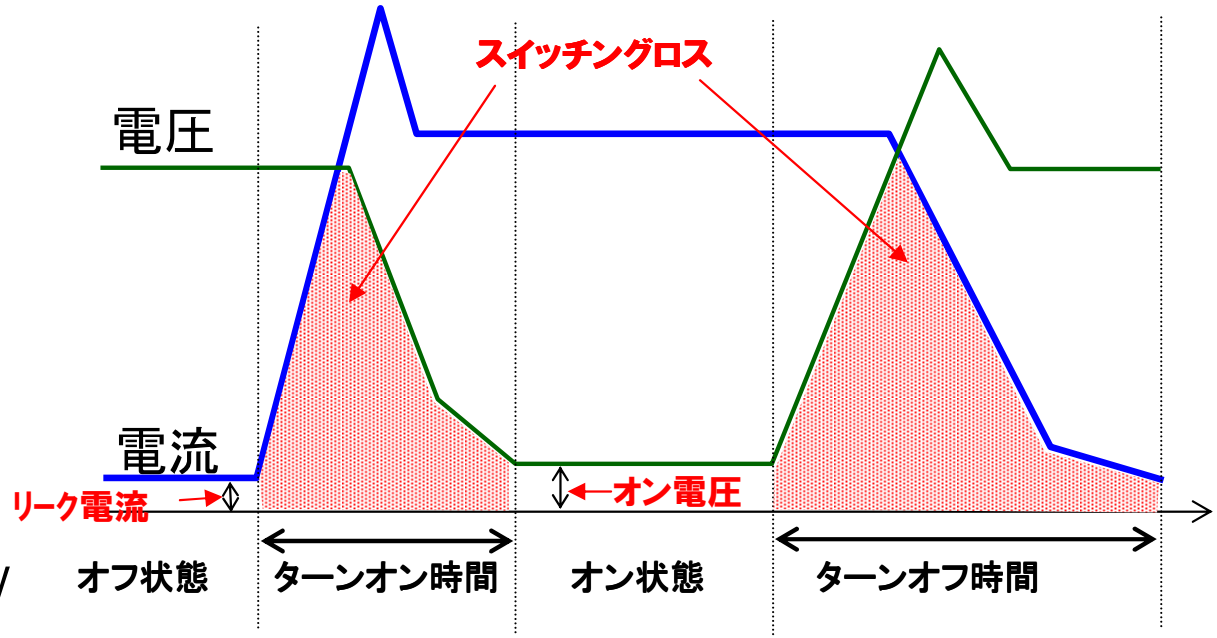
理想特性



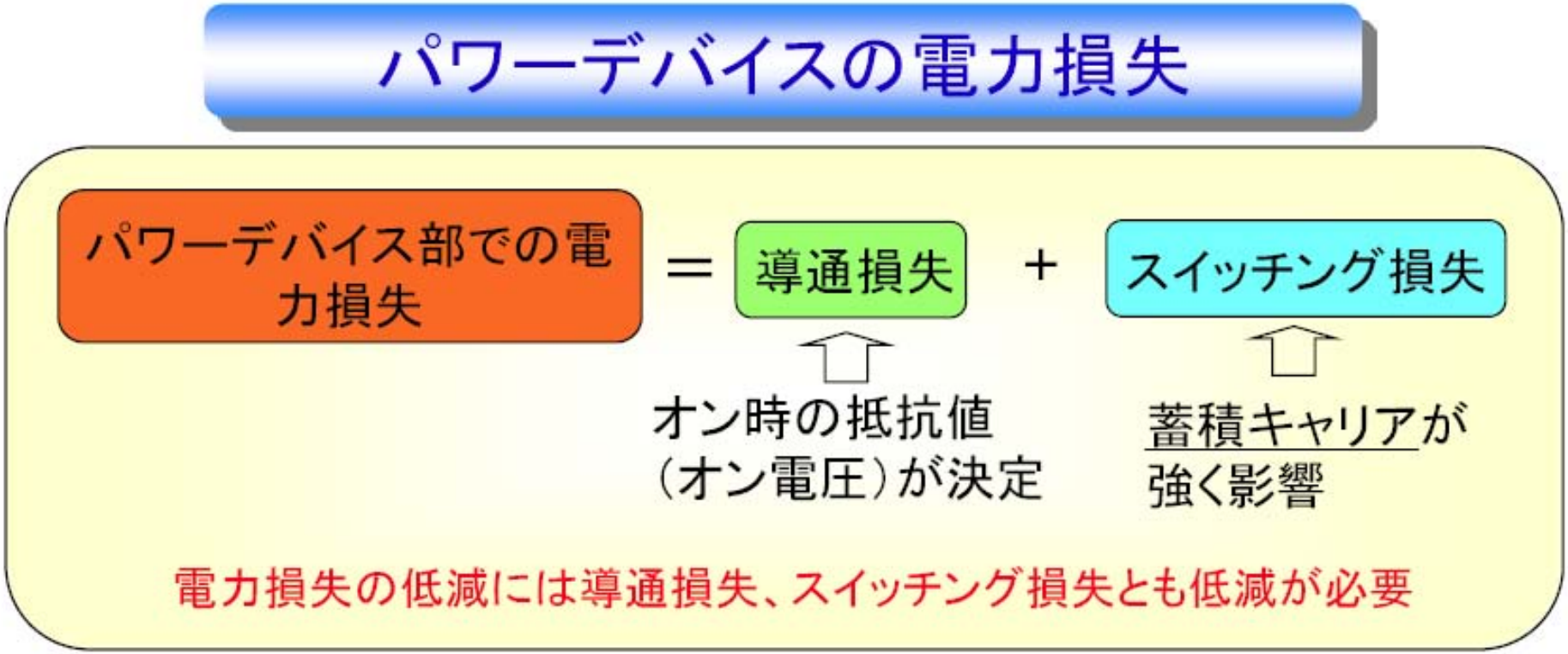




L負荷でのスイッチング波形

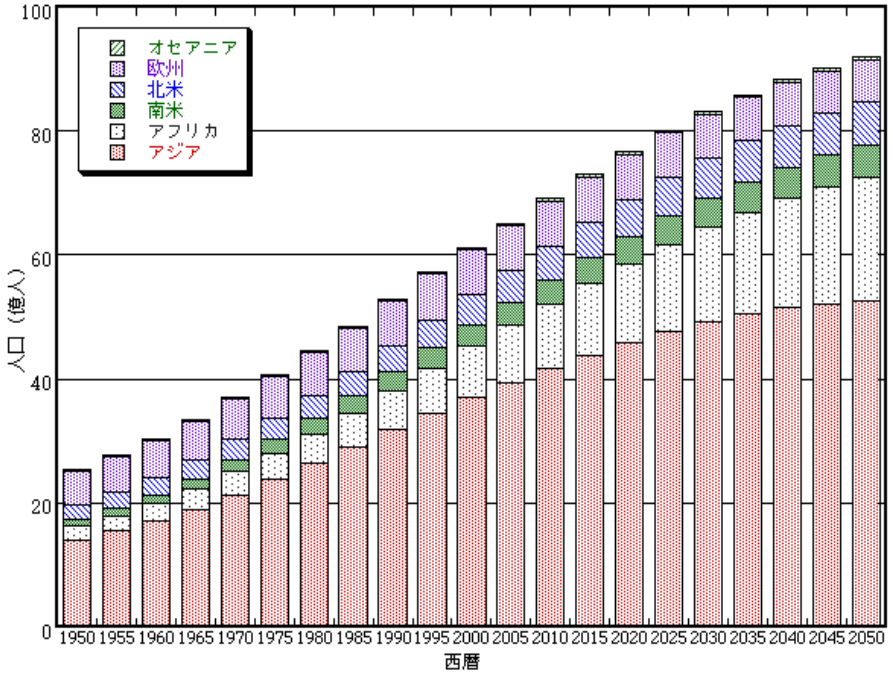


パワー素子開発の歴史は理想スイッチに近づける。。。歴史



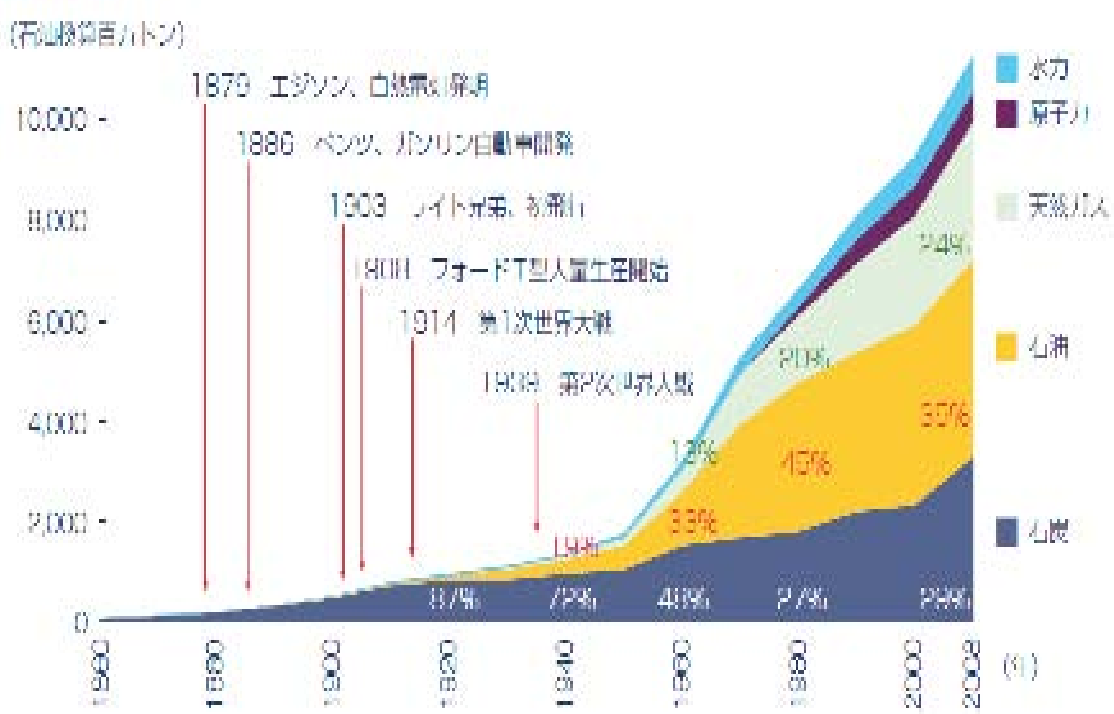
電気に依存する社会

世界人口の推移とエネルギー消費

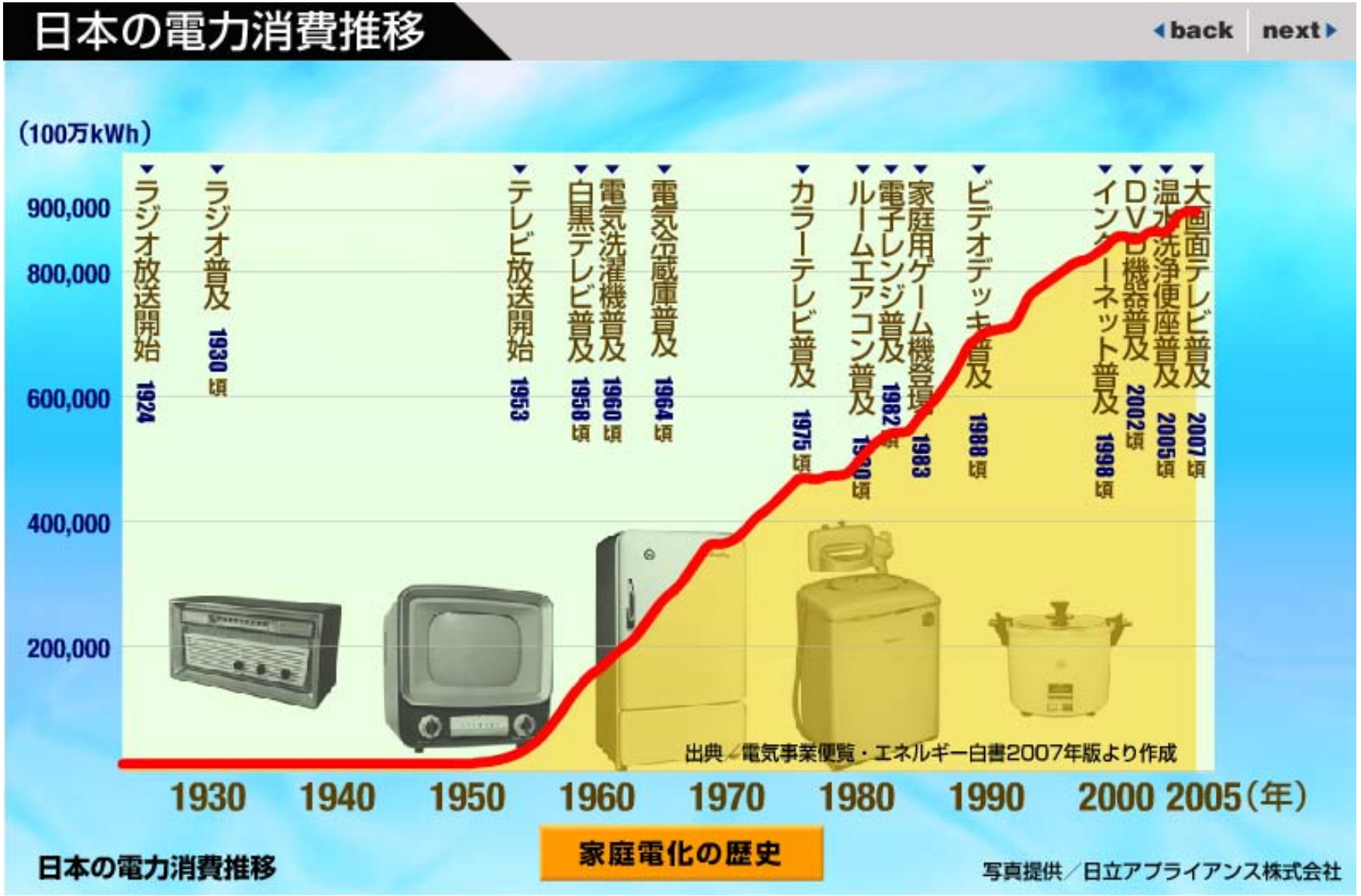


世界人口の推移と見通し

使用データ:総務省＞統計局ホームページ＞世界の統計　第2章 人口

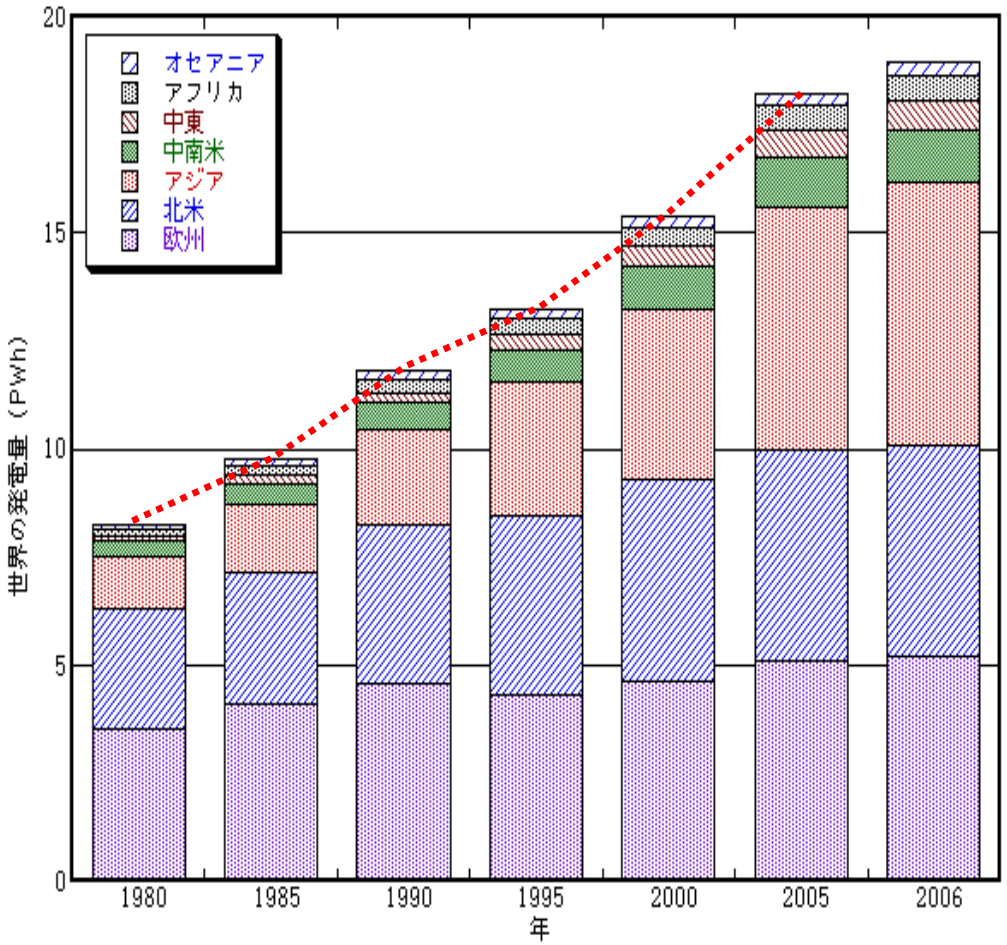


エネルギー白書2010



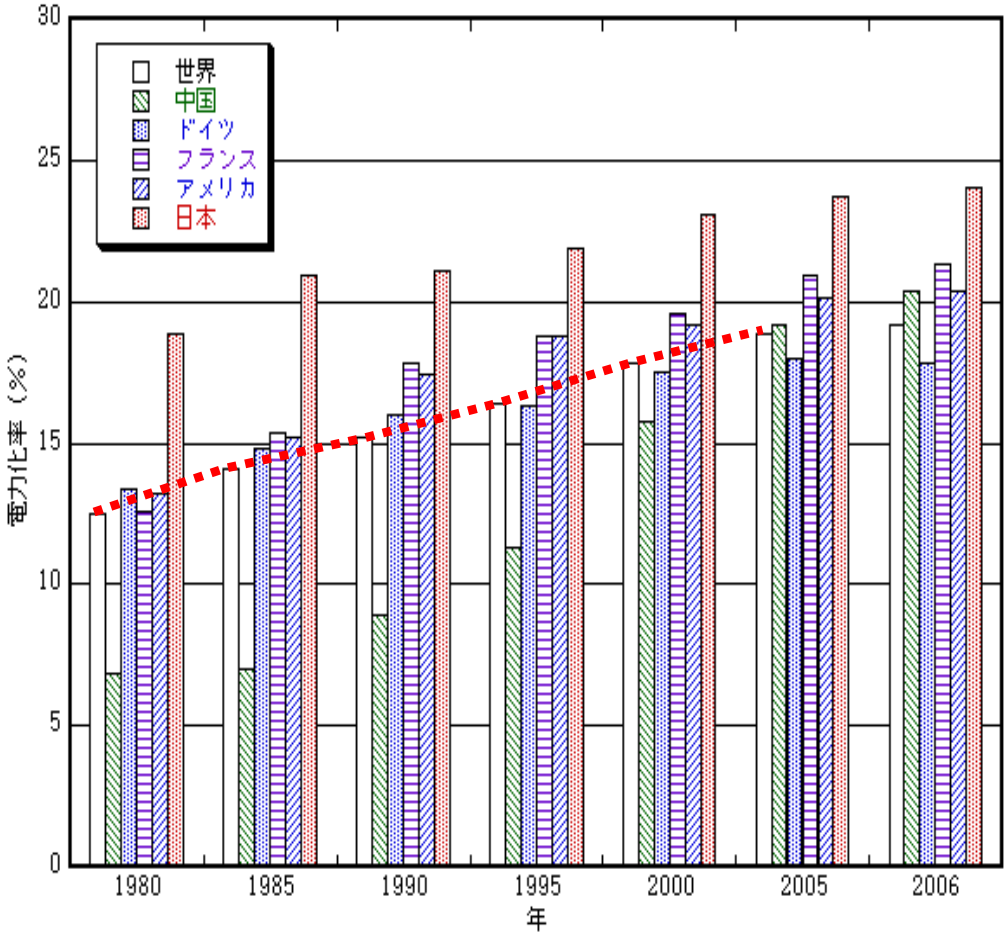
出所：科学技術振興機構 理科ネットワーク

世界の発電電力量



使用データ：EDMC／エネルギー・経済統計要覧（2009年版）

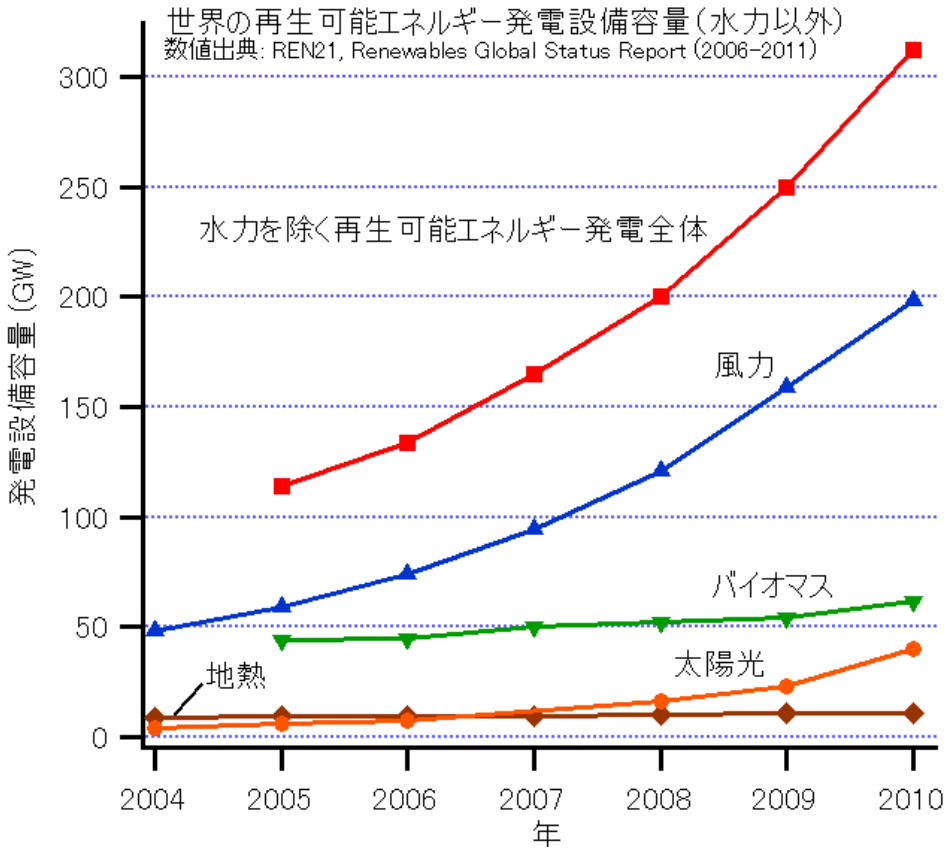
エネルギー消費に占める電力の比率
電力化率

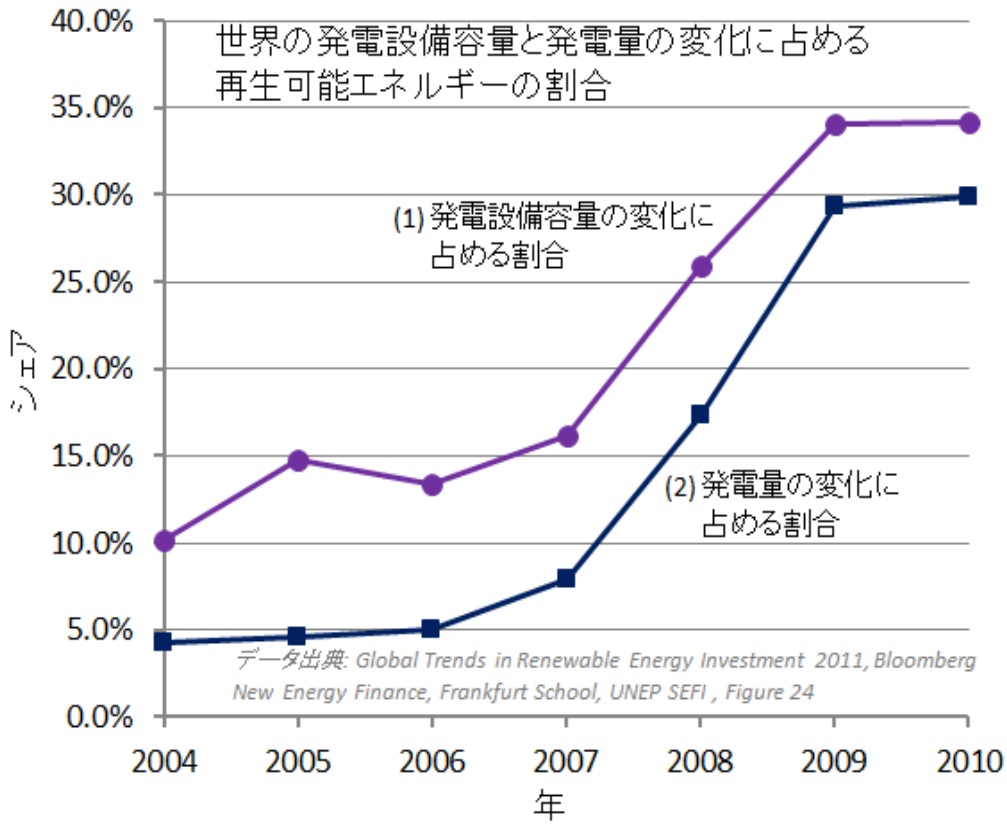


世界と各国の最終エネルギー消費に占める電力の比率（電力化率）
使用データ：EDMC／エネルギー・経済統計要覧（2009年版）

http://www.iae.or.jp/energyinfo/kaisetu.html

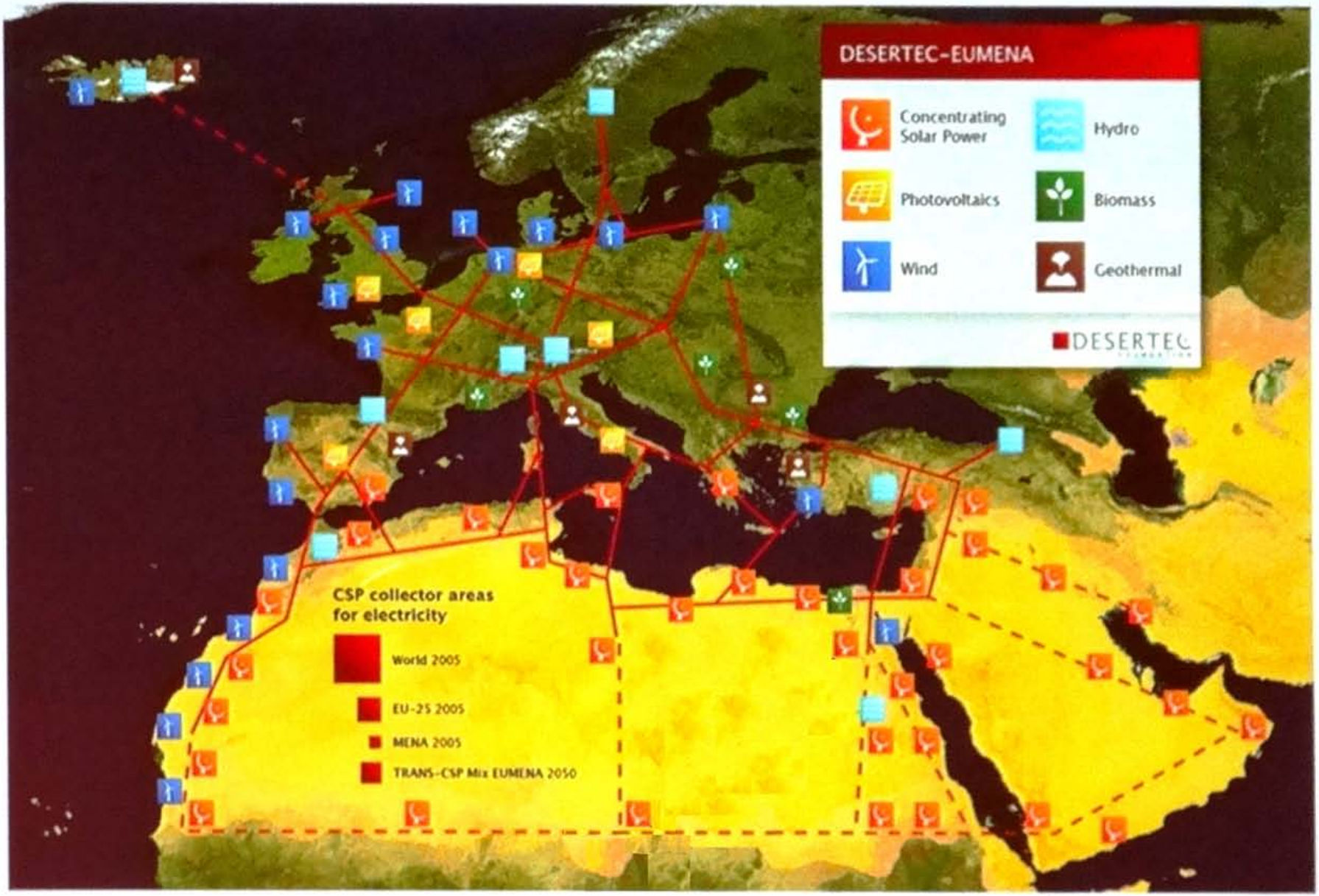
増大する再生可能エネルギー





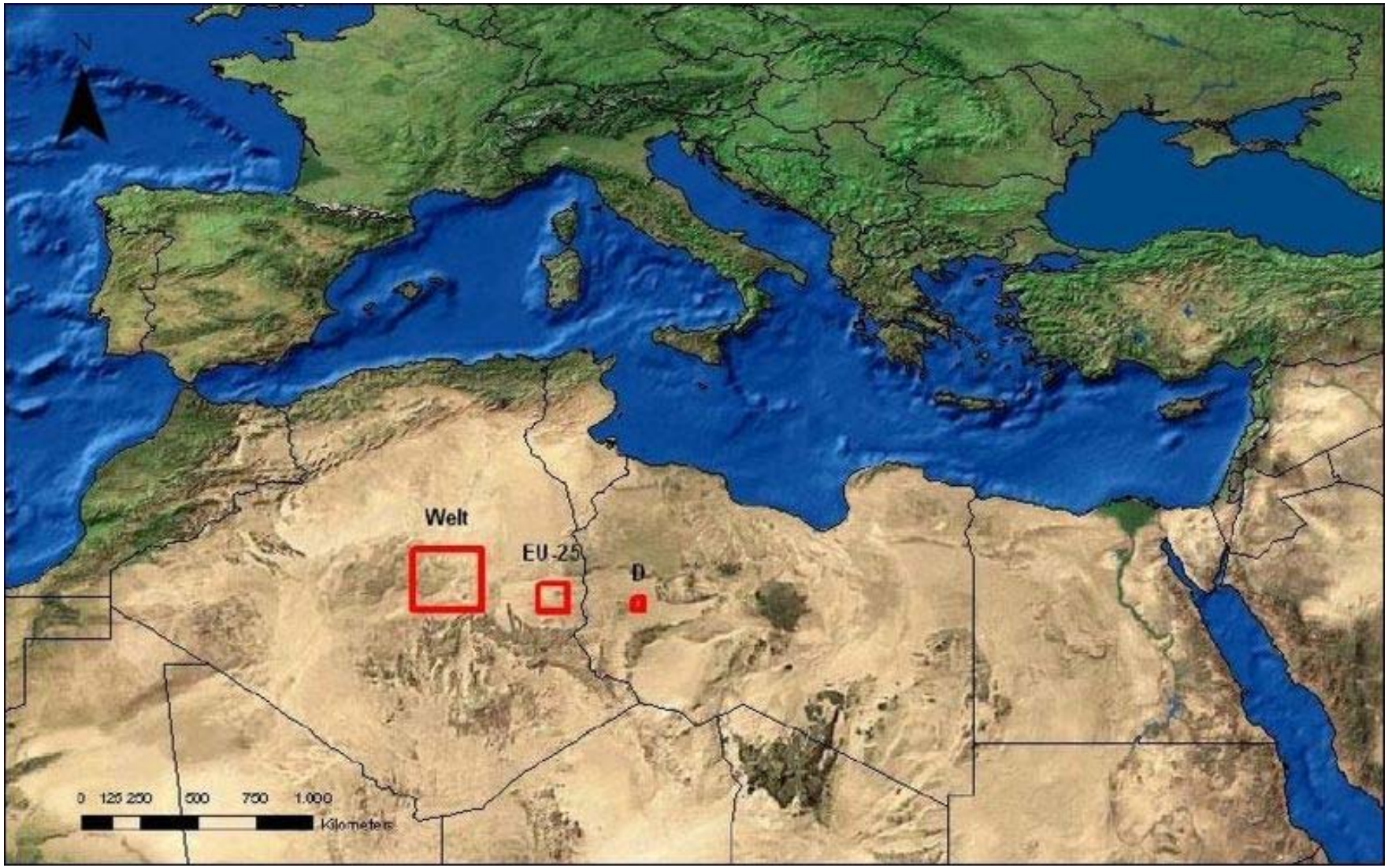
Desertec and Seatec Concept

E.ON Energy Research Center



Source: www.desertec.org

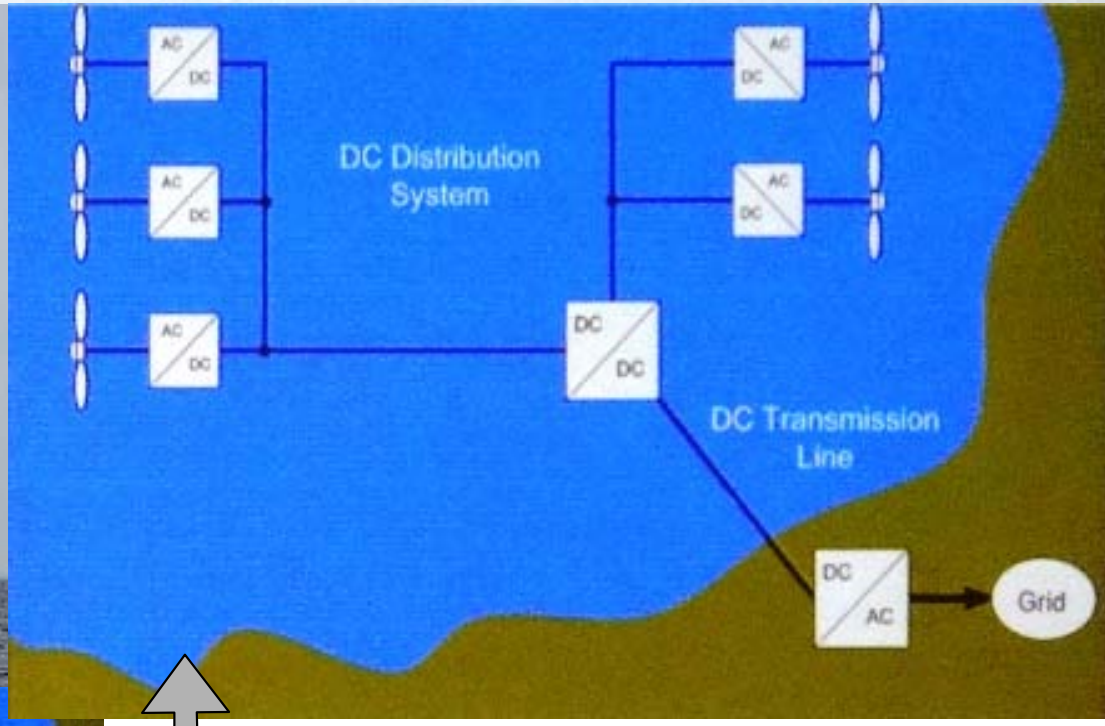
サハラ砂漠の6％の太陽エネルギー発電で全世界がまかなえる!!

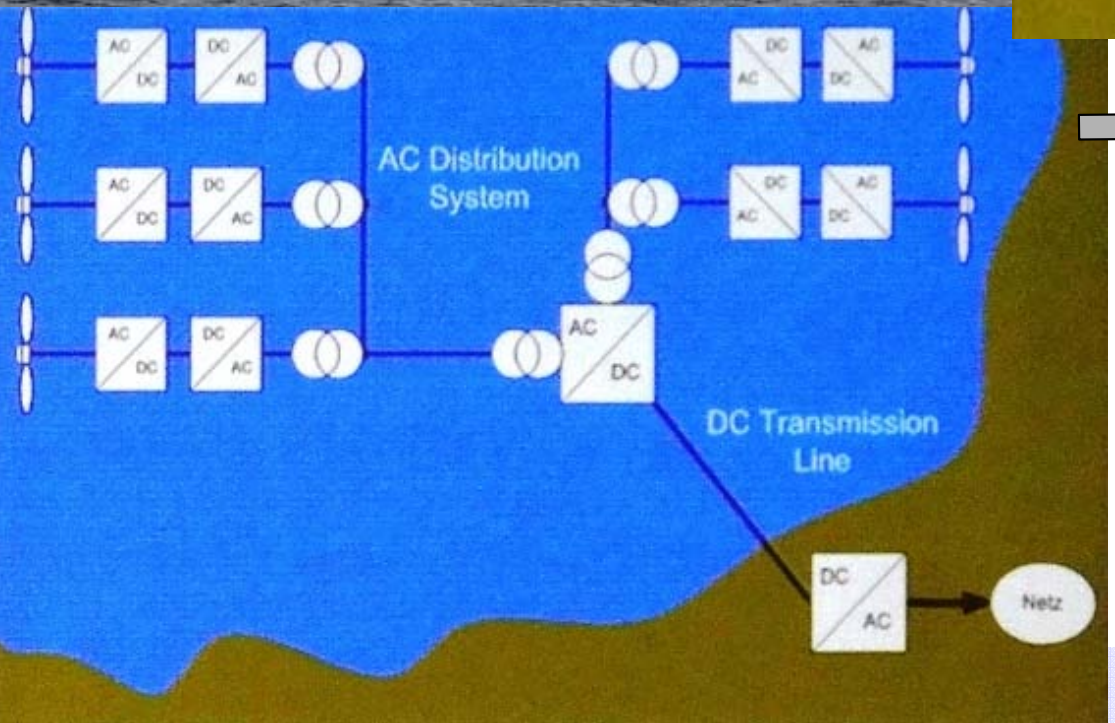


ドイツ、EU25カ国および全世界の需要と等しい電力を太陽エネルギーで発電するのに必要な面積

Grid Topologies for Offshore Wind Farms

E.ON Energy Research Center





電力の選択
ポスト3・11　5

国境またぐ大送電網構想

地域ごとに電力会社が分かれ、互いに電気をほとんど融通しない日本。ここから眺めると、とてつもない動きが欧州で始まった。自然エネルギーをさらに増やすために、国境を越えて電気が行き交う送電網を広げようとしている。

面積も人口も北海道に近い英国スコットランドの自治政府は、自然エネルギーの輸出大国を目指している。2020年までに、国内電力消費量の2倍を発電する目標を掲げた。その半分以上は自然エネルギーから、残りは火力など従来の発電所からつくる。

アレックス・サモンド首席大臣は今年5月にこう宣言した。「欧州大陸の自然エネルギー発電所としての地位を確立する」

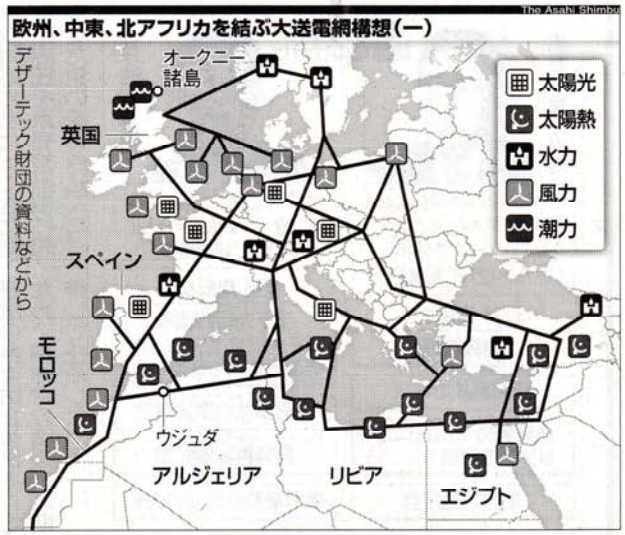
自信を支えるのは、豊富な自然エネルギー資源だ。スコットランドのオークニー諸島は大西洋と北海に挟まれ、行き来する強い潮流に洗われている。

港を出て30分、島と島の間で船長が船を止めた。海面が波立ち、川のように流れている。「今は毎時6キロの速さだ。最大では11キロ、深さ35メートルの海底では28キロにもなる」。海底では、新たな発電機を実験中だ。潮の流れが巨大なプロペラを回し、電気をつくる。

風や潮の流れを、電気を生む資源とみれば、欧州全体の風力と潮力資源量のそれぞれ25%が、スコットランドに集中する。

この資源を電気に換えて外国に売るだけではない。次世代の自然エネルギーと言われる潮力や波力発電の研究開発を支援し、新たな産業に育て上げる。風力や太陽光発電の開発では他国に立ち遅れたため、新分野で巻き返しを図るのだ。

合言葉は「グリーンエネルギーの次は、ブルー（海洋）エネルギーだ」。自然エネルギーの技術開発競争は、次のステージへ移ろうとしている。



北アフリカにも

島国でつくった自然エネルギーの電力を、大陸に送る。英仏間はすでに送電線で結ばれているが、大量に扱うには、特別な送電線（グリッド）が必要だ。

英国、ノルウェー、デンマークなど北海沿岸の約10カ国は昨年、「スーパーグリッド」の建設をめざすことに合意した。各国を高圧の海底直流送電線で結ぶ。

20年ごろの建設を目指し、費用などの調査を始めた。

変動する自然エネルギーを電力消費量に合わせるためには、人工的に制御できるほかの電力で調整する必要がある。日本では主に火力発電で対応しているが、スーパーグリッドが見込むのはノルウェーに多くある水力発電所だ。足りないときに電気を補充してくれる巨大な電池のような存在。関係者は「欧州のジャイアントバッテリー」とよぶ。

英ストラスクライド大学のキース・ベル博士は「国境を越えて調節できれば、欧州でより多くの自然エネルギーが入り、移動も簡単になる」と期待する。

送電線の広がりは北にとどまらない。北アフリカのモロッコ北東部のウジュダで昨年、巨大な太陽熱発電所が動き始めた。湾曲した反射鏡で熱を集め、蒸気をつくってタービンを回す。

「デザーテック計画」の一環で、アルジェリアや中東にも太陽熱発電所を増やし、50年までに欧州の電力の15%を供給する構想だ。すでに、スペインとの間には2本の送電線があり、今後強化する。

きっかけはドイツが03年に始めた太陽エネルギーの調査。北アフリカと中東には「強い日差しがあり、潜在力は世界全体の電力需要をはるかに超える」ことがわかった。フランスもよく似た「トランスグリーン構想」を進めていた。いまはドイツが発電系を、フランスが送電系を担う。

欧州の「大送電網構想」は、バラ色ではない。スーパーグリッドの建設費は3000億㌦（3兆4千億円）とも、それ以上ともいわれる。デザーテック計画は、経済レベルが異なる地域を巻き込むため、お互いの利益になるかどうか。

「欧州が安い値段で土地を借りて施設をつくり、電力を持っていく。我々にはどんな価値がもたらされるのか。交渉が必要だ」（モロッコの電力業界関係者）という声も漏れる。中東の政情不安も影を落とす。

生かされぬ技術

スーパーグリッドを支える技術の先進例は日本にある。1979年にできた北海道と青森県を高圧直流で結ぶ海底送電線「北本連系線」だ。北海道の風力資源をもっと開発し、本州に送ることも可能だった。だが、今回のような原発の大規模停止以外ではほとんど使われてこなかった。

デザーテック計画を推進するドイツ企業中心のデザーテック財団は、福島第一原発事故を受けて声明を出した。「中国やモンゴルにも太陽熱発電の適地は多い。安全で二酸化炭素を出さない電気を広い地域へ供給できる。世界の人口が増え続けるなか、十分なエネルギーと温暖化が止まった気候を必要としている」

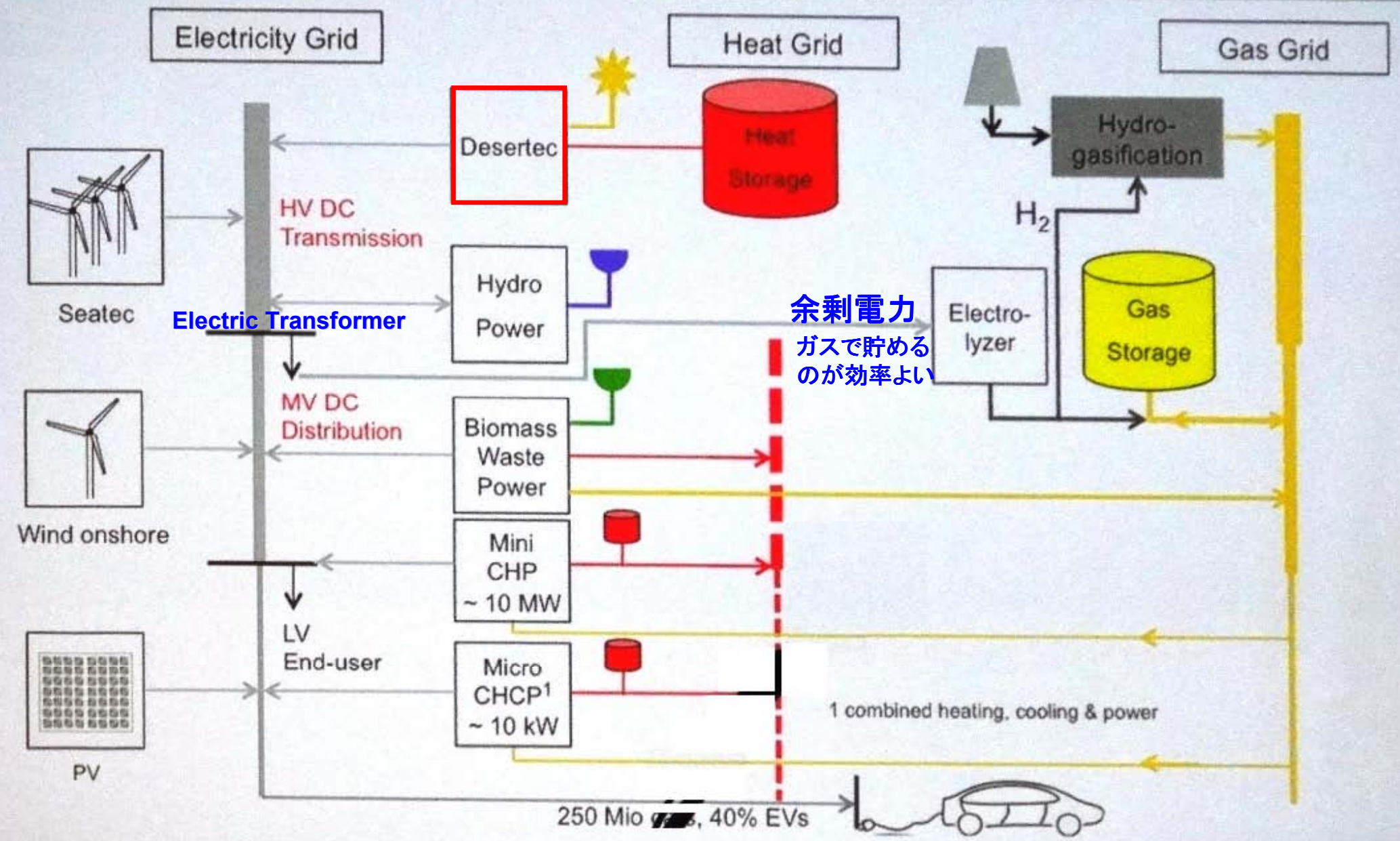
日本の電力政策も、こんな大胆な発想で考えたい。

（編集委員・竹内敬二、有田哲文）

▼国際面＝「エコ電気」選べるドイツ

Future electrical grid – ultra large capacity REN
Concept for EU27 + Norway and Switzerland

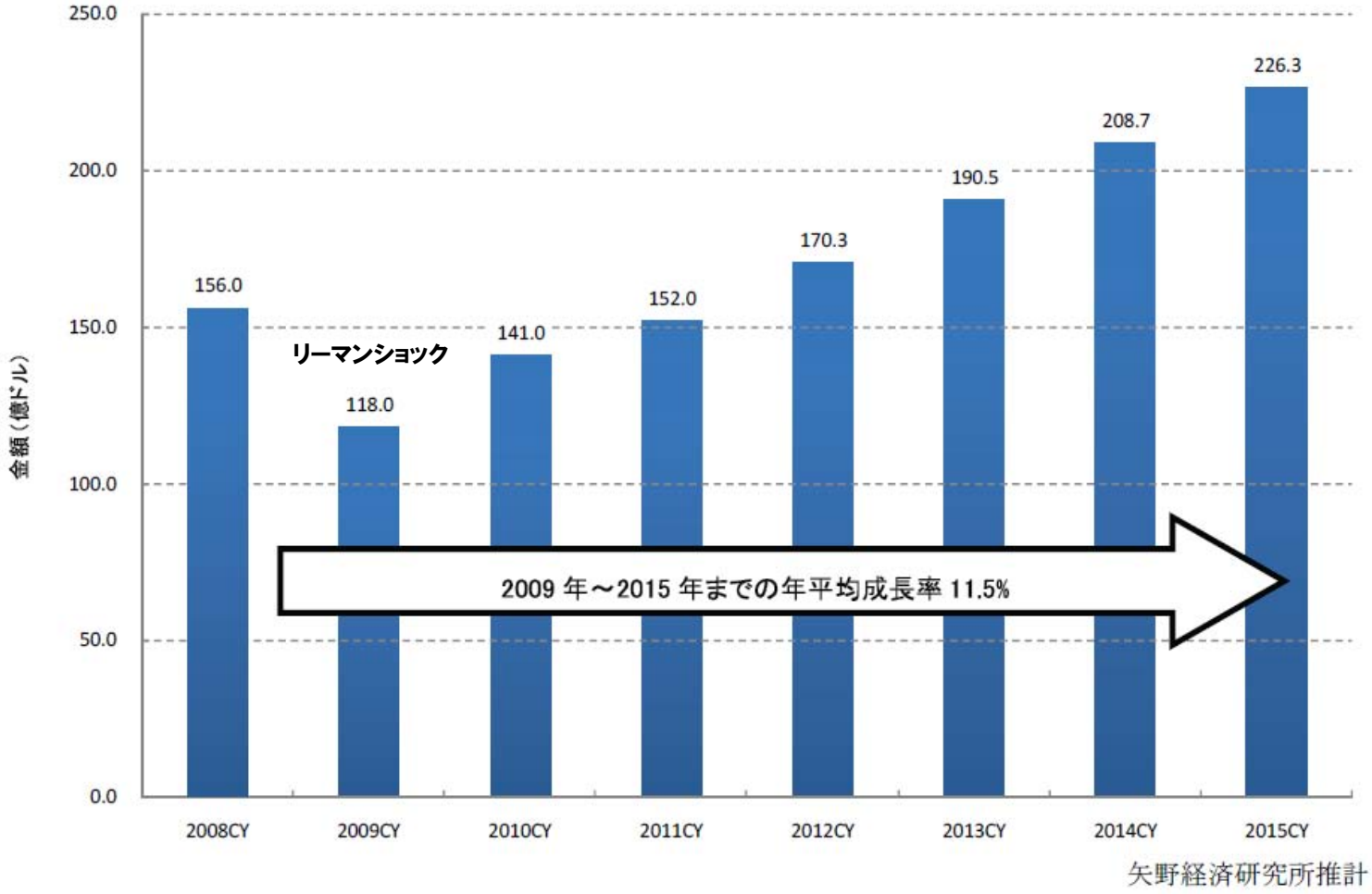
E.ON Energy Research Center



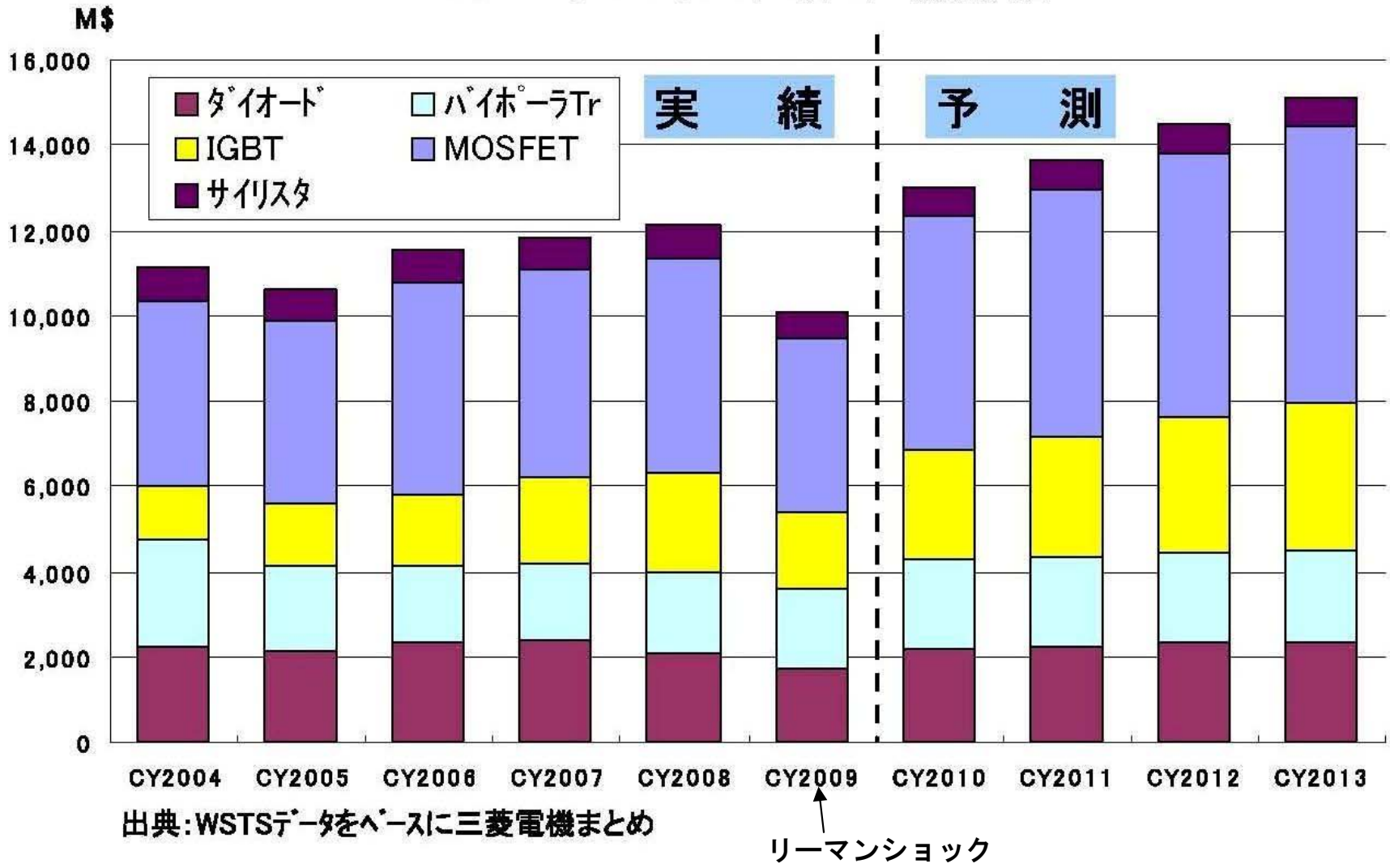
CHP：Combined Heat Power（コージェネレーション）

パワーデバイスの市場

パワーデバイスの成長見通し

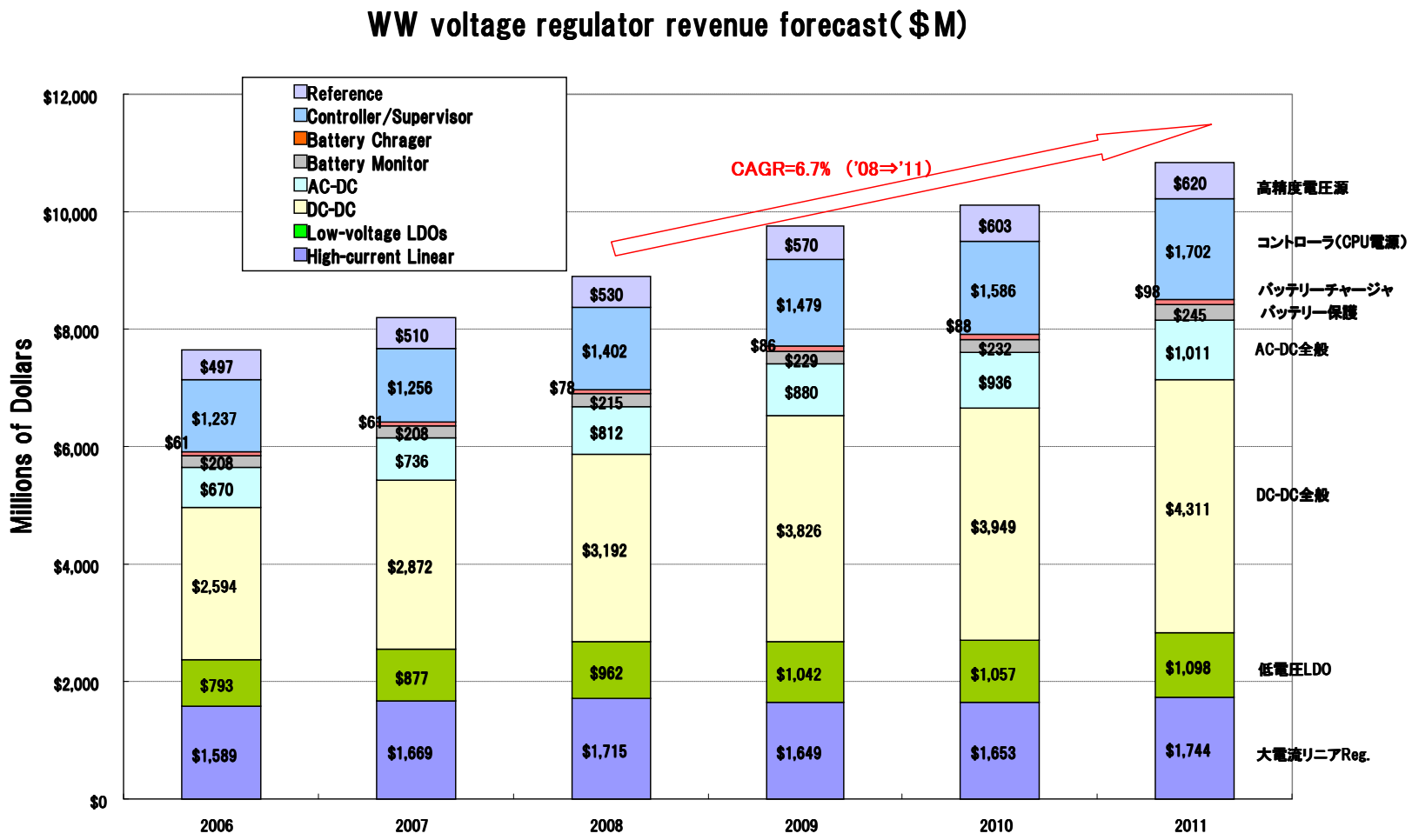


パワーデバイス世界市場規模



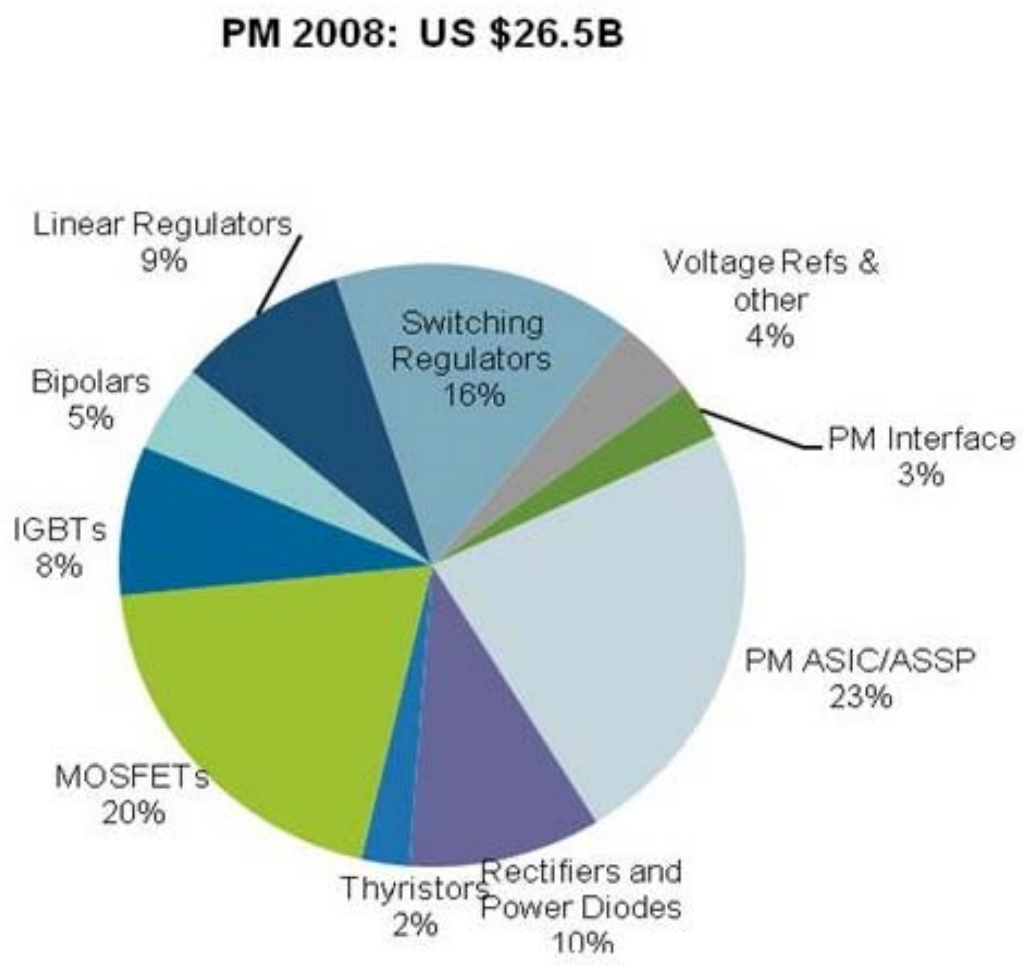
電源半導体の世界市場

1兆円@2010年



出典:Gartner

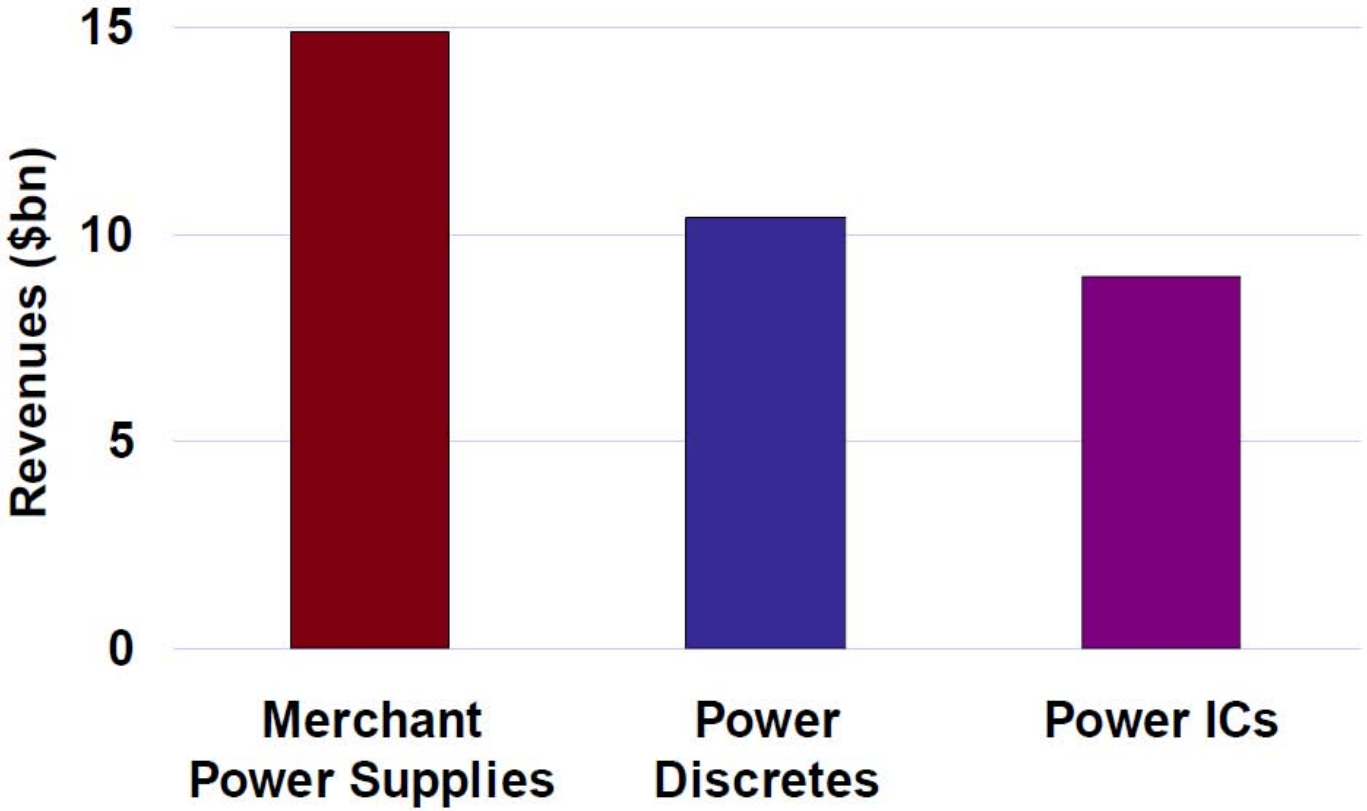
広義のパワーデバイス市場は２兆円超え



パワー・マネージメント半導体の2008年市場規模

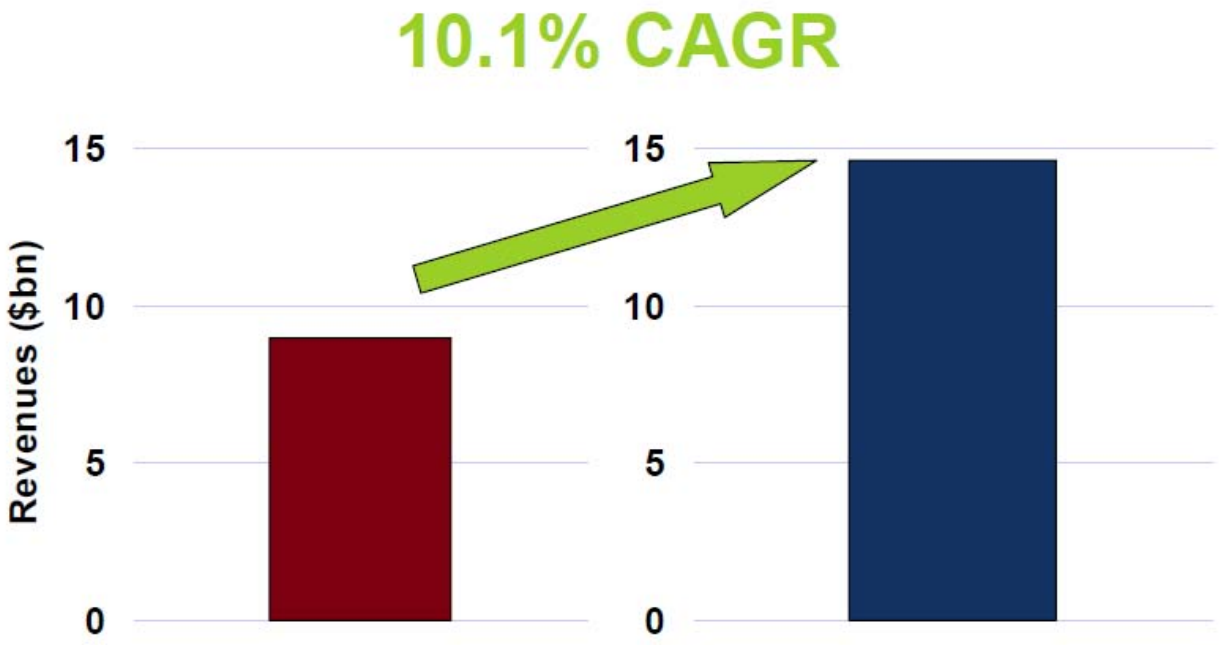
出所：南川 明＝アイサプライ・ジャパン

電源のマーケットサイズ



出所:IMS Research

パワーICの成長見込み

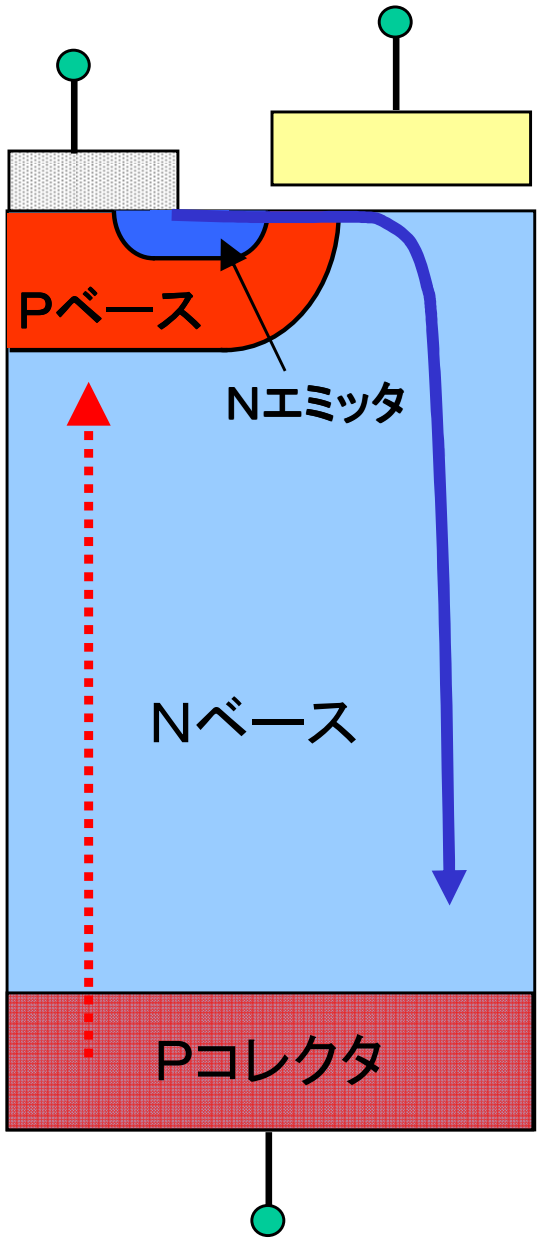


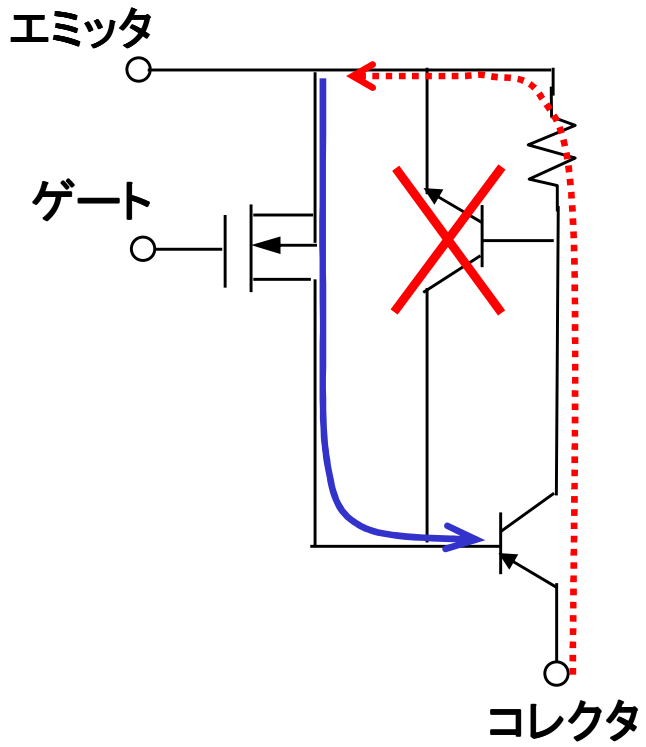
- Ongoing move to IBA & DPA
- Increasing voltage rails and variety of voltages
- Demand for higher value products & higher ASPs

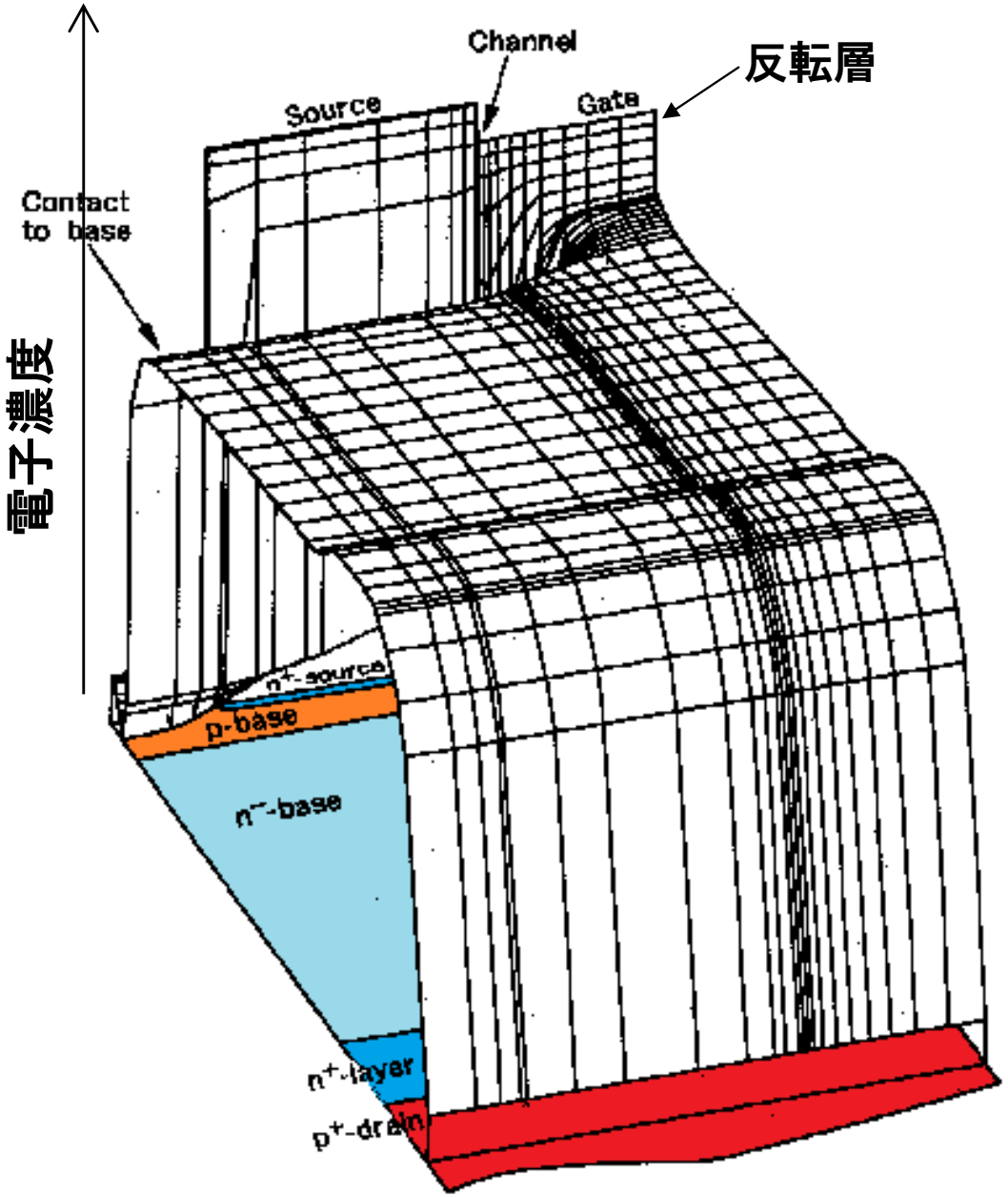
出所:IMS Research

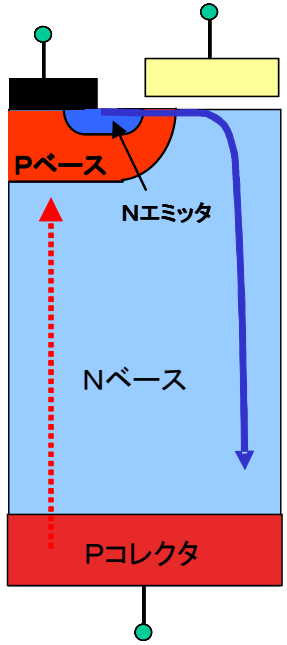

－－IGBTとは－－

IGBT(絶縁ゲートバイポーラTr)の動作



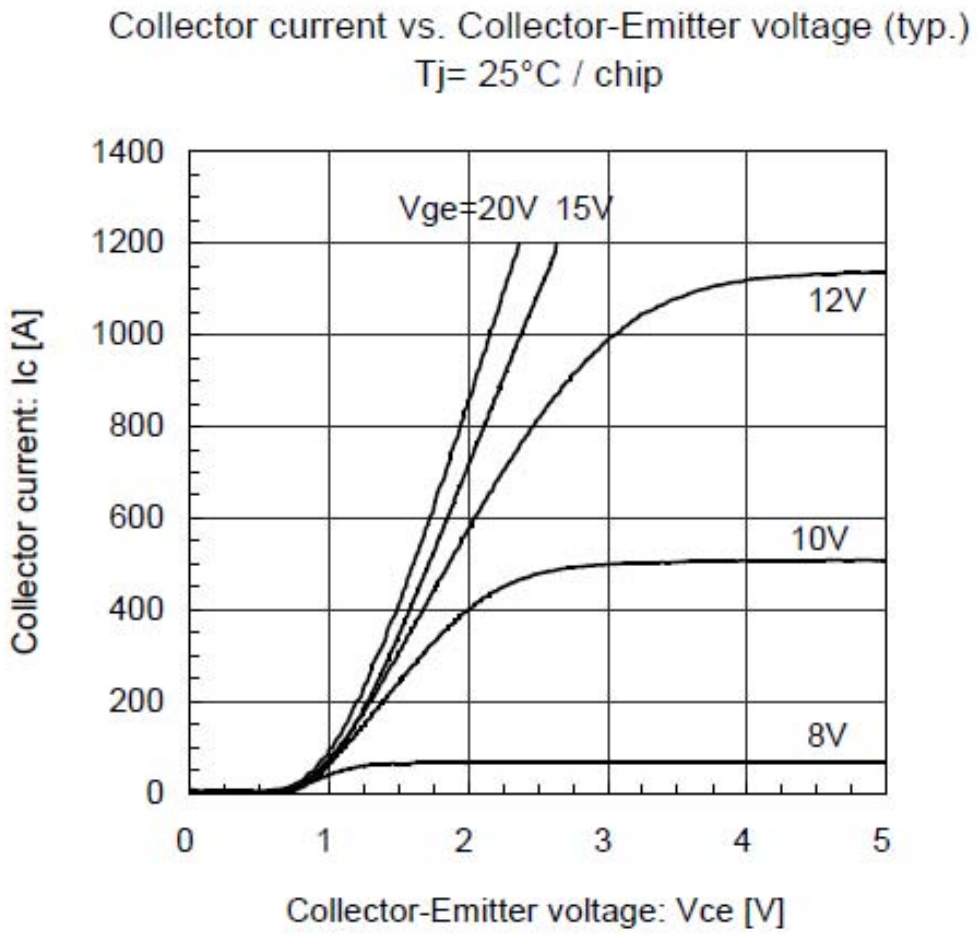






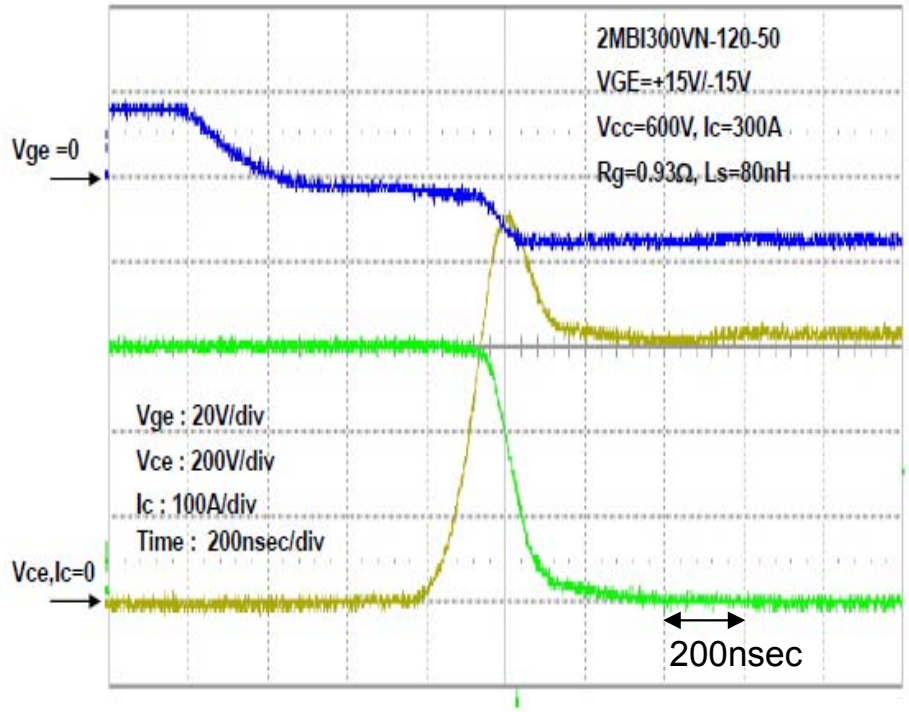
Nベースにキャリアが蓄積、伝導度変調により抵抗が下がる!!

1200V 600A素子の電流電圧特性



2MB1600VN-120-50

600V 300Aのターンオフ特性



2MBI300VN-120-50(1200V/300A) ターンオフ電流・電圧波形

1982年のBaligaの論文!!!

THE INSULATED GATE RECTIFIER (IGR):

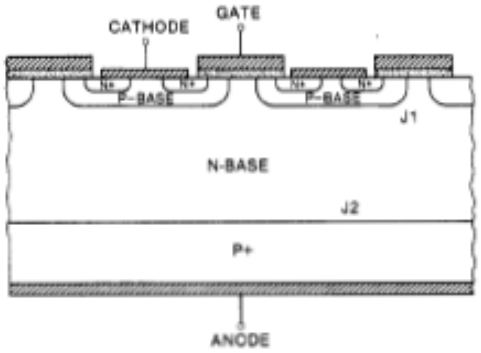
A NEW POWER SWITCHING DEVICE

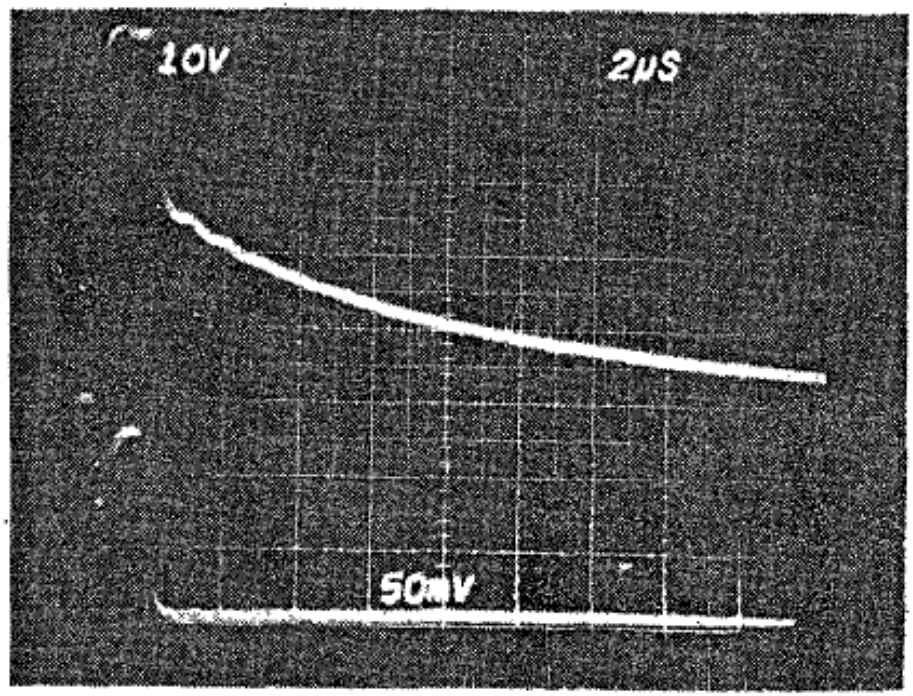
B.J. Baliga, M.S. Adler, P.V. Gray, R.P. Love

General Electric Company
Corporate Research and Development Center
Schenectady, NY

Nathan Zommer

Intersil Inc.
Cupertino, CA





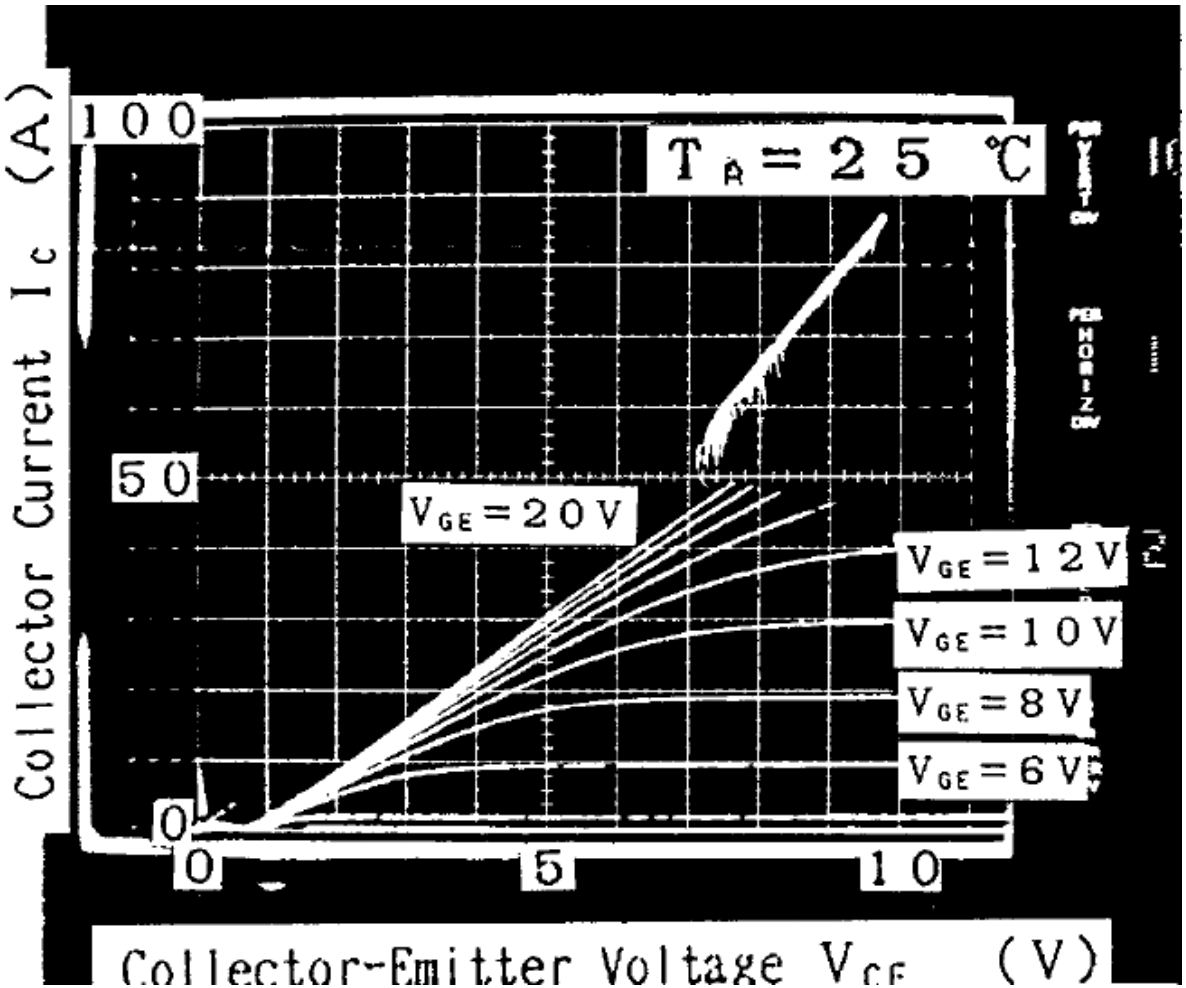
スイッチング時間 >18μsec

新規性はあるが、
「何故このような遅い素子を発表するのか」
「良くこのような素子を実証して見せたものだ」という驚き

米国の多くのメーカが開発に参入するがラッチアップの問題を解決できない!!

１９８３年

ＩＧＢＴは壊れやすく、ラッチアップを防ぐことは不可能に近いと考えられた!!!



高い目標を掲げる!!!

その１：
1983年 ラッチアップしない
ＩＧＢＴの開発

Non-Latch-Up IGBTができてしまうと、 1984年

実現したNon-Latch-up IGBTは
思った以上に良い素性を持っていた!!!

Non-Latch-Up 1200V 75A Bipolar-Mode MOSFET with Large ASO

Akio Nakagawa, Hiromichi Ohashi, Mamoru Kurata
Hoshihiro Yamaguchi, Kiminori Watanabe

Toshiba R&D Center
1 Komukai Toshibacho, Saiwaiku
Kawasaki, Japan

In 1984 ICSSDM, Kobe, we already reported the development of 1200V, 75A bipolar-mode MOSFETs(BIFET[1], or called IGT, COMFET [2,3]), which could turn-off 75Amps drain current with 1000V applied drain voltage at the elevated temperature, 125 C(see Fig. 1).

This paper presents improved BIFETs with non-latch-up structure as well as a large ASO. Figure 2 shows a cross section of a new BIFET. A part of the source layer is periodically eliminated, providing a low resistance bypass for holes to the source electrode without biasing the source-base junction. The maximum drain current was substantially limited by the channel pinch-off effect before ti reached the increased latch-up current level, which was attained by the vertical BIFET structure and the optimized source pattern. Thus, the latch-up mode was not observed under any driving conditions unless gate voltage exceeds 20V.

It was found that the latch-up current density J_L depends gate width L_G through the following equation [1]:

$J_L = V_{bi}/(L_G R_b)$ ----- L_G: gate width; V_{bi}:built-in voltage for sourcebase junct.;
R_b:channel to source electrode p-base resistance for unit channel width.

New BIFET structure provides a lower R_b, which enables to use a larger L_G than the original BIFET with attaining a high latch-up current density. Thus, new BIFETs exhibit low forward voltage regardless of reduced channel width.

BIFETs should have a sufficiently large ASO so that BIFETs can be used as a key switching device in place of bipolar transistors in a power application system. If the external load is caused to be short-circuited due to system failure, drain current is limited only by the device resistance itself with the drain voltage being the same as the external power supply voltage. The device should dissipate a large heat until a protection circuit works, reducing gate voltage to zero. Figure 3 shows the measured 25 μsec forward conduction ASO limit. The improved BIFETs can sustain more than 65Amps drain current with 600V forward voltage drop and 20V gate voltage during 25 μsec, which is sufficient for sensing and device protection. Measured switching ASO is also included in Fig. 3. Voltage and current density product exceeds $3X10^5 VA/cm^2$, which suggests avalanche multiplication for a failure cause.

Neither snubber nor clamp circuit is necessary for the inductive load switching. Figure 4 shows 48Amps switching waveforms, wherein voltage surge is clamped by the device itself. The electrical characteristics for the improved BIFETs are given in Table. BIFETs are now ready for applications.

References [1] A. Nakagawa et al, in Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp.309-312

[2] M.F. Chang et al, 1983 IEEE IEDM Tech. Digest, pp. 83

[3] A.M. Goodman et al, 1983 IEEE IEDM Tech. Digest, pp. 79

CH2099-0/84/0000-0860 $1.00 © 1984 IEDM

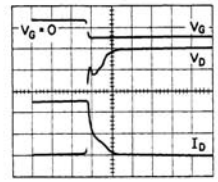


Fig.1 Typical turn-off waveforms for a BIFET. I_D:30A/Div, V_D:200V/Div, Time:2μsec/Div, Temp:125°C.

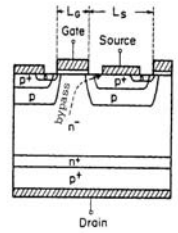


Fig.2 A cross section of a new BIFET

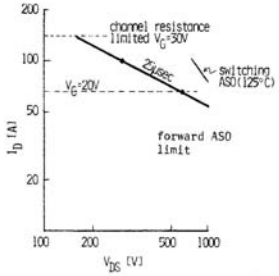


Fig.3 Measured 25μsec forward conduction ASO limit, which actually means device destraction.

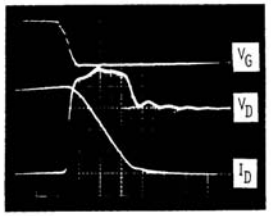


Fig.4 Typical inductive load switching waveform. I_D:12A/Div, V_D:200V/Div, Time:0.5μsec/Div.

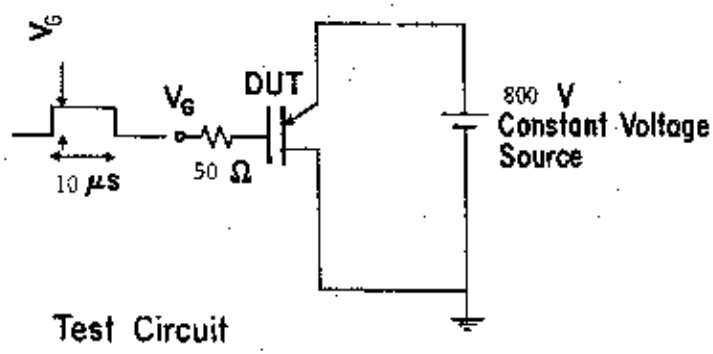
Breakdown voltage	1200V	Turn-off delay time	0.3μsec
Continuous drain current	20A	fall-time	1.6μsec
Forward voltage drop	3V(20A)	Device active area	$20mm^2$
Turn-on time	120nsec	Maximum turn-off current (V_D=1000V, Temp=125°C)	more than 75A

Table electrical characteristics

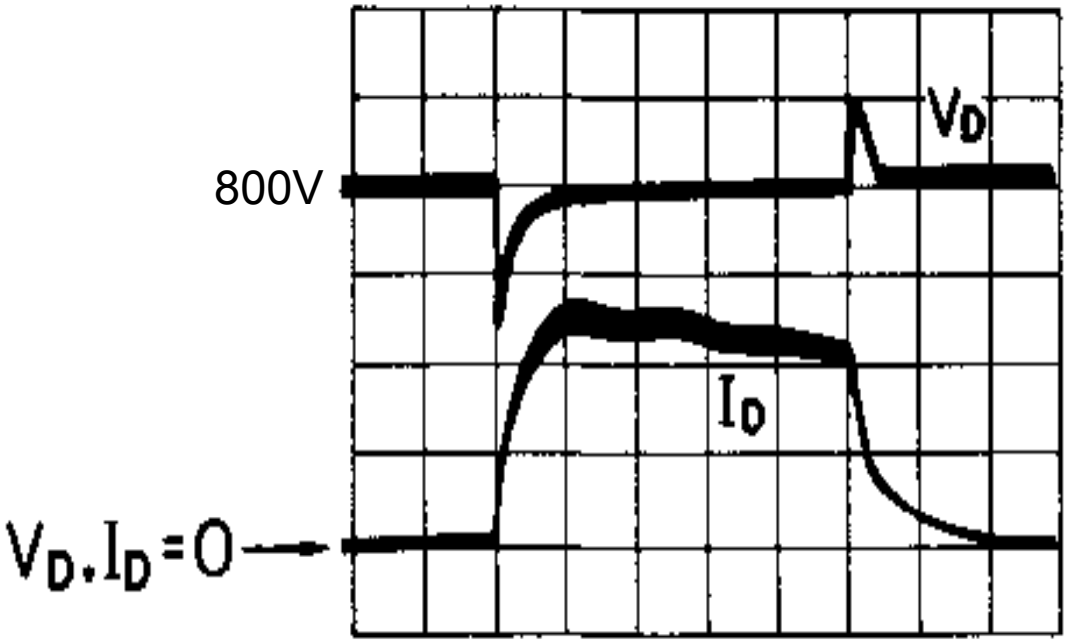
ノンラッチアップIGBT最初の論文
IEDM Late News 1984年12月

IGBTが負荷短絡に耐えられるとは誰も考えなかった!!!

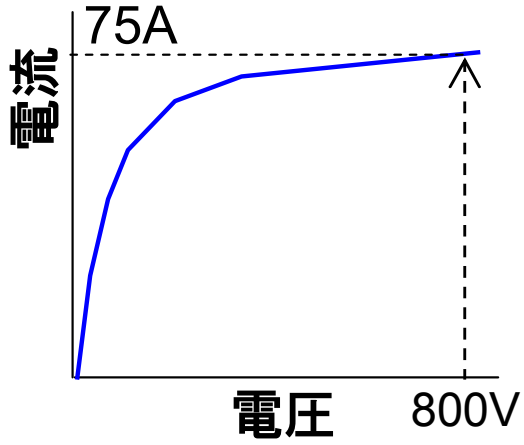
『IGBTは非常に強い素子』と評価が180度転換



Test Circuit

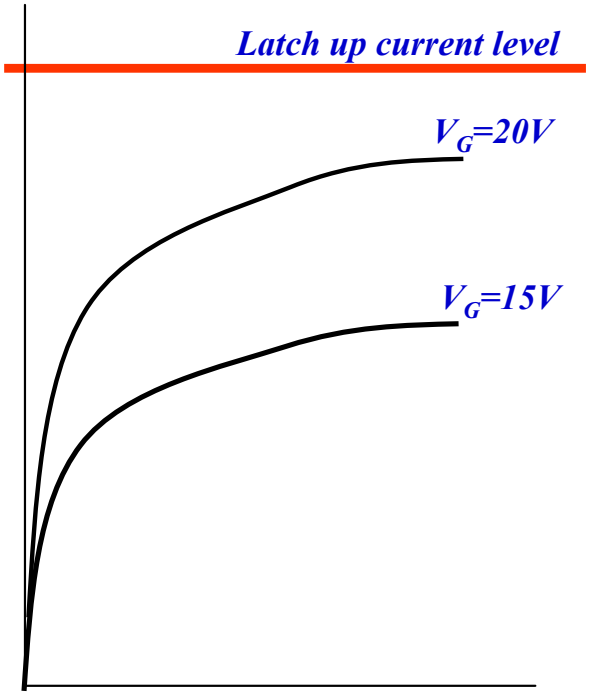


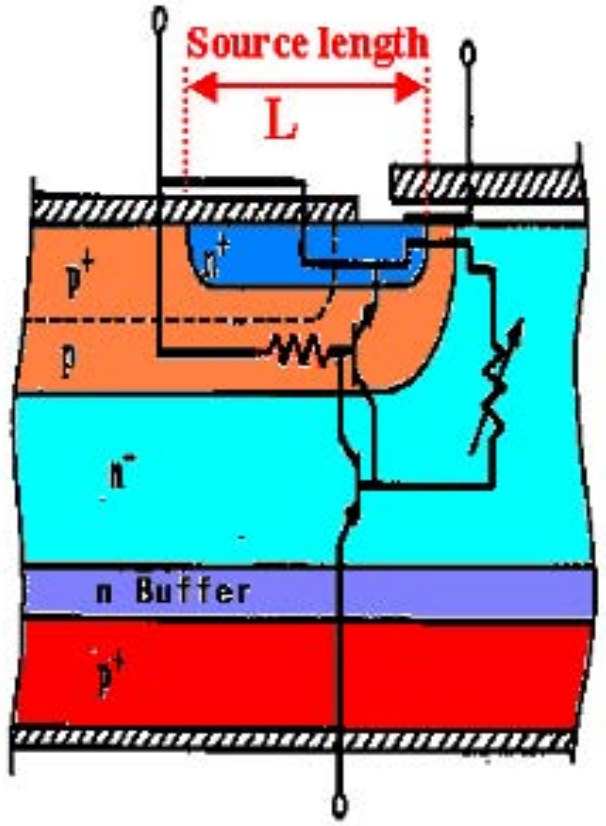
I_D : 30A/Div
V_D : 200V/Div
Time : 2μs/Div



Non-latch-Up Bipolar-Mode MOSFETの概念

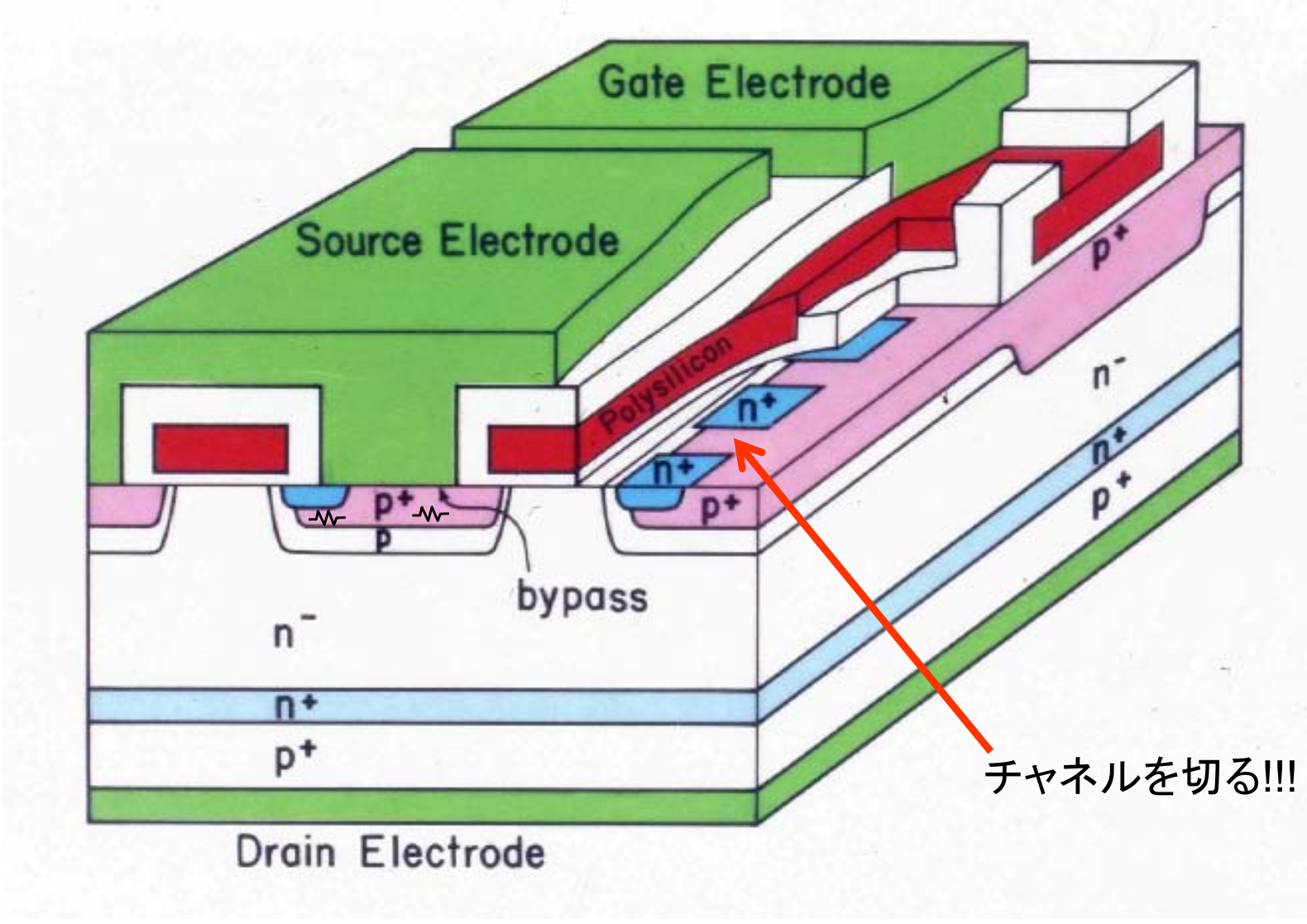
飽和電流(@ V_G =20V) < ラッチアップ電流



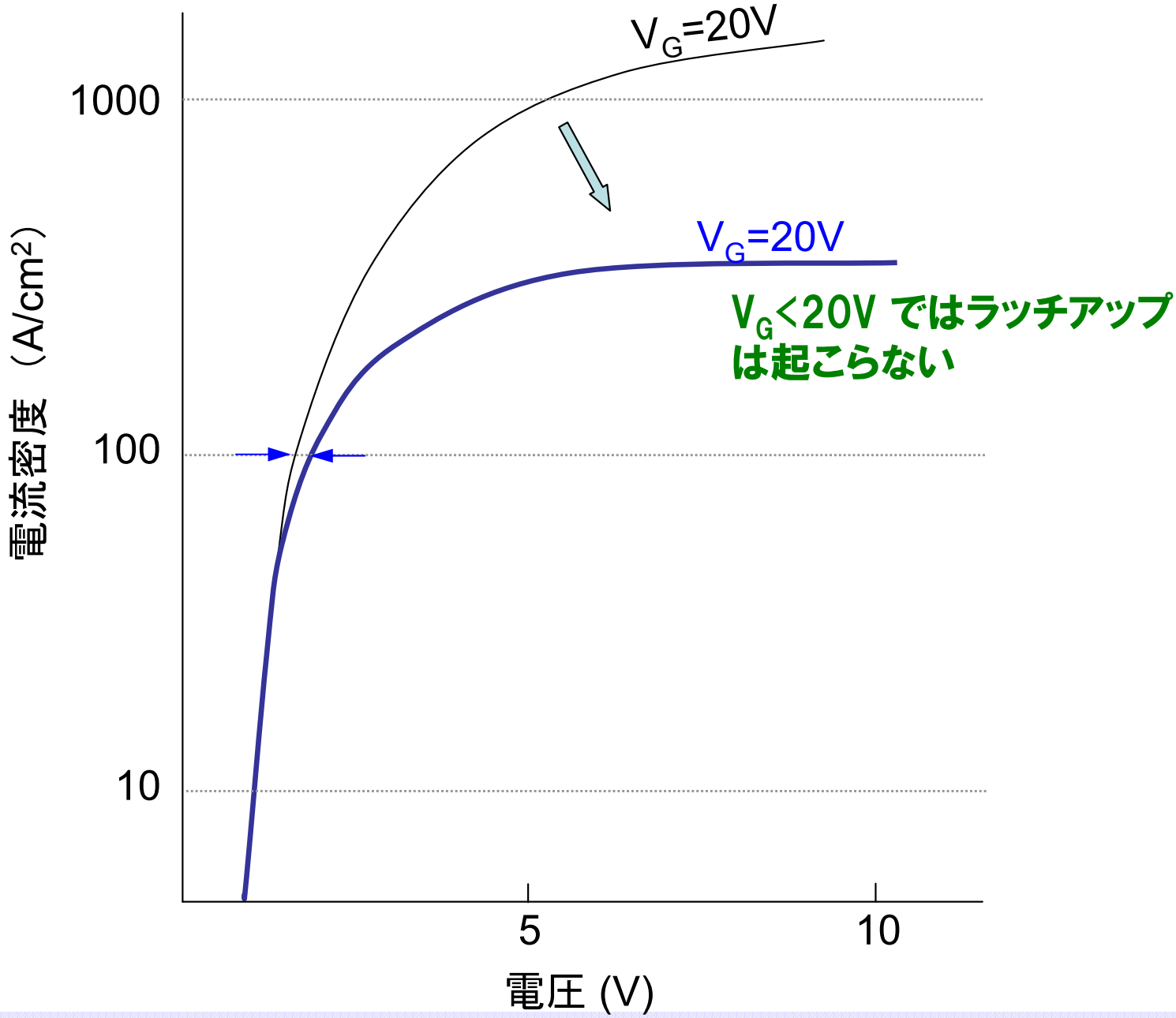


Non-Latch-Up IGBT構造

Hole Bypass： チャネルを切って低抵抗の正孔バイパスを形成

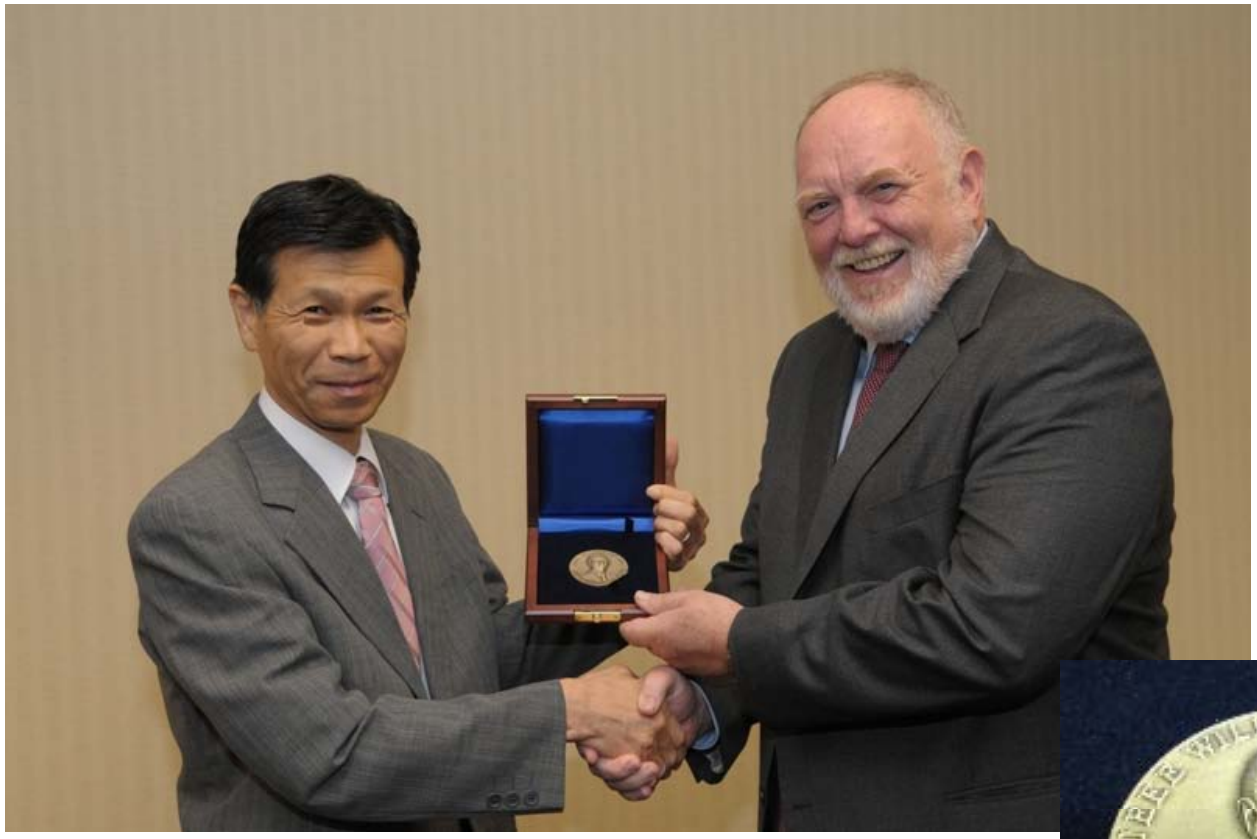


V－I 特性の変化


V_G=20V
1000
V_G=20V
V_G<20V ではラッチアップ
は起こらない
100
10
電流密度（A/cm²）
5
10
電圧 (V)

2010年　9月 IEEE William E. Newell Power Electronics Award

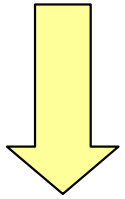
For development of non-latch-up IGBTs



高い目標 その２：

無謀とも言う
べき課題

BTrはIGBT化できた!
次はGTOのMOSゲート化



POST-GTO PJの発足@１９８９年

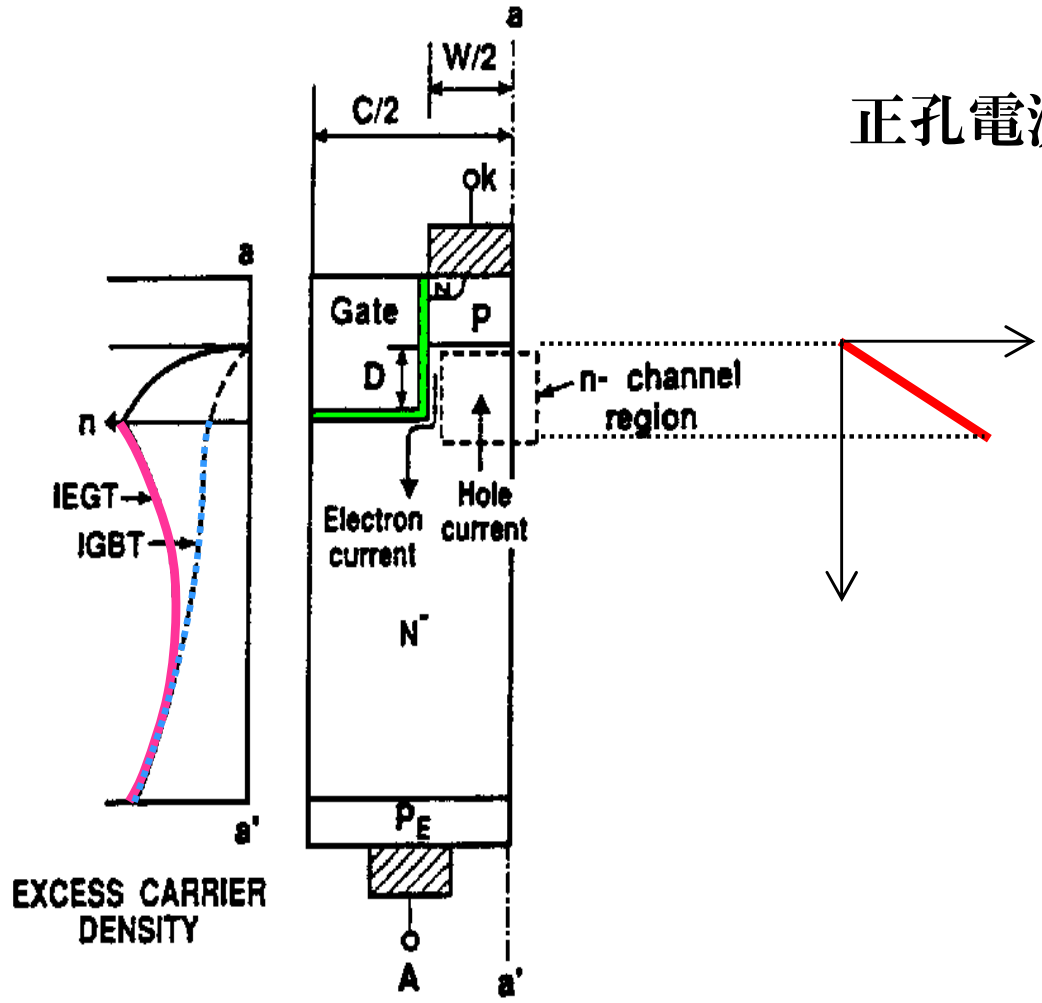
IGBTはオン電圧が高いという先入観から
MOSGTOを試作・検討するが全くうまく行かない!!!

---　行き詰る　---

デバイスシミュレータによる試行錯誤の検討!!!

1990年 Injection Enhanced IGBT（IE効果）の発見

デバイスシミュレータでの予測　(特許出願1991、発表1993)



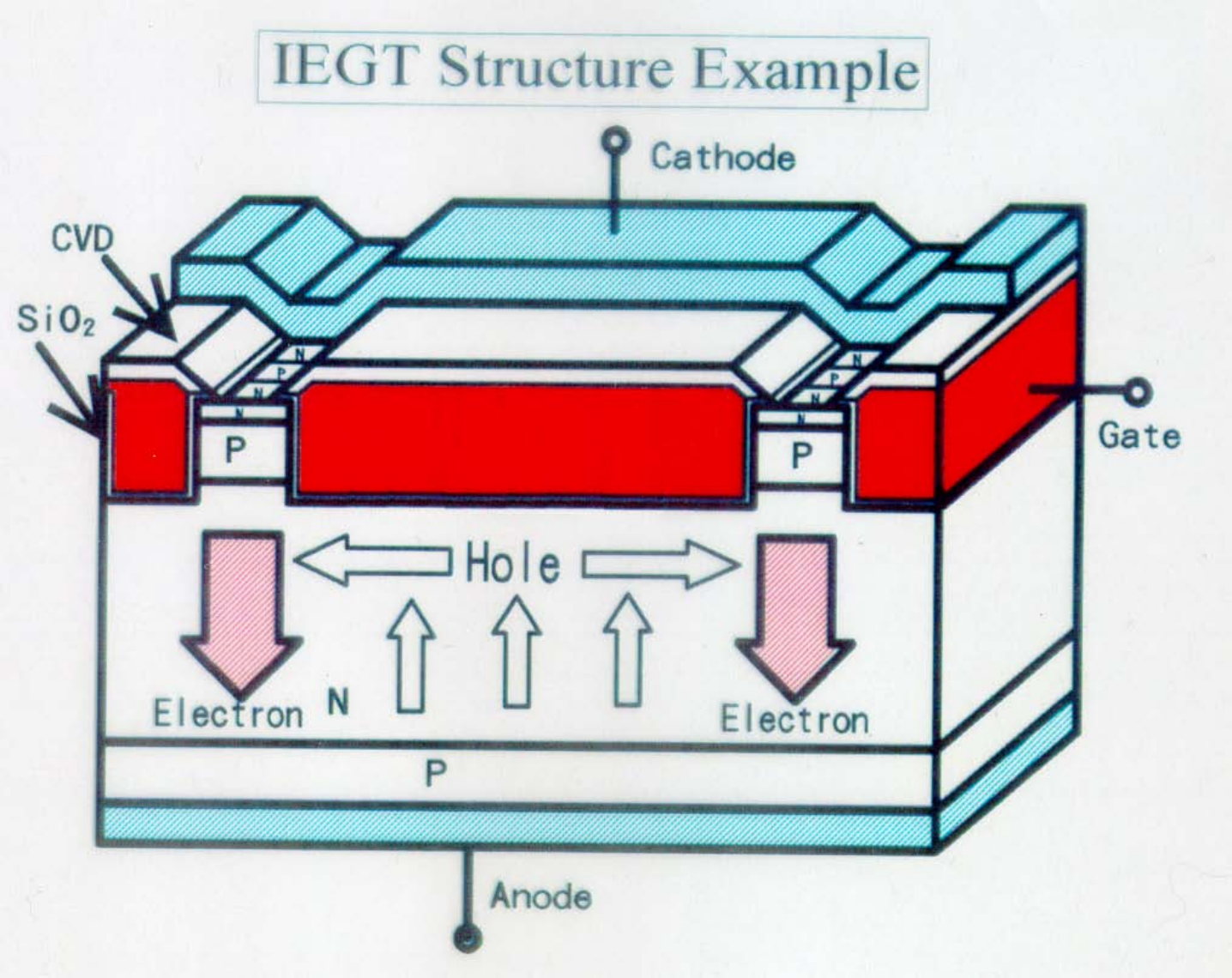
$$\text{正孔電流 } J_p = qD_p \frac{\partial p}{\partial x}$$

キャリアの勾配で
正孔を蓄積

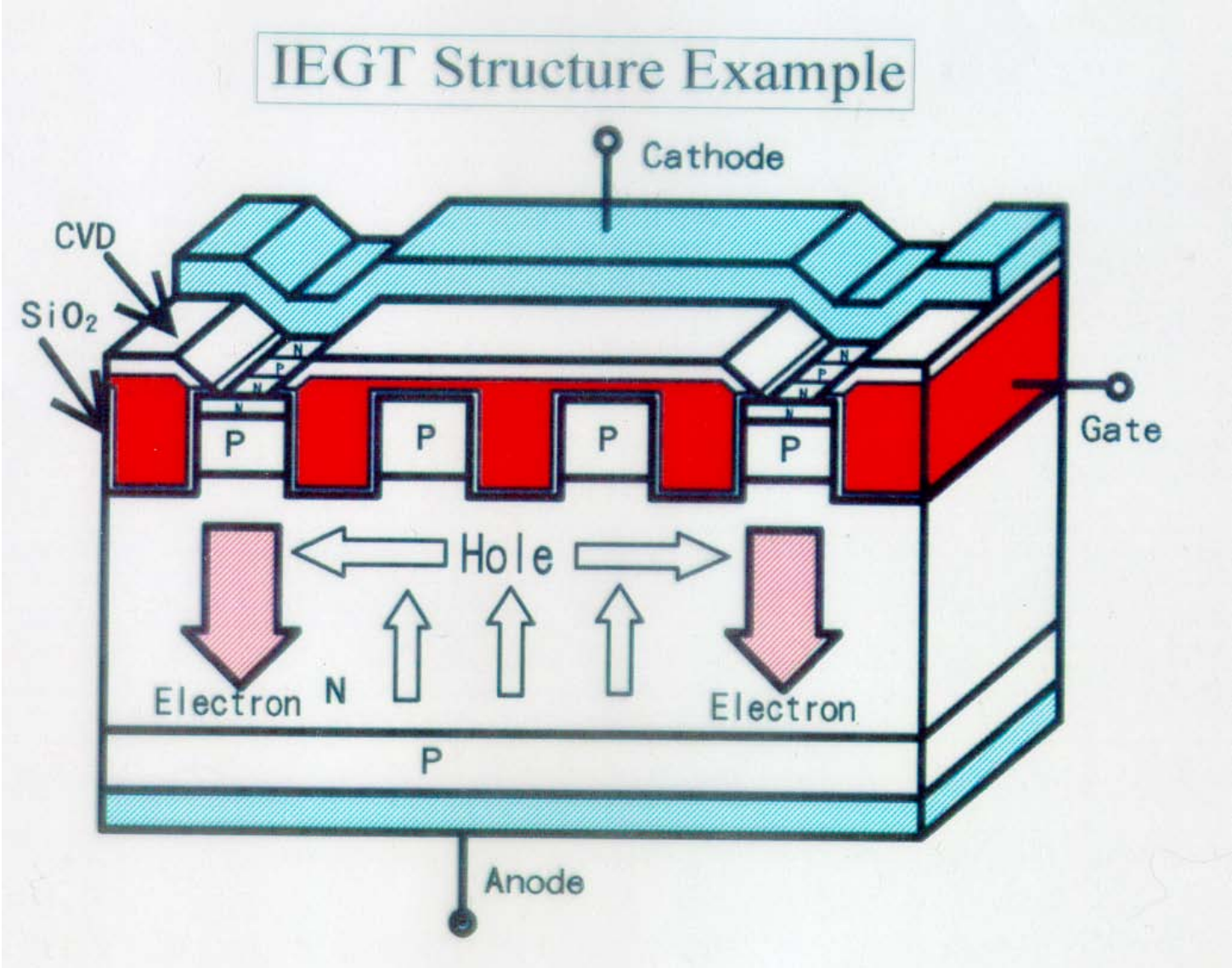
サイリスタのキャリア分布を実現

北川他, 1993 IEEE IEDM Tech. Digest, pp.679

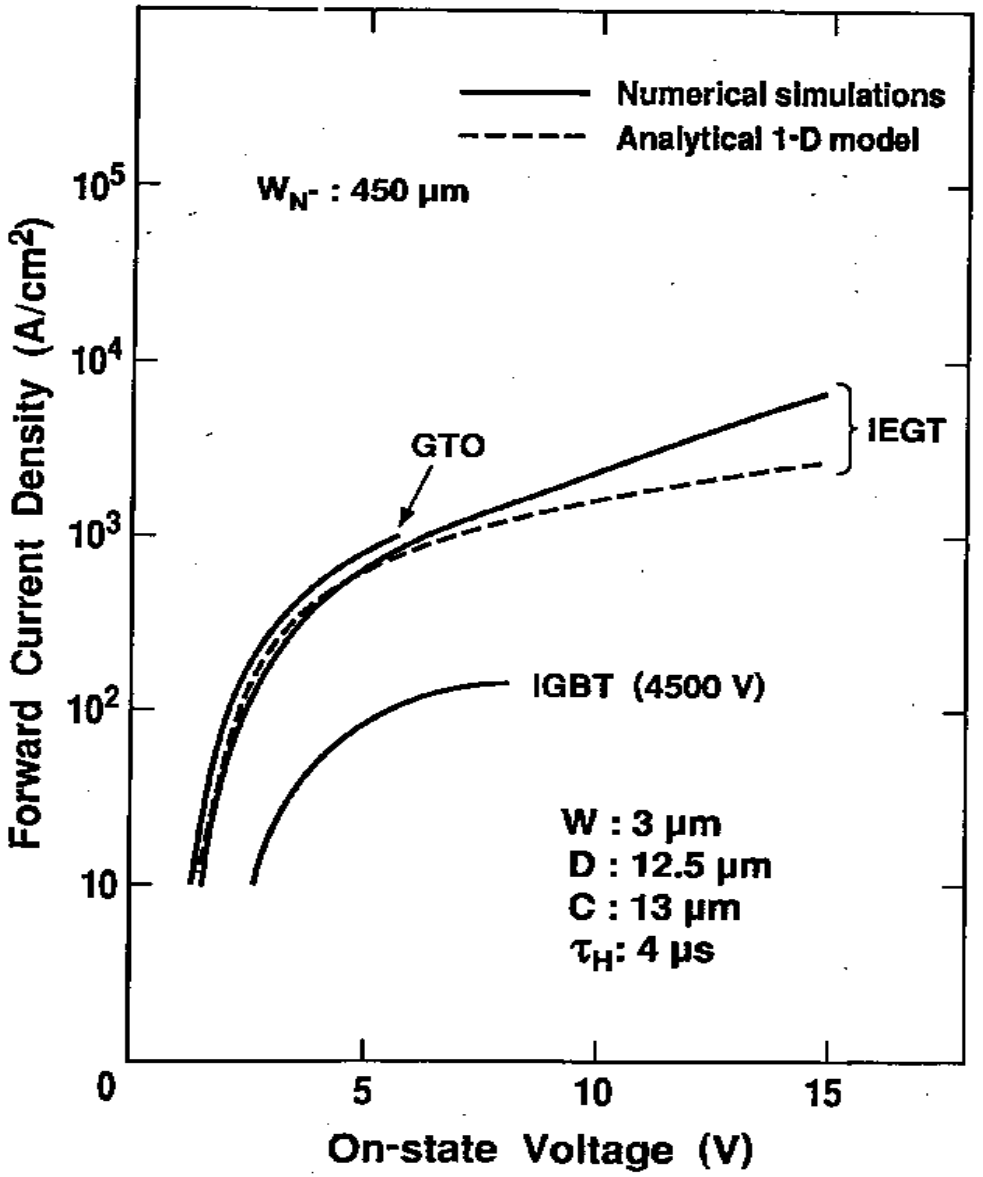
理想のIEGT


IEGT Structure Example
Cathode
CVD
SiO_2
Gate
P
P
Hole
Electron
N
Electron
P
Anode

現実的構造


IEGT Structure Example
Cathode
CVD
SiO_2
Gate
P
P
P
P
Hole
Electron
N
Electron
P
Anode

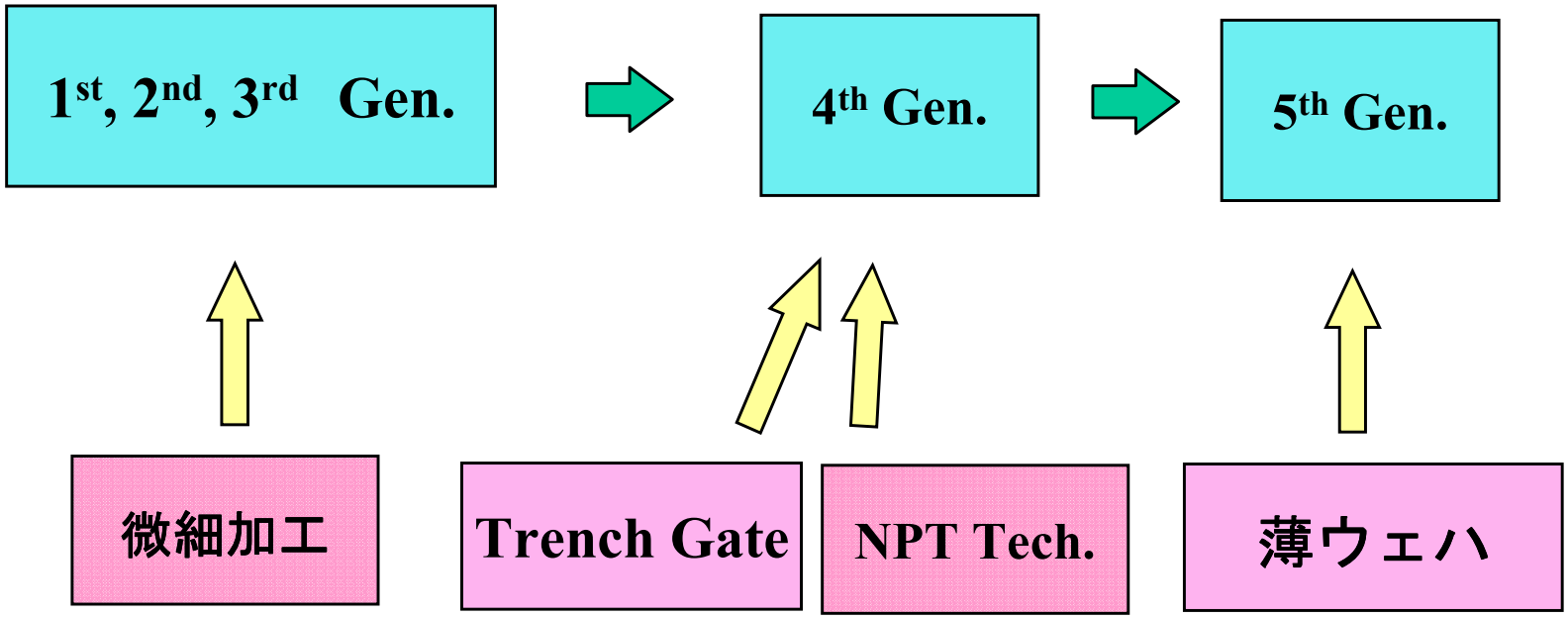
2000年 4.5kV IEGTの実現へ

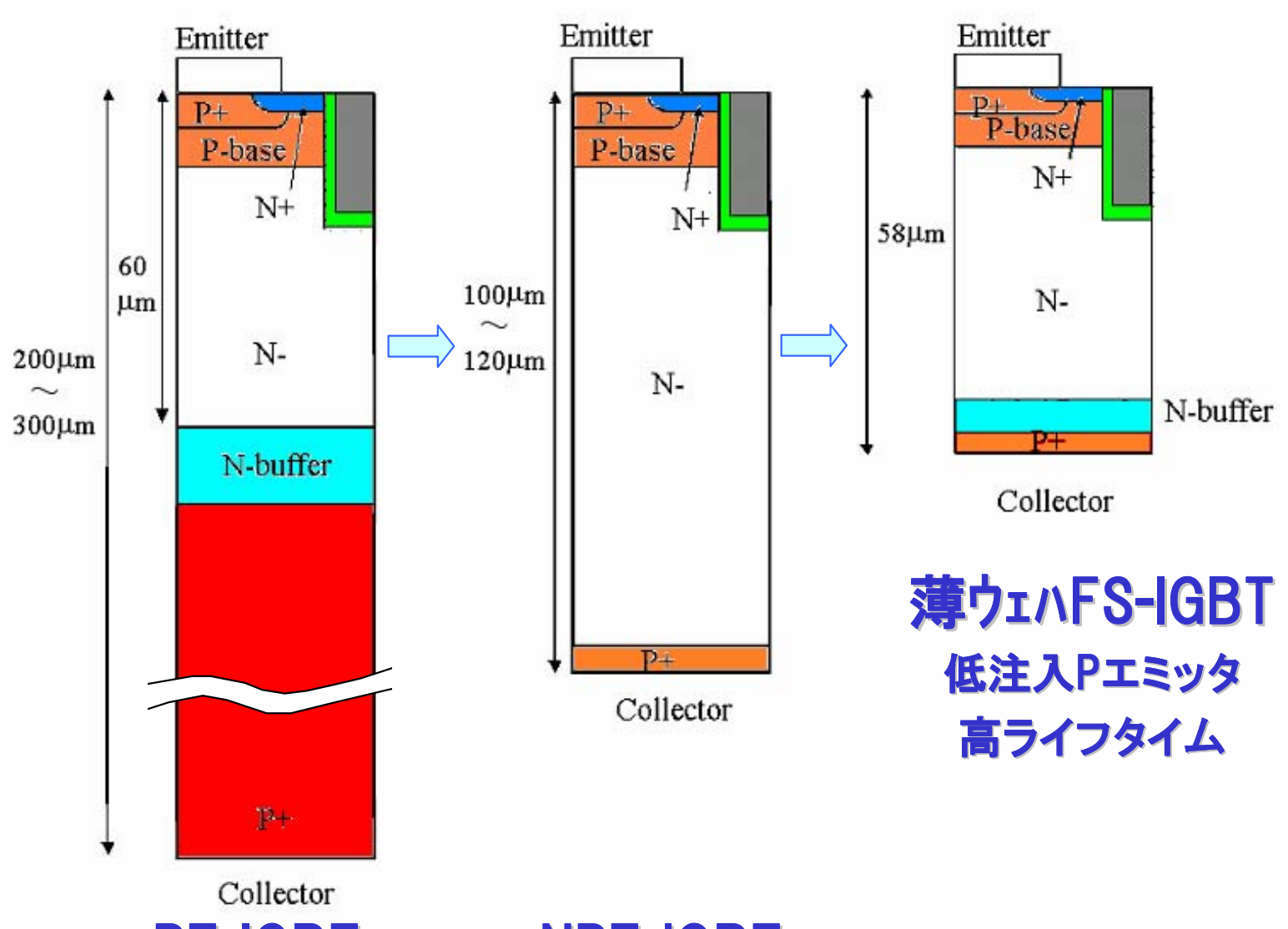


1995年 圧接型パッケイジ
2.5kV圧接型IGBT

2000年 4.5kV IGBT（IEGT)

600-1200V IGBT
技術トレンド





薄ウェハFS-IGBT

低注入Pエミッタ

高ライフタイム

PT-IGBT

高注入Pエミッタ

低ライフタイム

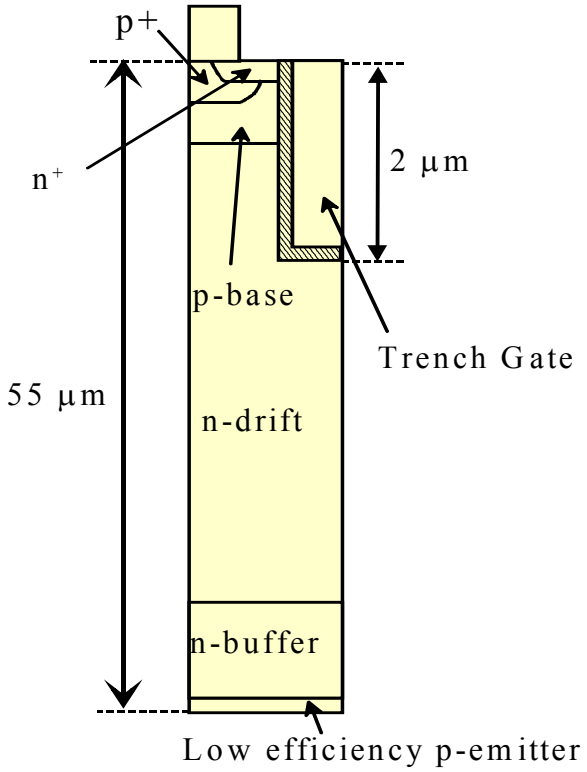
NPT-IGBT

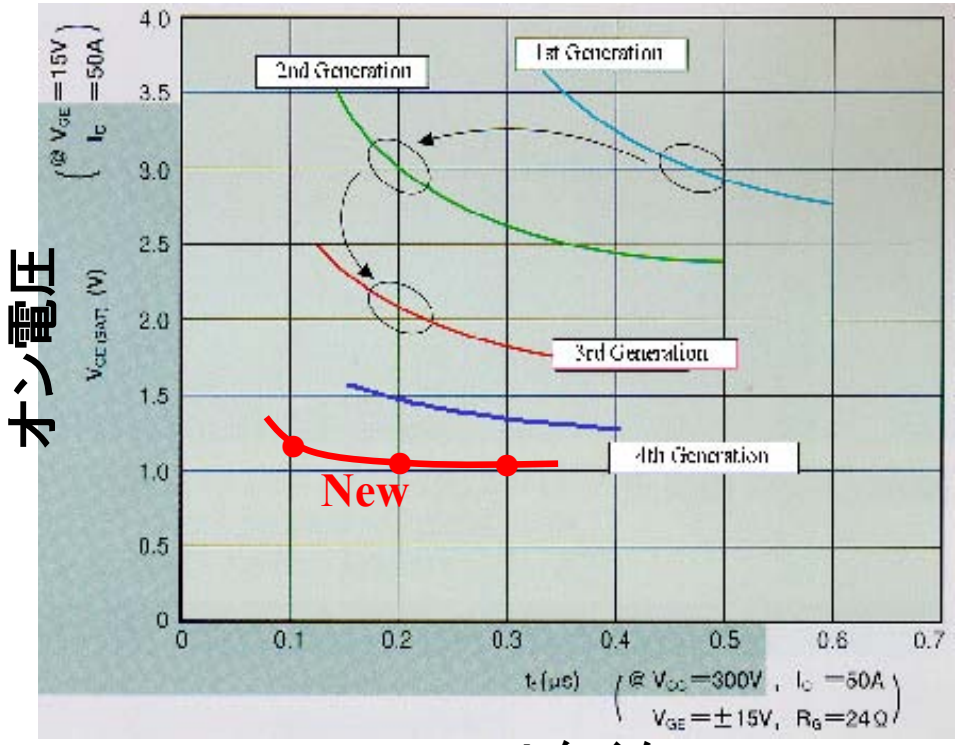
低注入Pエミッタ

高ライフタイム

最新世代IGBT技術 FSIGBT

n-buffer & Low efficiency emitter
Thin wafer technology





フォールタイム

高い目標その3： IGBTで1.0Vのオン電圧@1998年

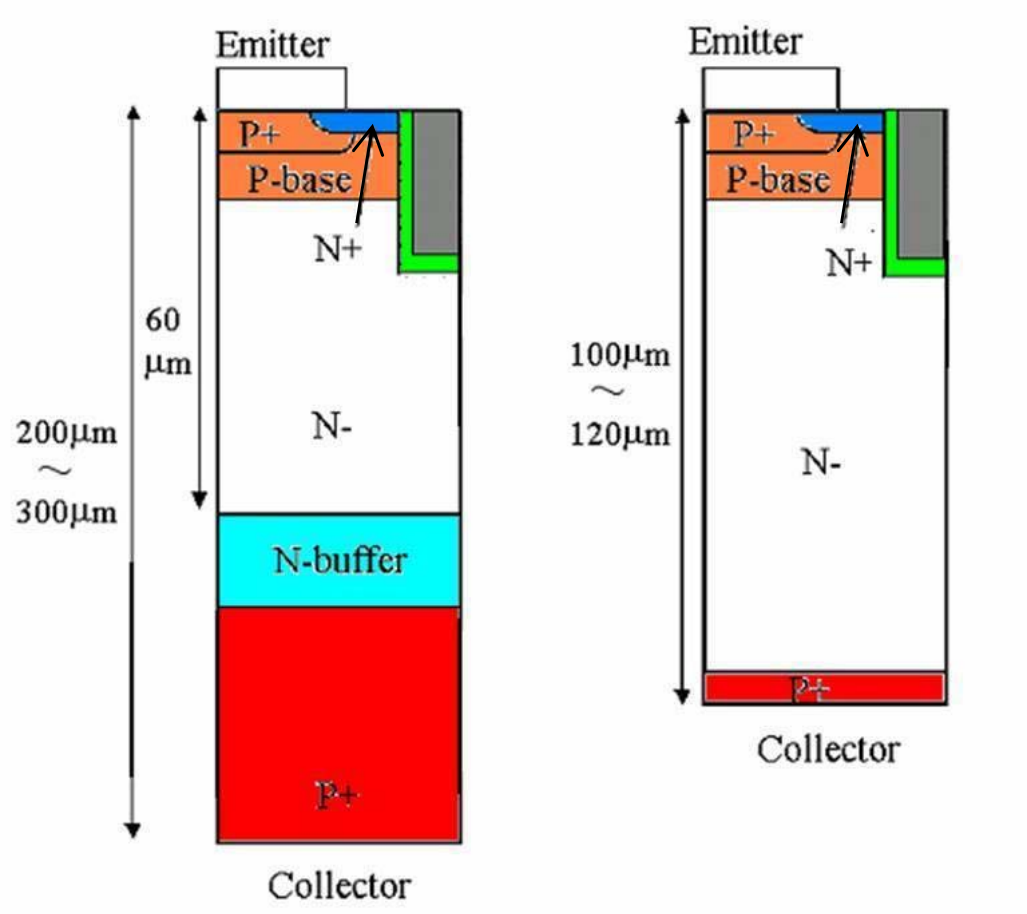
NPT-IGBT全盛の時：

NPTがPTより良いはずがない!!!

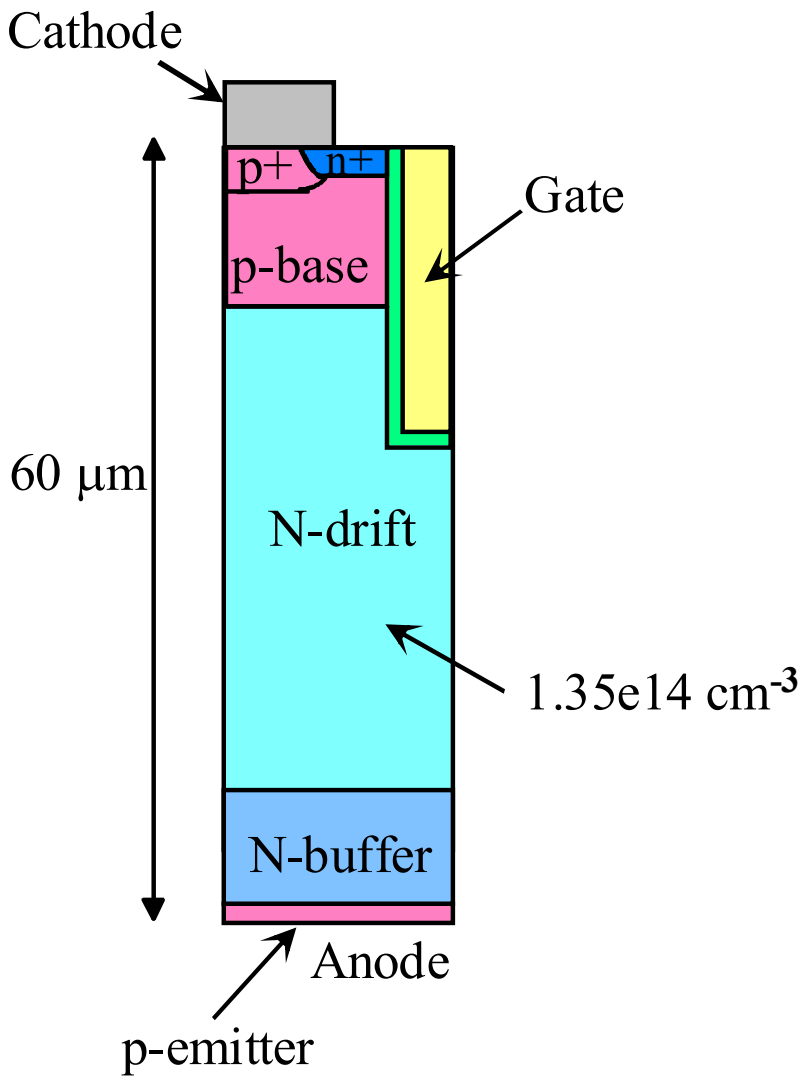
最初のIGBTでPT構造を採用

NPTが良いのはライフタイム制御をやめて低濃度エミッタであるはず!!!

“PT+低注入＋微細加工”で高性能IGBTは可能であろう…と予測!!!



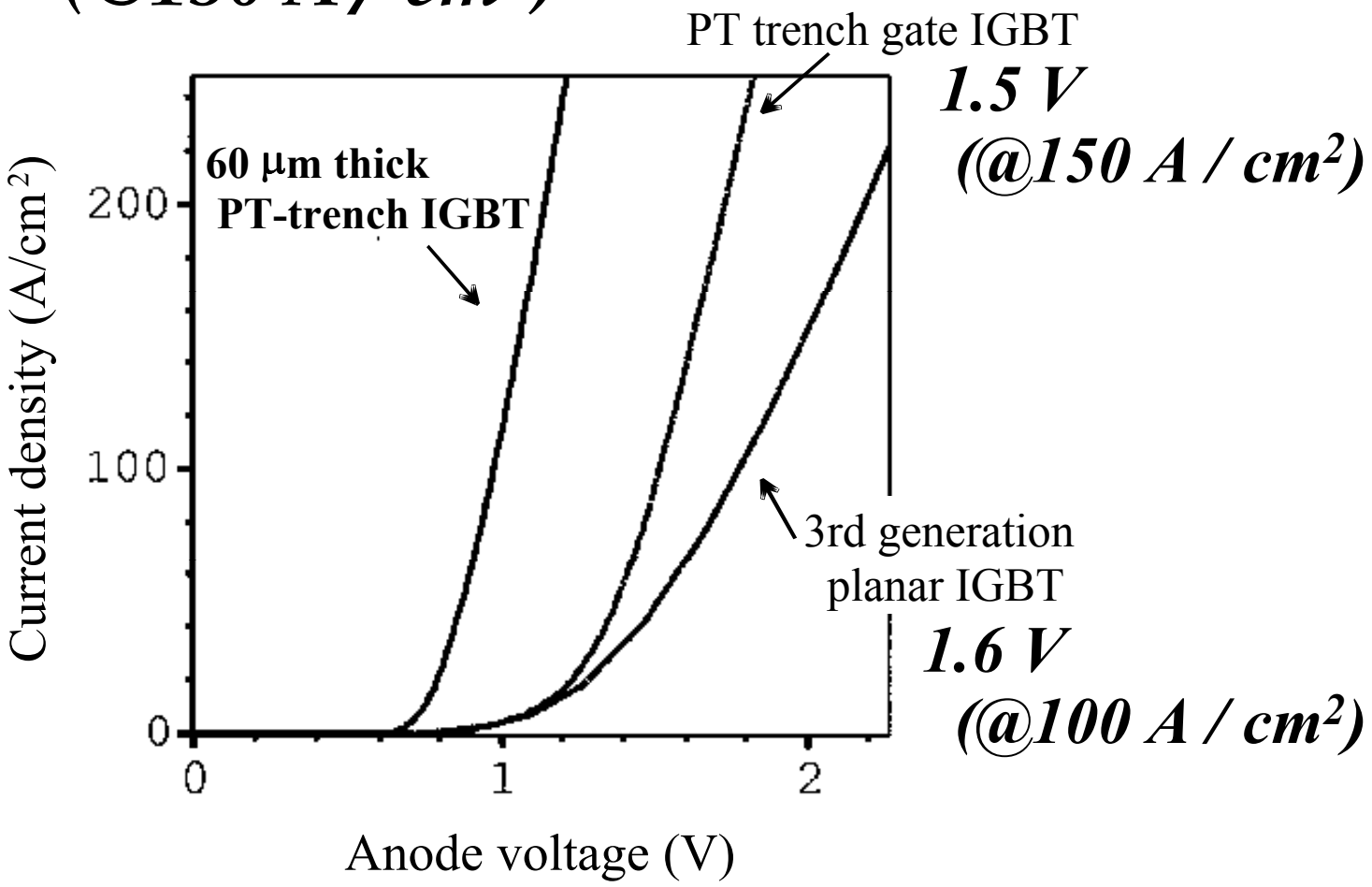
そして、計算した構造の特性が非常に良かった!!! @1998年



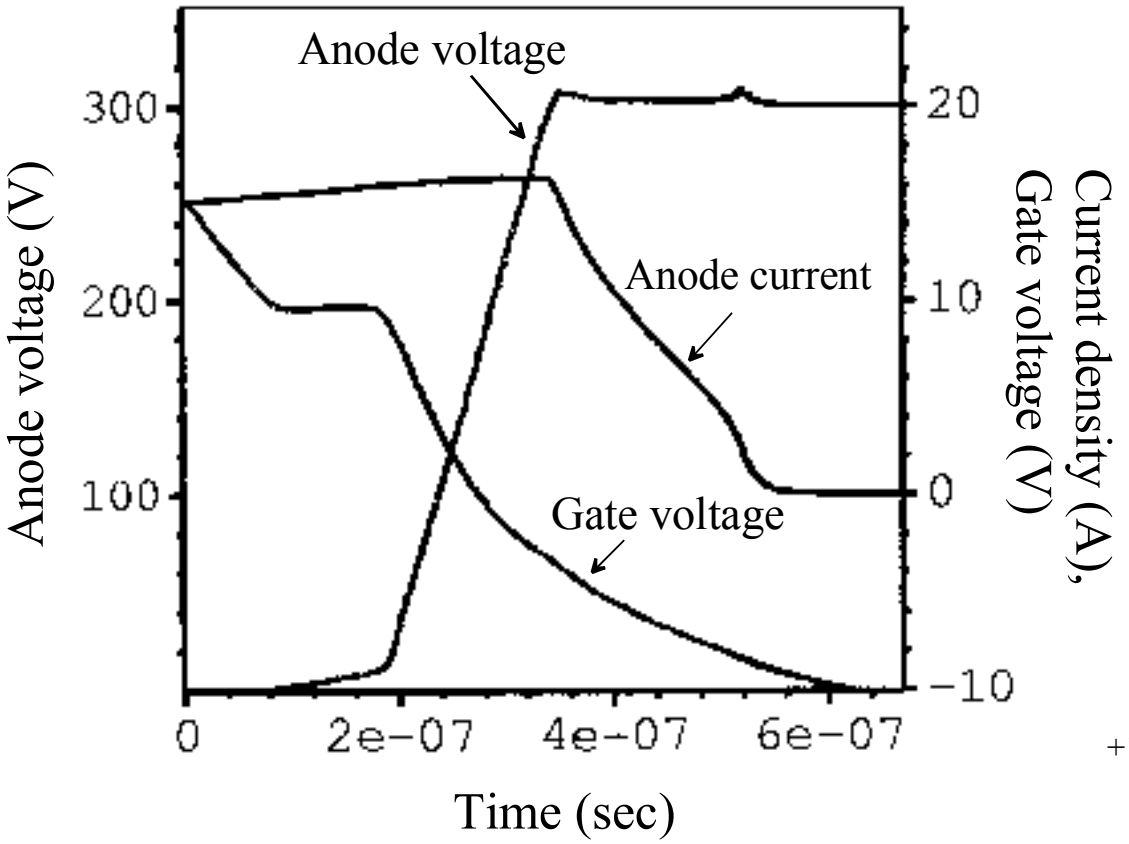
- Total wafer thickness
  - ➔60 μm
- N-buffer layer
  - ➔PT-IGBT
- 低濃度 p-emitter
  - ➔High speed switching
- High carrier lifetime

Calculated forward current-voltage characteristics

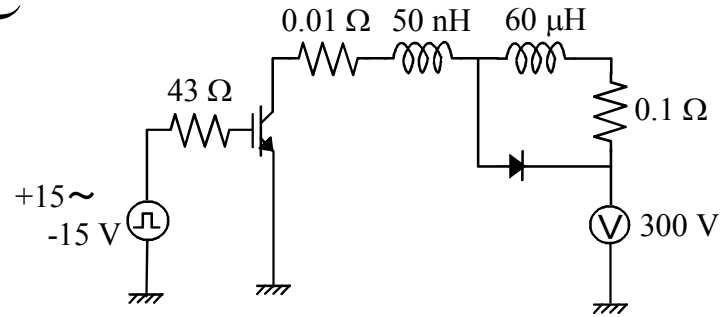
1.04 V (@150 A / cm²)



Turn-off characteristics



tf = 170 nsec



FS-IGBT 最初の学会発表

2000年4月 IPEC-Tokyo 2000 (末代,木下,中川/東芝)

New 600 V Trench Gate Punch-Through IGBT Concept with Very Thin Wafer and Low Efficiency p-emitter, having an On-state Voltage Drop lower than Diodes

Tomoko Matsudai, *Kozo kinoshita and **Akio Nakagawa

Discrete Semiconductor Div., Semiconductor Company, Toshiba Corporation
**Information System Center, Toshiba Corporation*
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1 Komukai Toshiba-cho Saiwai-ku, Kawasaki 210-8583, Japan
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E-mail: tomoko.matsudai@toshiba.co.jp

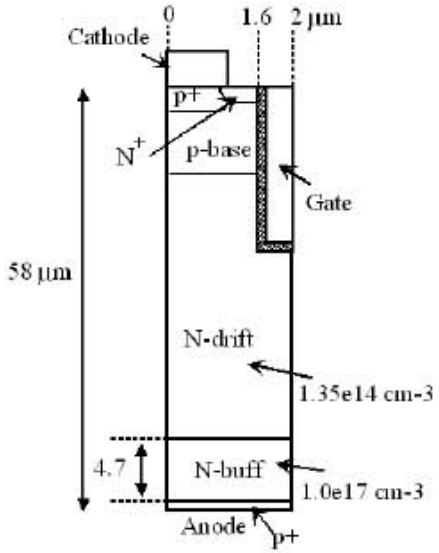


Fig. 1 Cross-sectional view of the simulated trench gate IGBT

Abstract : A vertical trench gate 600 V punch through IGBT(Insulated Gate Bipolar Transistor) structure with a new concept of thin substrate wafer with a low dose n-buffer is proposed, for the first time, to realize an excellent trade-off relation between the device on-state voltage and the switching speed. This paper outlines the ultimate limit design and characteristics, using a very thin wafer in trench gate IGBTs with the transparent p+ emitter and the n-buffer layer. The realized forward voltage drop is predicted to be even lower than that of 600 V diodes with retaining a fast switching speed.

INTRODUCTION

In the vertical devices, the trench gate structure has been widely introduced both for low voltage 600 V IGBTs and high voltage 4.5 kV IGBTs[1,2,3]. The reason is because of the significant improvement that has been achieved in the trade-off relation between a device on-state voltage and a switching speed. It has been widely believed that a lower on-state voltage can be attained by electron injection enhancement from the MOS channel into the drift layer. This leads to an

In the present paper, we successfully introduce the idea of very thin wafer punch-through IGBTs, for the first time, and numerically study the potential of 600 V IGBTs, having an on-state voltage drop lower than diodes. We propose very thin substrate wafer with a low dose n-buffer and the transparent p+ emitter. The proposed IGBT will realize a on-state voltage drop that is even lower than that of 600 V diodes with retaining fast switching speed! The merits of proposed design are that the lifetime control is not necessary and the shallow trench gate is sufficient.

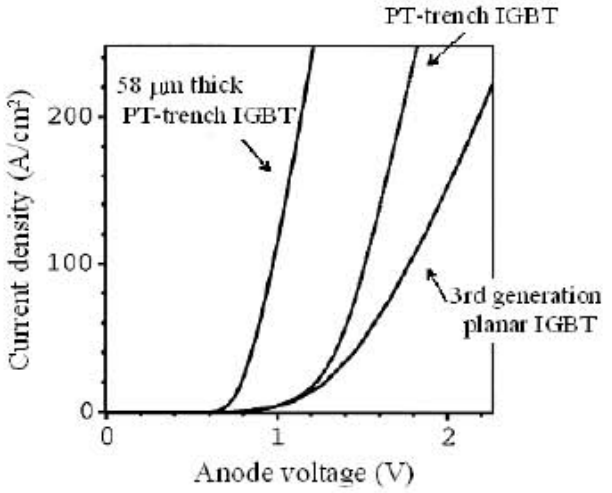


Fig. 3 Simulated forward current-voltage characteristics for conventional IGBTs and 58 µm thick trench gate IGBTs

FS-IGBT Infineonの発表 110um厚みの1200V IGBT

2000年6月 ISPSD 2000 (T.Laska/Infineon)

The Field Stop IGBT (FS IGBT) – A New Power Device Concept with a Great Improvement Potential

T. Laska[1], M. Münzer[2], F. Pfirsch[1], C. Schaeffer[3], T. Schmidt[4]

[1]Infineon Technologies, Balanstraße 73, D-81541 München
[2]eupec, Max-Planck-Straße 5, D-59581 Warstein
[3]Infineon Technologies EZM, Siemensstraße 2, A-9500 Villach
[4]Infineon Technologies OHG; Siemensstraße 2, A-9500 Villach

***Abstract*—By a vertical shrink of the NPT IGBT to a structure with a thin n⁻ base and a low doped field stop layer a new IGBT can be realized with drastically reduced overall losses. Especially the combination of the field stop concept with a trench transistor cell results in the almost ideal carrier concentration for a device with minimum on state voltage and lowest switching losses.**

I. Introduction

In recent years both IGBT concepts of PT (Punch Through) and NPT (Non Punch Through) seem to have been improved vertically to their optimum by innovations of the buffer structure and the lifetime killing process (1,2) on the PT side as well as reducing wafer thickness on the NPT side (3). Also the transistor cell structures were modified by minimizing the planar cells (4) or implementing trench cell geometry (2,5,6,7).
But this must not be the end in progress on IGBT devices, as some drawbacks of both PT and NPT IGBT still did remain: The PT IGBT has an unneccessary high carrier concentration at the back resulting in undesired high turn off current and losses or extremely high lifetime doping leading to a rather high on state voltage. In contrast, the NPT IGBT has the desired low carrier concentration at the back, but the n⁻ layer has to be rather thick due to its triangular electrical field in case of blocking condition. This rather thick n⁻ layer results in higher static and dynamic losses than necessary if the NPT structure were thinner. So both structures are not yet ideal.

advantages of the NPT concept of the low efficient emitter and the high carrier lifetime should not be given up. This is possible by implementing a field stop layer with a very low dose not influencing the low dose p emitter of the NPT IGBT but high enough for stopping the electrical field under blocking conditions (8). So it is possible to shrink the thickness of the NPT structure by 1/3, e.g. a 1200V Field Stop IGBT (FS IGBT) can be made with a thickness of 120µm instead of 175µm. In this case the field stop layer has a doping of only 10^{15} to $10^{16}cm^{-3}$ totally different from typical buffer layers in PT IGBTs. The latter have to act not only for stopping the electrical field but also for reducing the enormous p emitter efficiency in PT IGBTs and therefore have dopings of more than $10^{17}cm^{-3}$ at thicknesses of 10µm or more (figure 1).

	PT-IGBT	NPT-IGBT	FS-IGBT
p-emitter	very high efficient	low efficient	low efficient
n⁻-layer	thin	medium	thin
additional n-layer	buffer layer = highly doped -to reduce the very high emitter efficiency -to stop the electrical field	no	field stop layer = weakly doped -to stop only the electrical field
carrier lifetime	low (lifetime killing)	high	high

Fig.1: Comparison of the different IGBT concepts

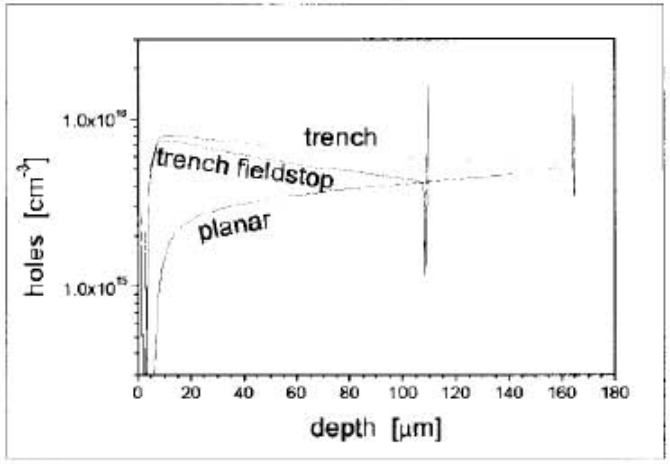


Fig. 7: Simulated carrier concentration of planar NPT, trench NPT and trench FS IGBT

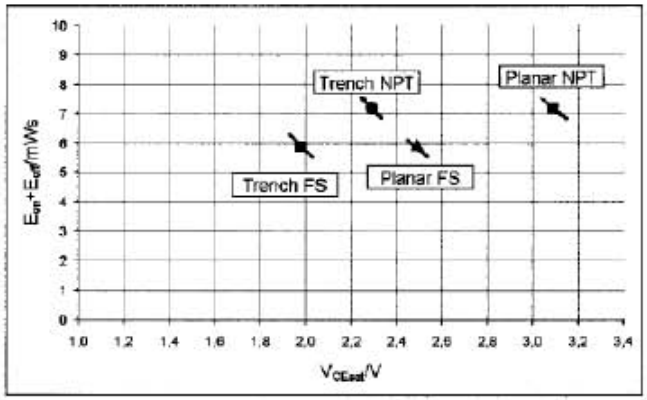
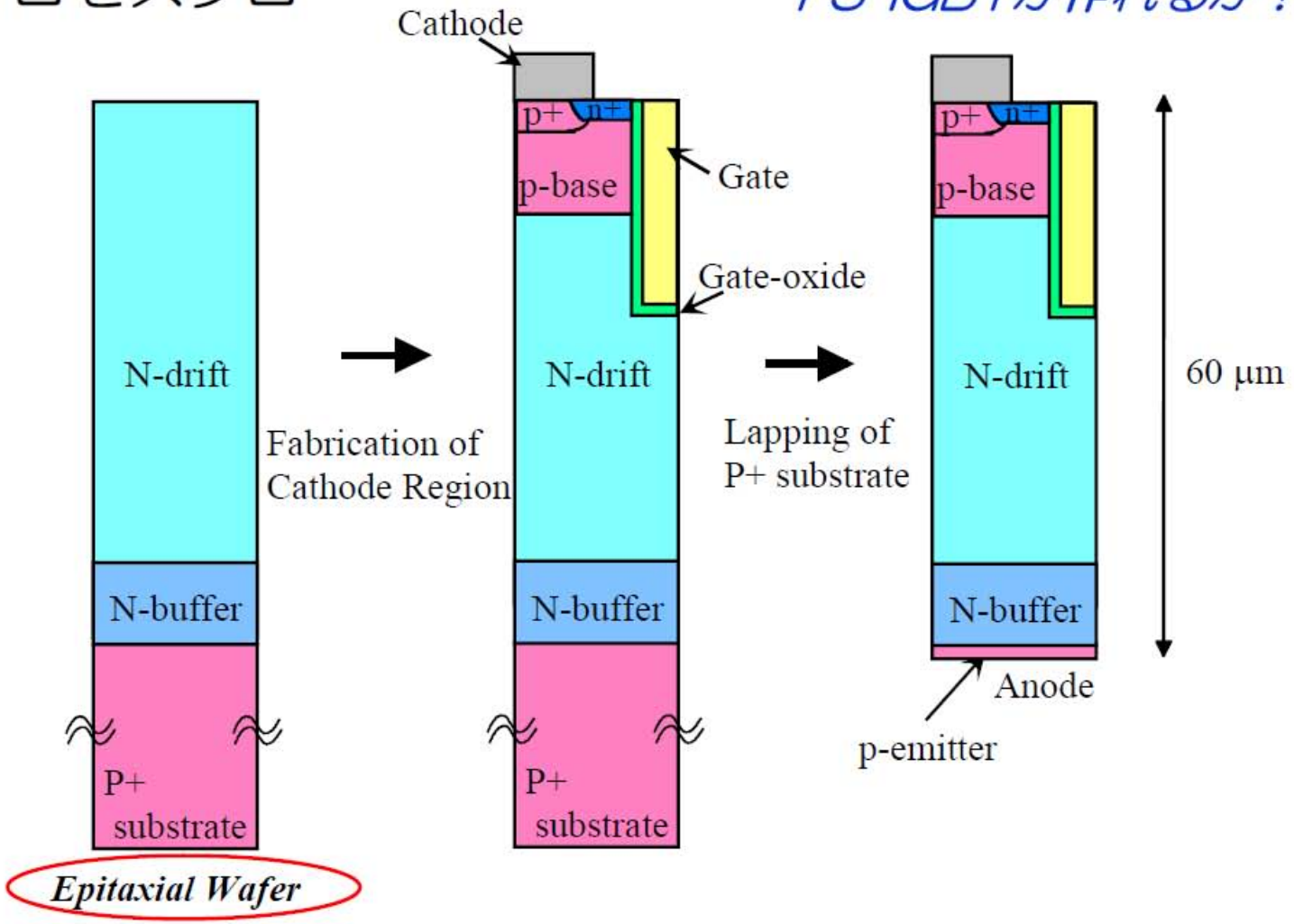


Fig. 6: Trade off diagramm switching losses versus on state voltage (at 125°)

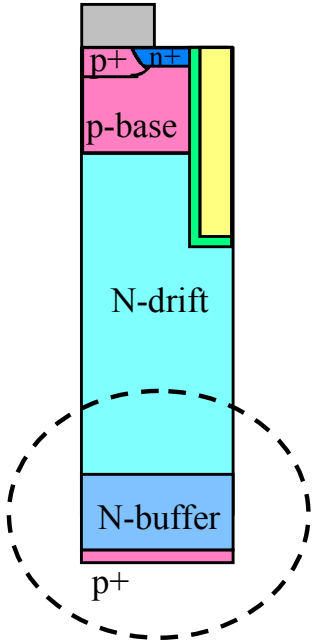
裏面削り残し

プロセスフロー

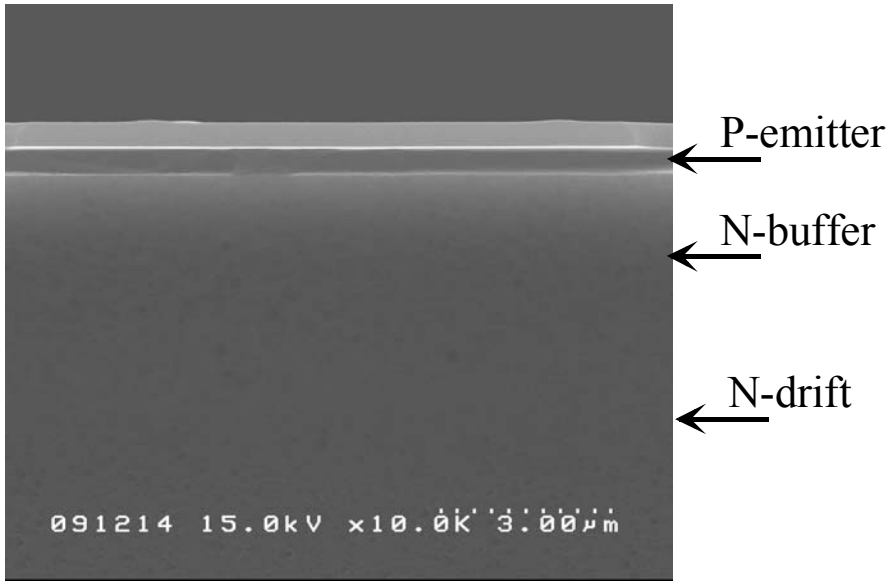
どうやれば今の自分たちに、FS-IGBTが作れるか？



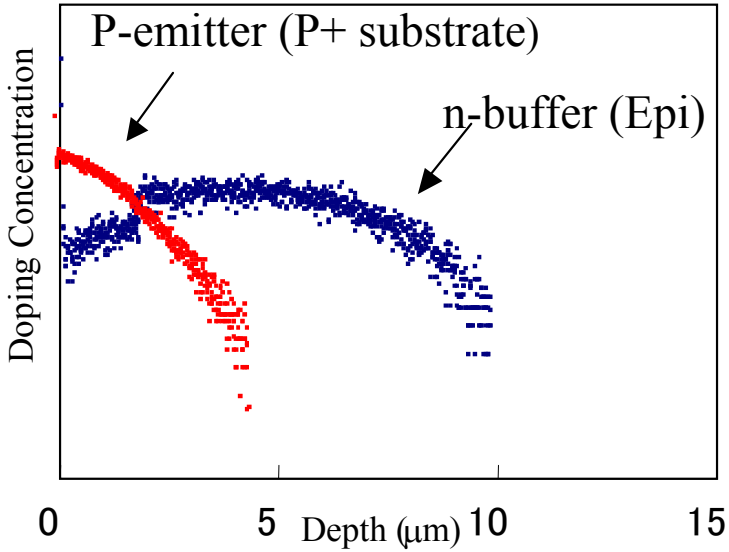
60um厚みの最初のIGBT



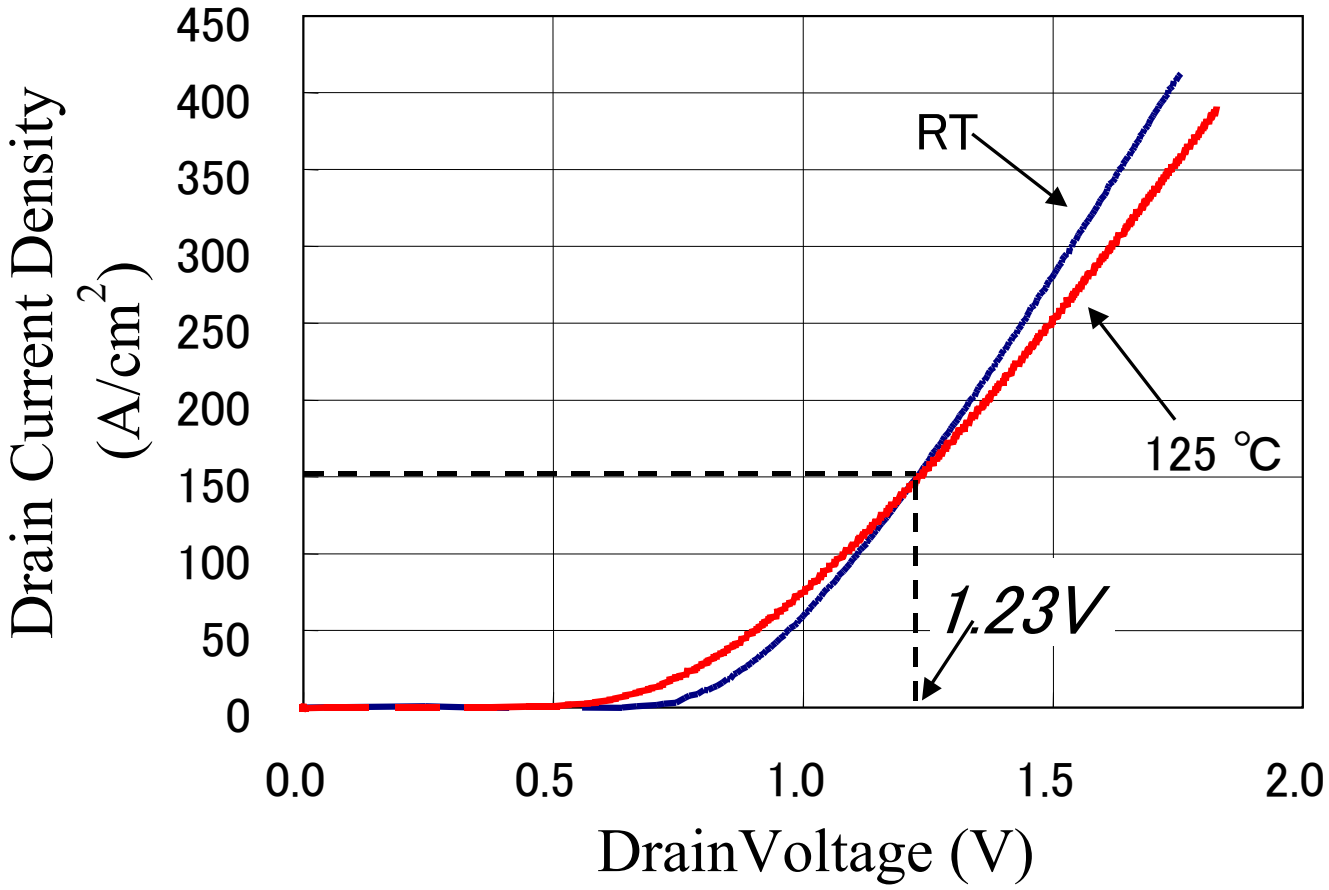
SEM photograph



Impurity distributions

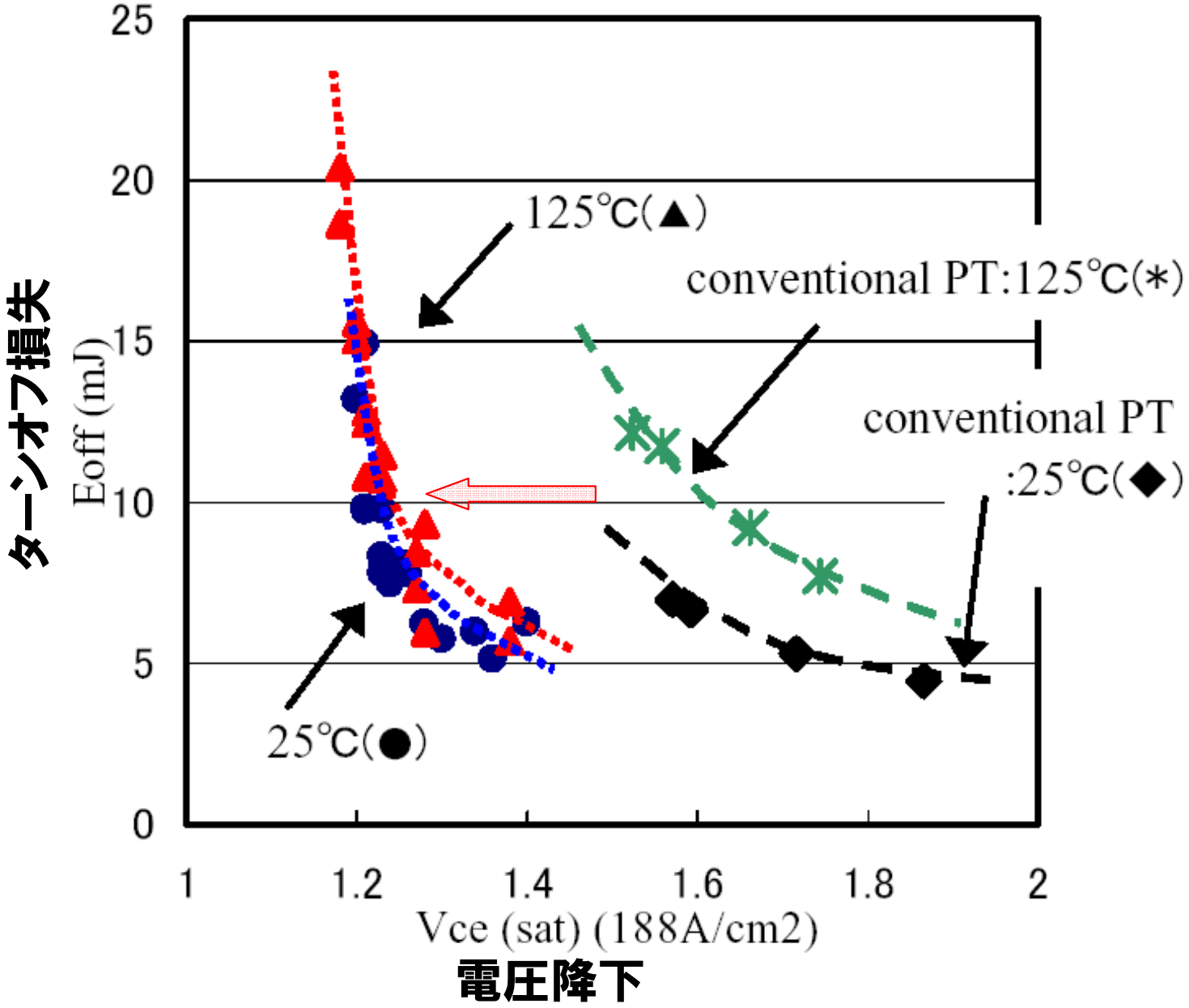


Measured forward current-voltage characteristics



Trade-Off 特性

ISPSD2001

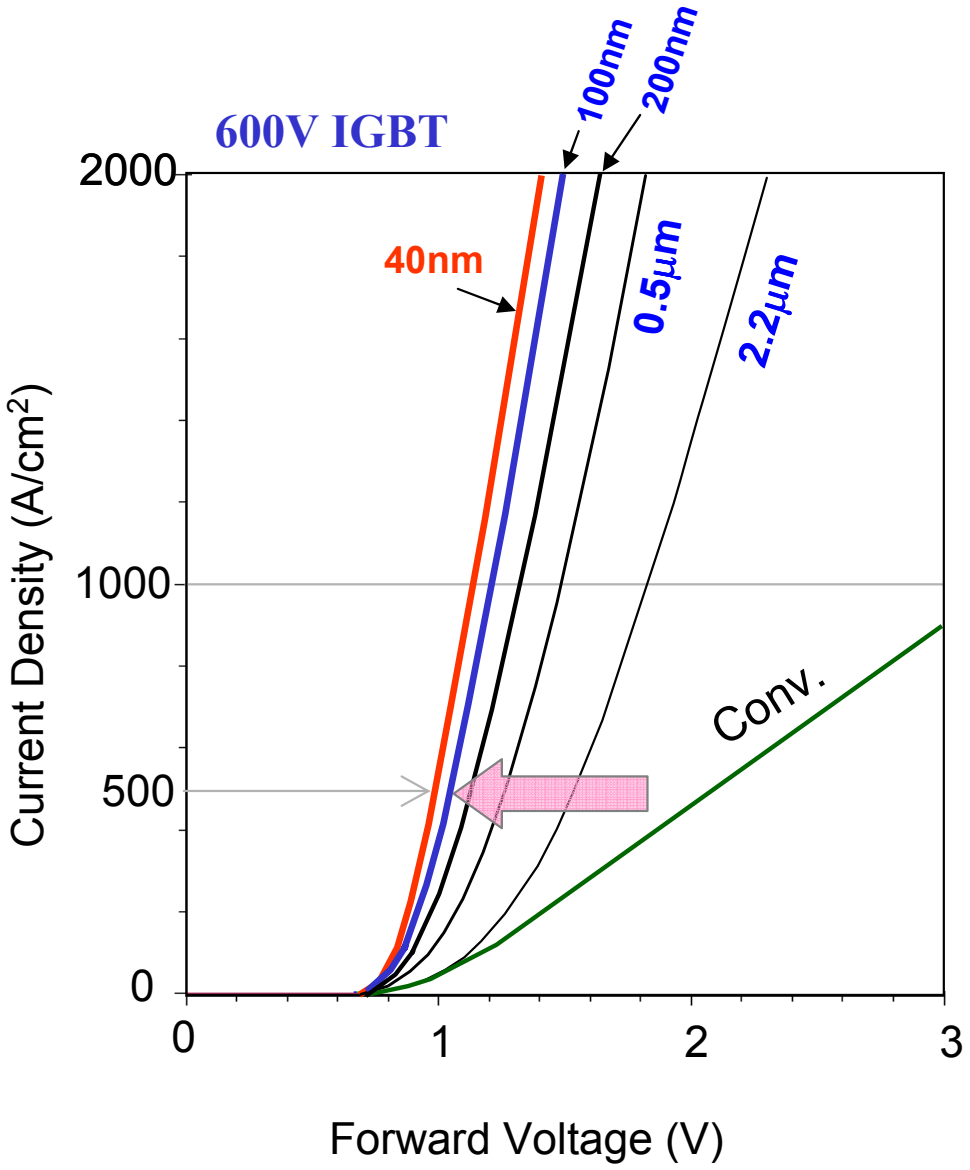


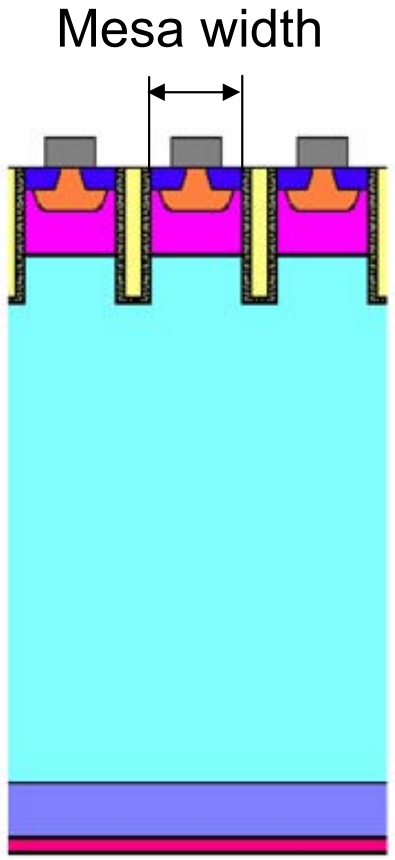
－IGBTのシリコン限界

→　微細化への挑戦!!!

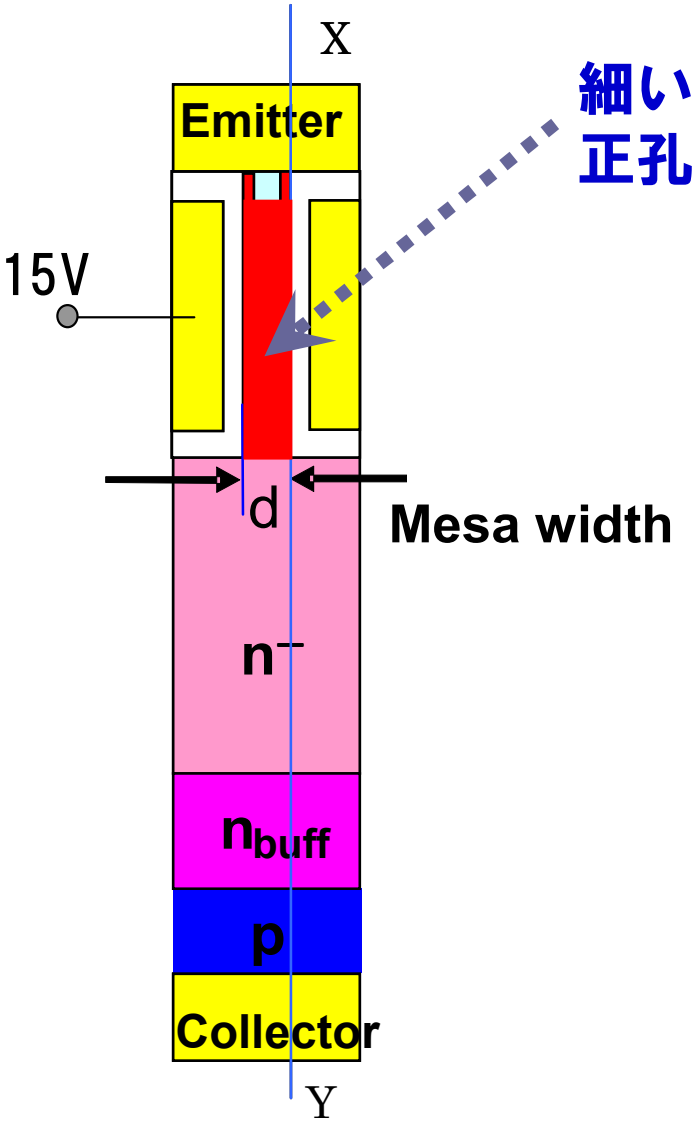
IGBTのシリコン限界は？

まず、メサ幅を小さくしてオン電圧の改善を求めた!!!

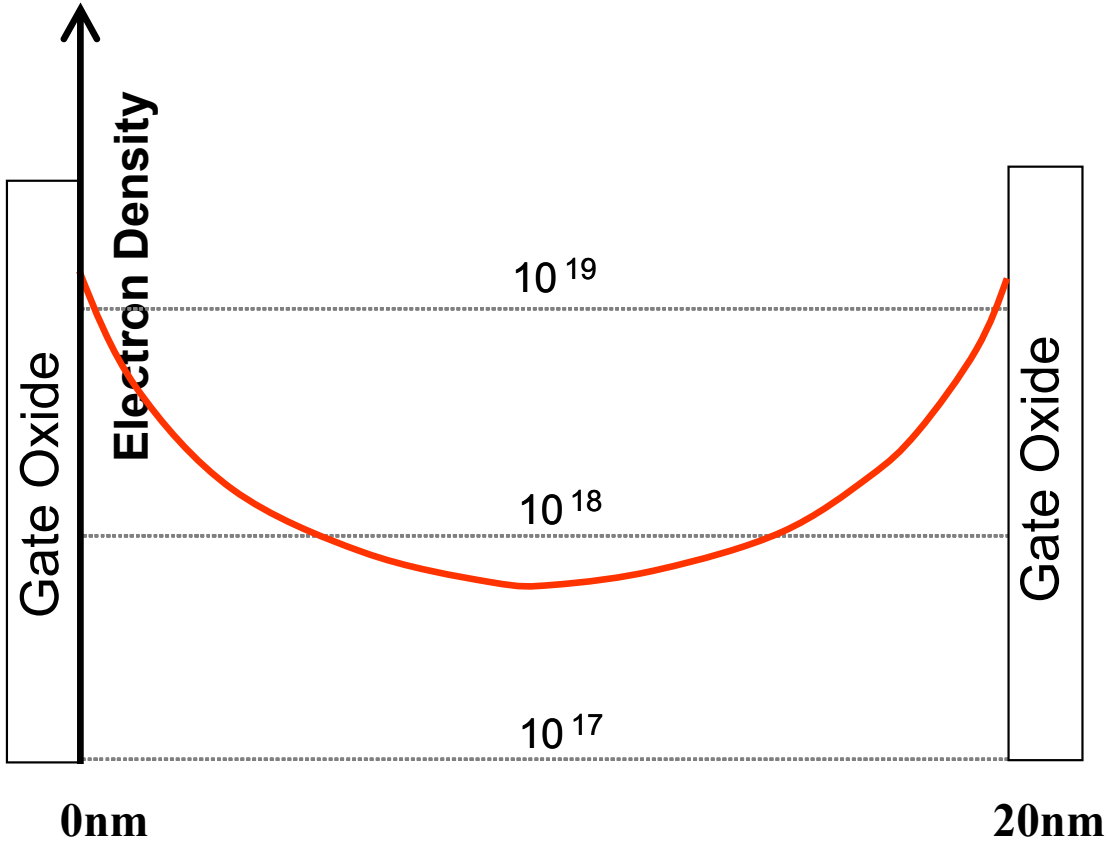




非常に狭いメサのIGBTで究極のIE効果を実現



細いメサではすべてがチャネルになり
正孔は通れなくなる!!　注入効率=1



移動度が高い電子だけで電流でながれるIGBT → 理論限界

$$V_F = \frac{2kT}{q}\ln[\frac{1}{n_i}\{(\sqrt{\frac{QJ}{qD_{pe}}}+b)\exp(\frac{JW_i}{2qa})-b\}]+R_{ch}J$$

$\mu_{electron} > \mu_{hole}$

If all current flows by electron,
this gives the lowest forward voltage!

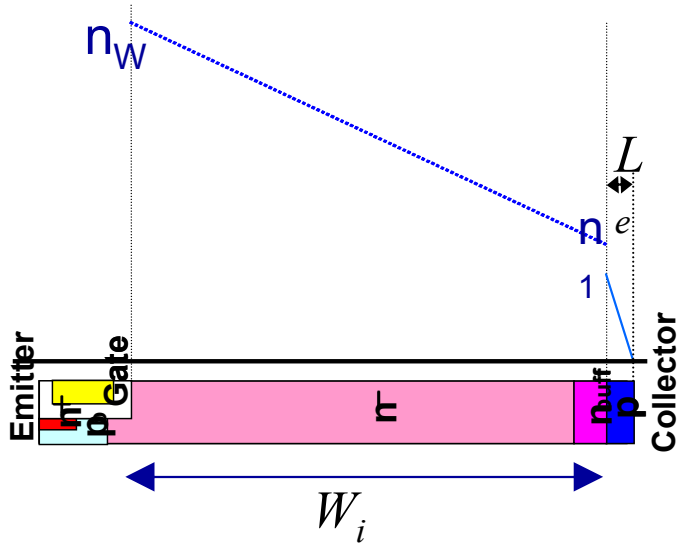
The silicon limit I-V relation can be derived based on the assumption:

(1) No hole current flow.

$$J_p = -qD_p\frac{\partial n}{\partial x}+n\mu_p E = 0$$

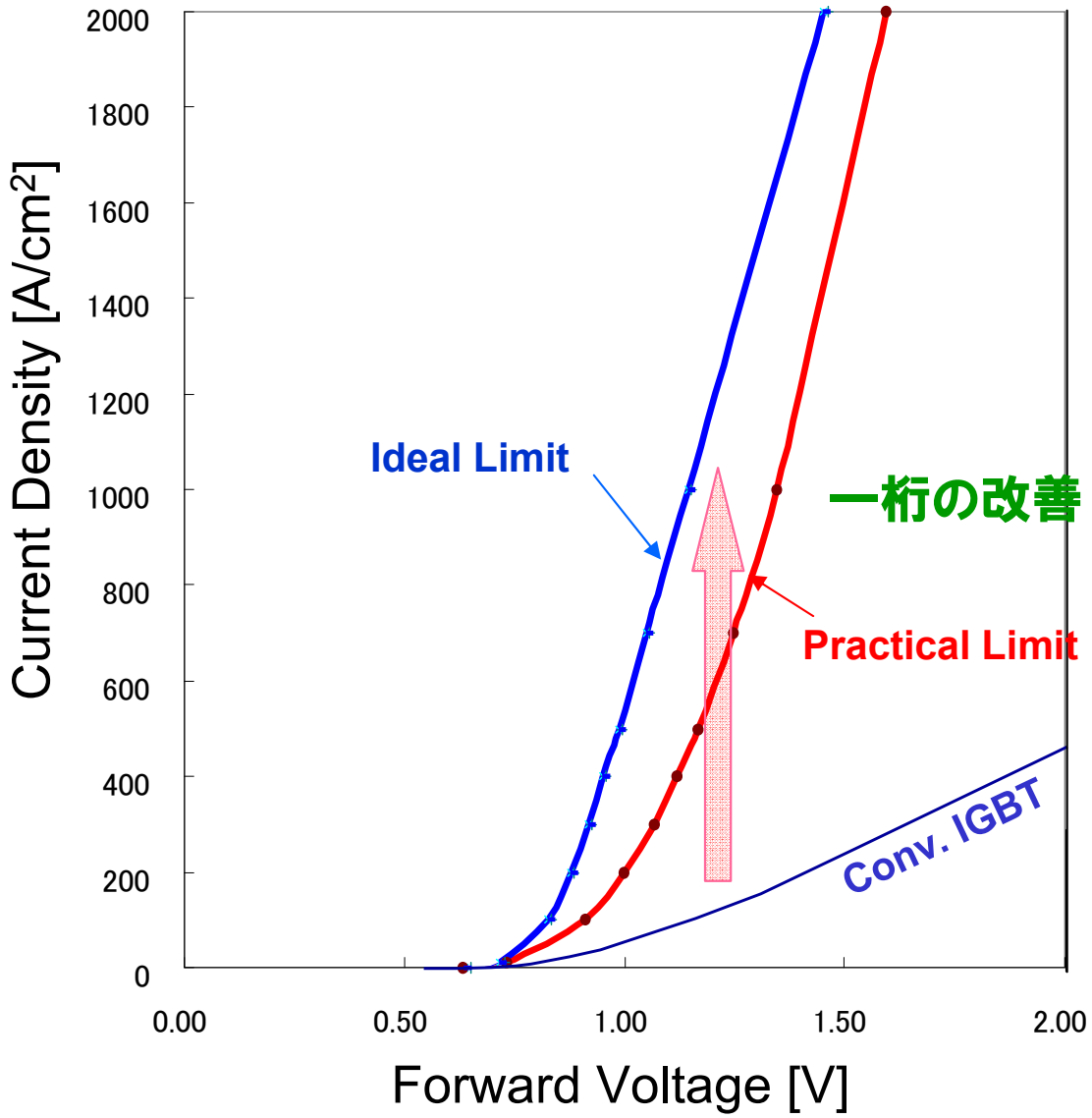
(2) All current flows by electrons.

$$J = J_n = 2\times qD_n\frac{\partial n}{\partial x}$$



理論限界と実用限界

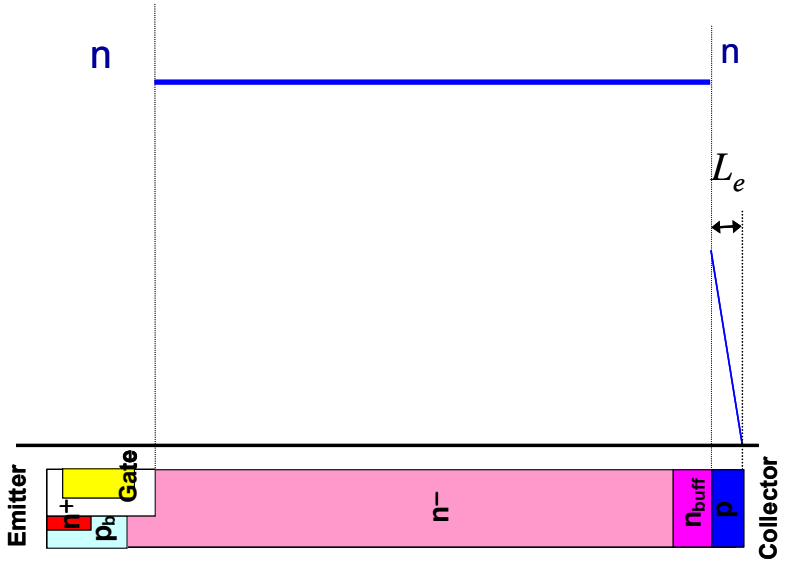
600V IGBT



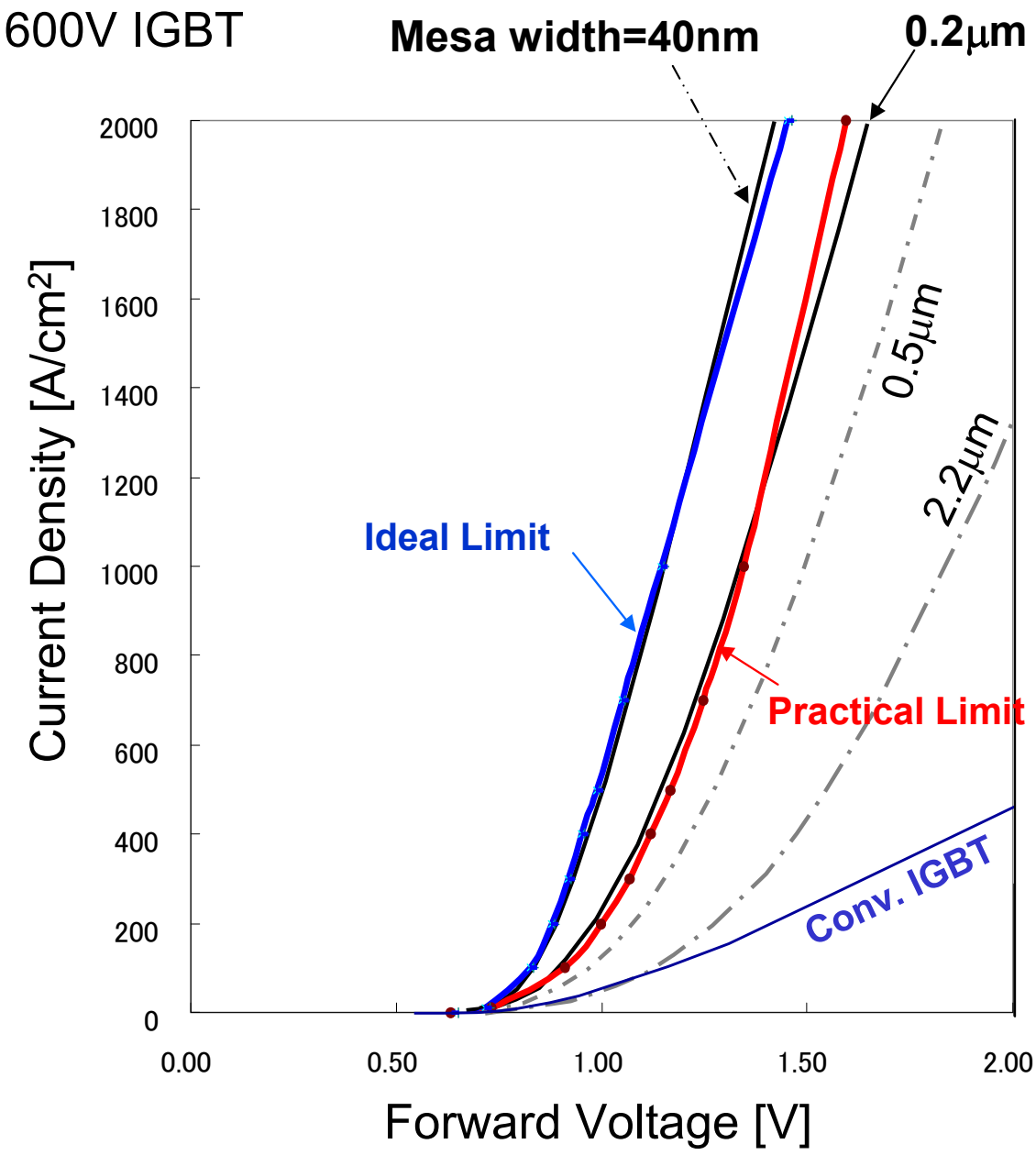
実用限界

Assumption： (1)Flat carrier profile in the n-base
(2)All current flows by drift

$$V_F = \frac{kT}{q}\ln\frac{\mu_n Q J}{qD_{pe}n_i^2(\mu_n+\mu_p)} + W_i\sqrt{\frac{D_{pe}J}{q\mu_n(\mu_n+\mu_p)Q}} + \frac{\mu_n R_{ch}}{\mu_n+\mu_p}J$$

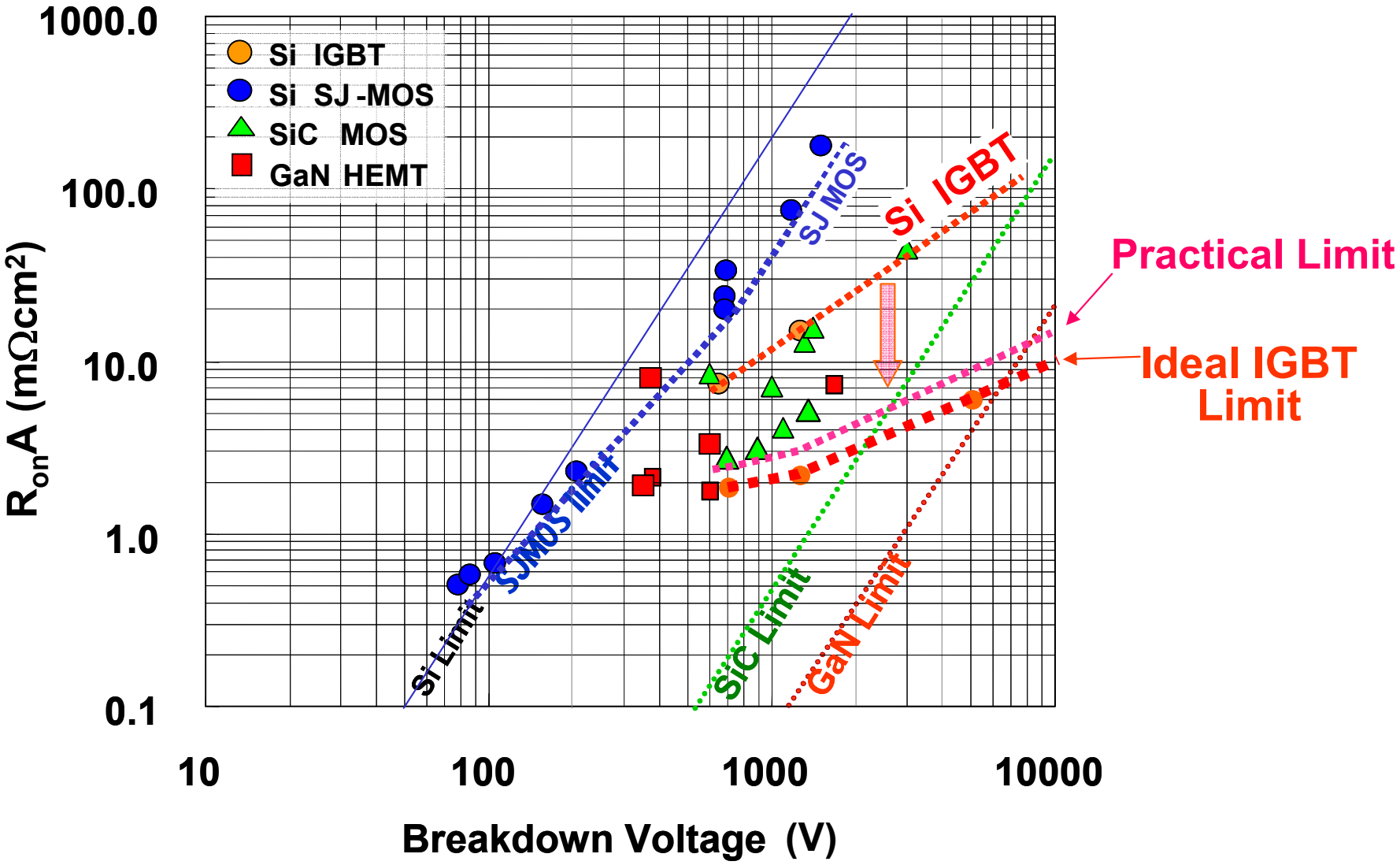


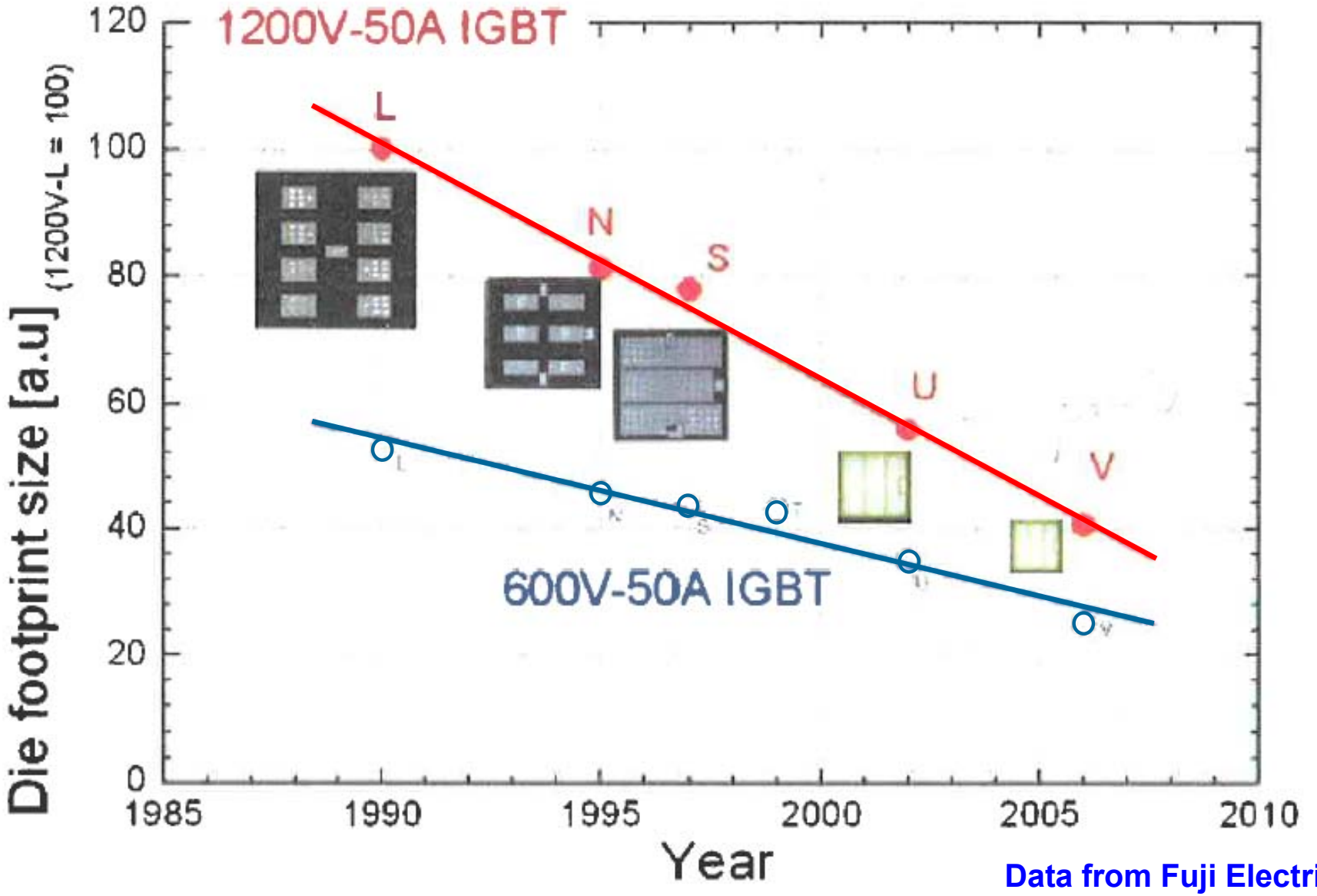
理論とTCADの比較


600V IGBT
Mesa width=40nm
0.2μm
0.5μm
2.2μm
Ideal Limit
Practical Limit
Conv. IGBT
Current Density [A/cm²]
Forward Voltage [V]
2000
1800
1600
1400
1200
1000
800
600
400
200
0
0.00
0.50
1.00
1.50
2.00

Theoretical limit of IGBT

IGBTs can still be greatly improved in future

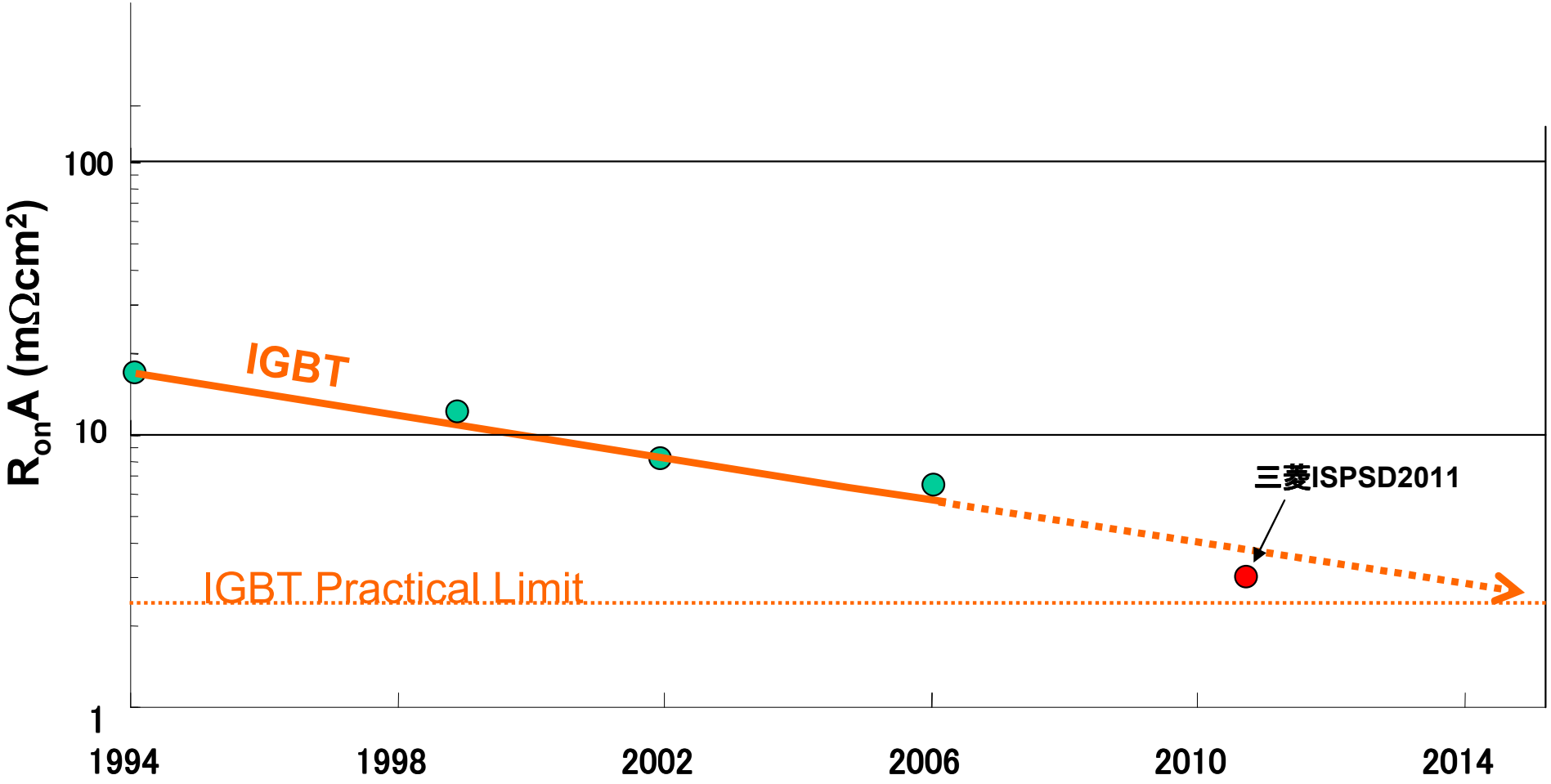




Data from Fuji Electric

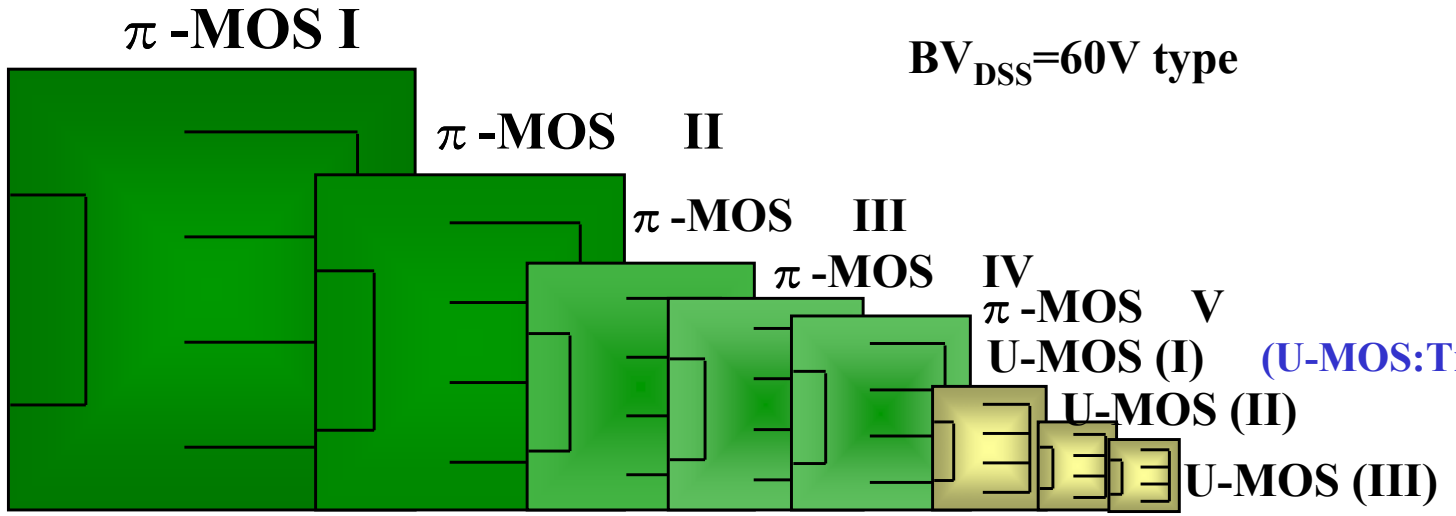
Trends of 600V IGBT

IGBT On-resistance has been steadily improved In the past,
It is predicted that it will approach the practical limit in the future.



パワーMOSFET
－Ideal switching in power MOSFET

パワーMOSFET チップ面積推移



	π-MOS I	π-MOS II	π-MOS III	π-MOS IV	π-MOS V	U-MOS(I)	U-MOS(II)	U-MOS(III)
チップサイズ（相対値）	1	0.6	0.33	0.25	0.2	0.08	0.05	0.04
$R_{DS(ON)}$ （mΩ・cm^2）	12.7	7.6	4.2	3.2	2.4	1	0.6	0.45
セル密度 （Mcells/Inch^2）		0.2	1	2	4	10	30	120
量産時期	1982	1984	1986	1989	1992	1994	1997	1999

Trends of Voltage Regulator Module (VRM)

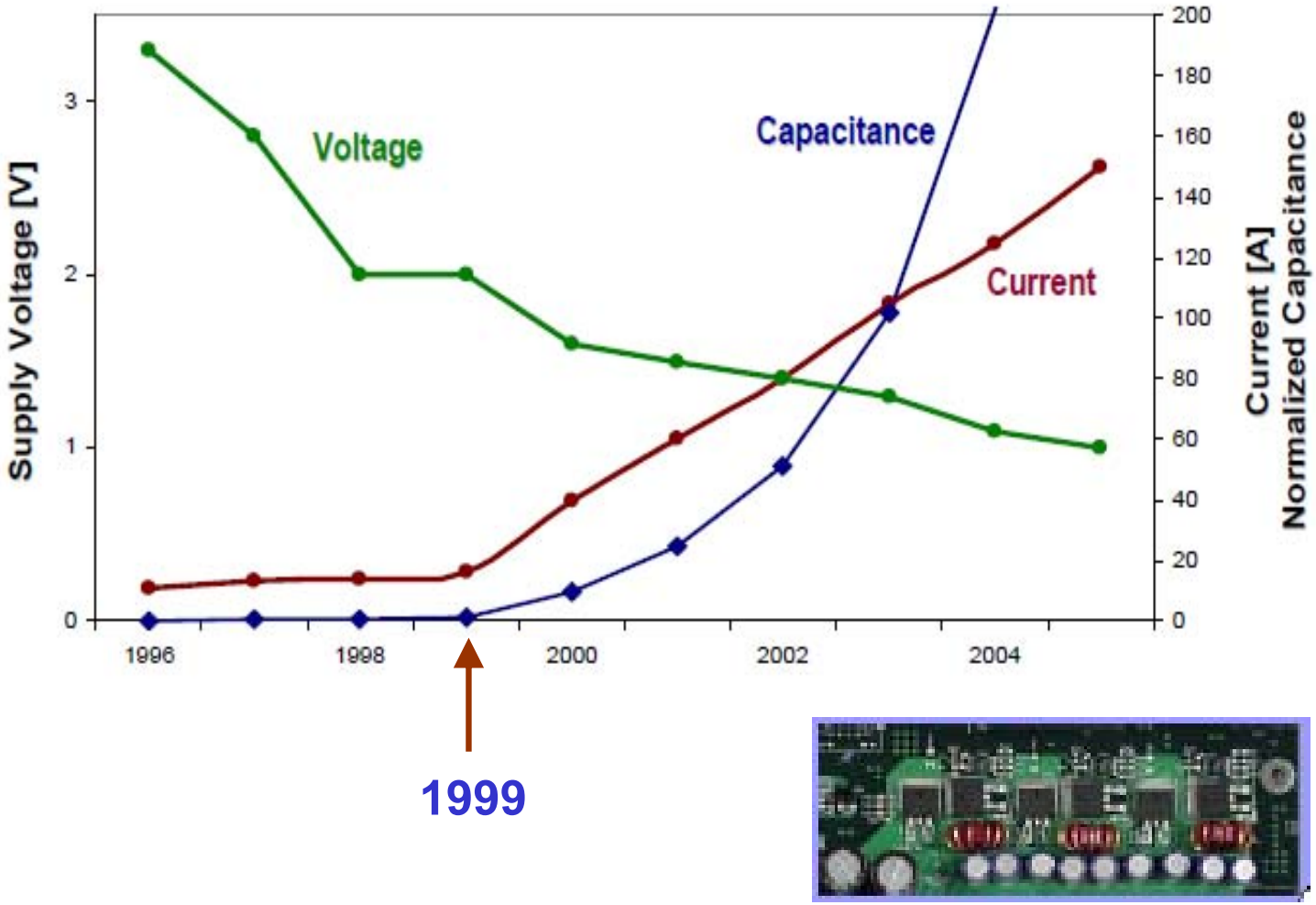
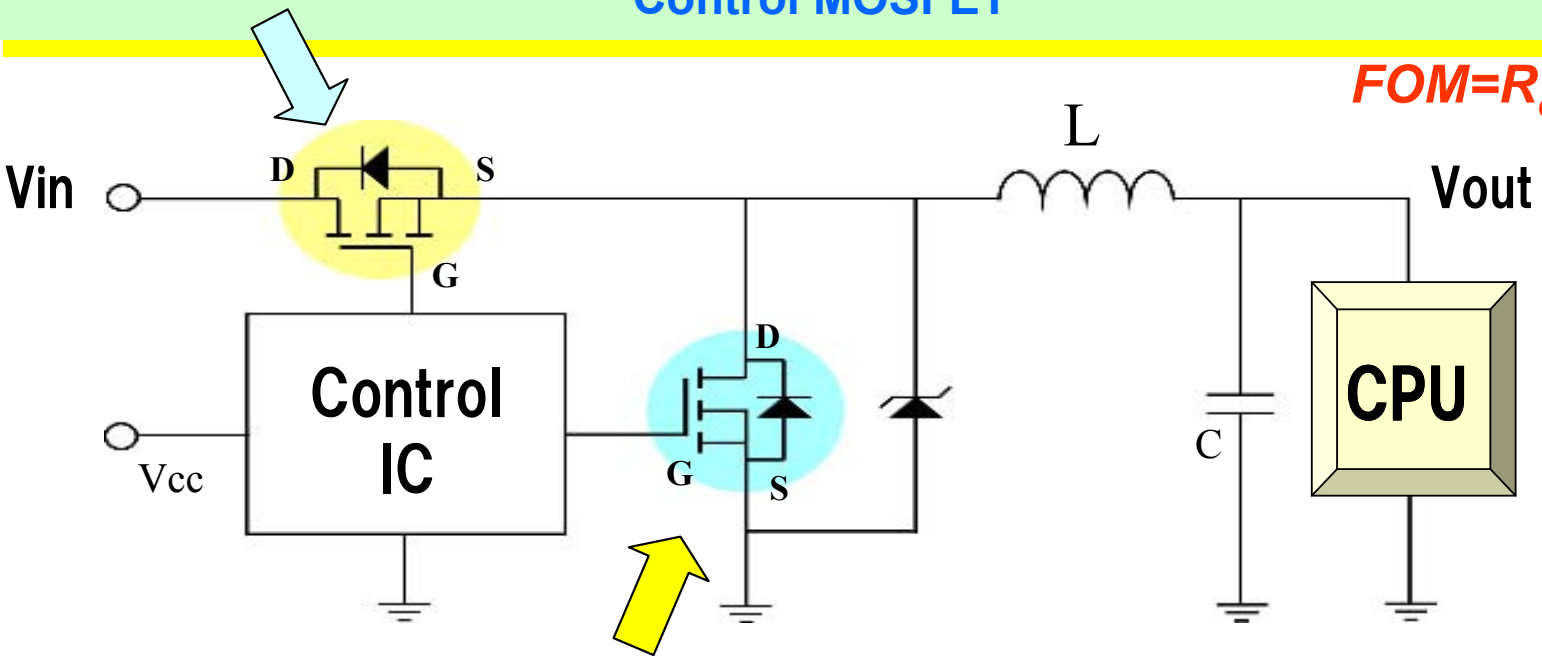


Figure of Merit

$$P_{loss}=(I_d^2 \times R_{on}) + (I \times Q_{gd}/i_g \times V_{in} \times f) + (Q_g \times V_g \times f) + (Q_{oss}/3 \times V_{in} \times f)$$

Control MOSFET

$FOM=R_{on}Q_{gd}$



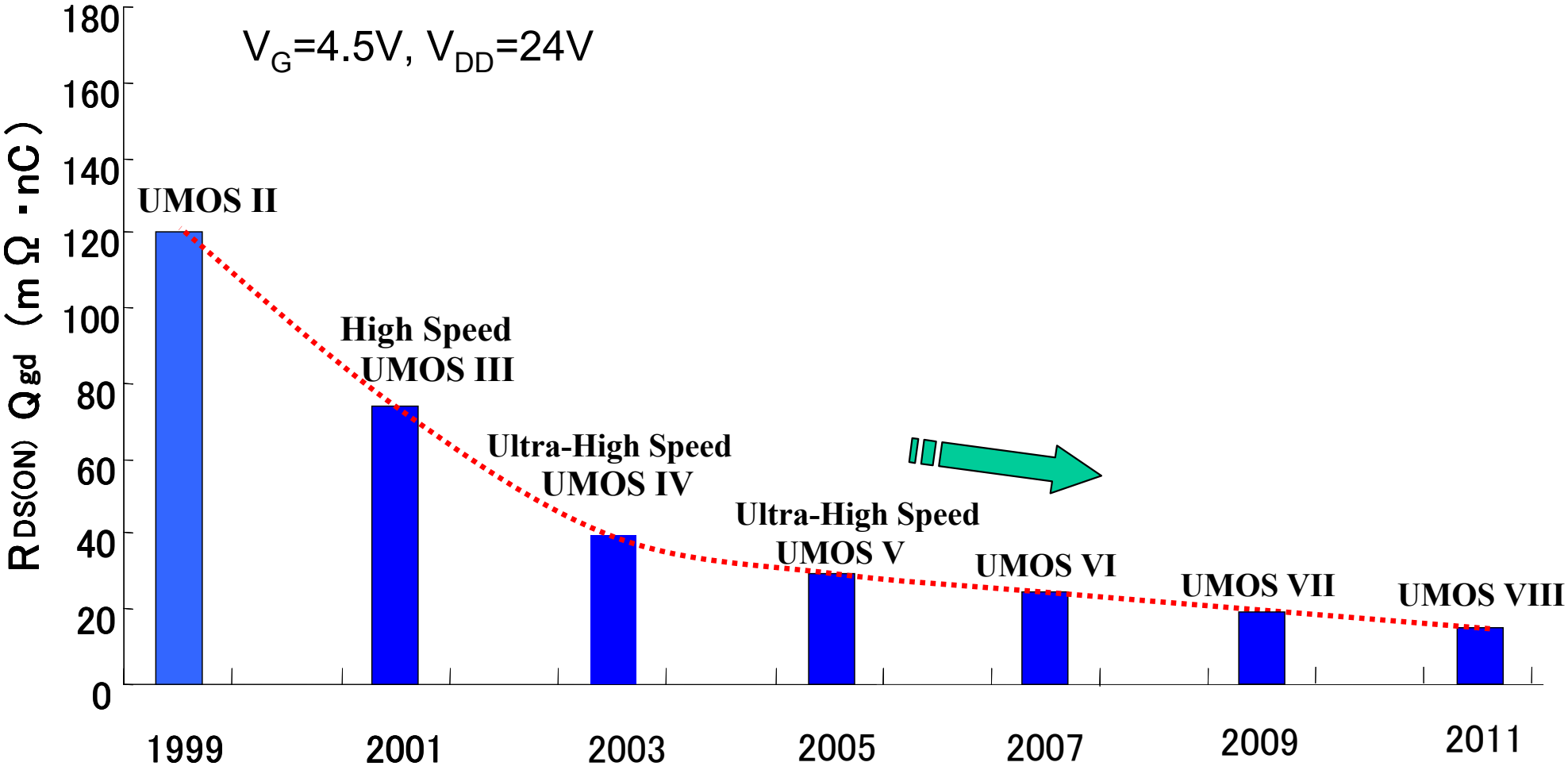
$$P_{loss}=(I_d^2 \times R_{on}) + (Q_g \times V_g \times f) + (Q_{oss}/3 \times V_{in} \times f)$$

Synchronous MOSFET

$FOM=R_{on}A$

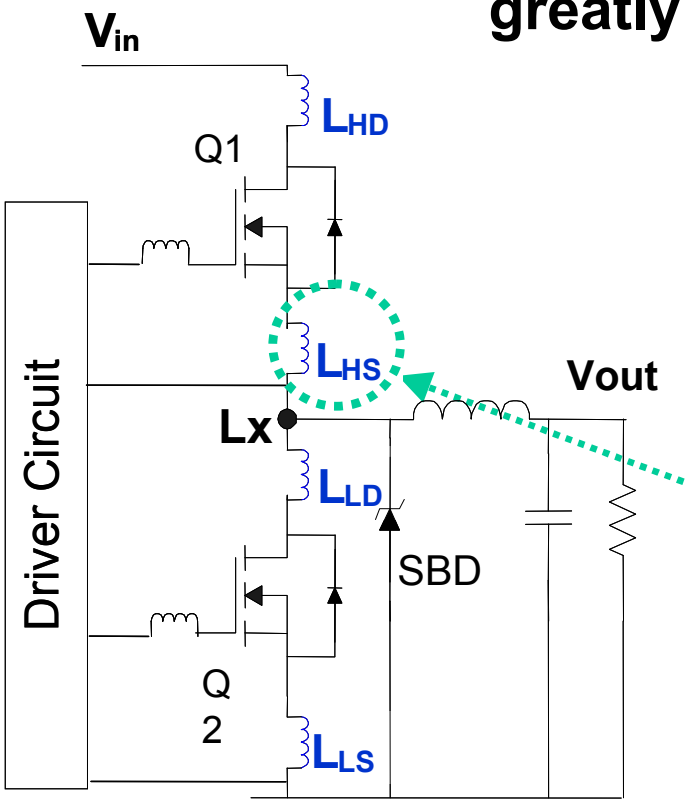
Trend of High Speed MOSFET

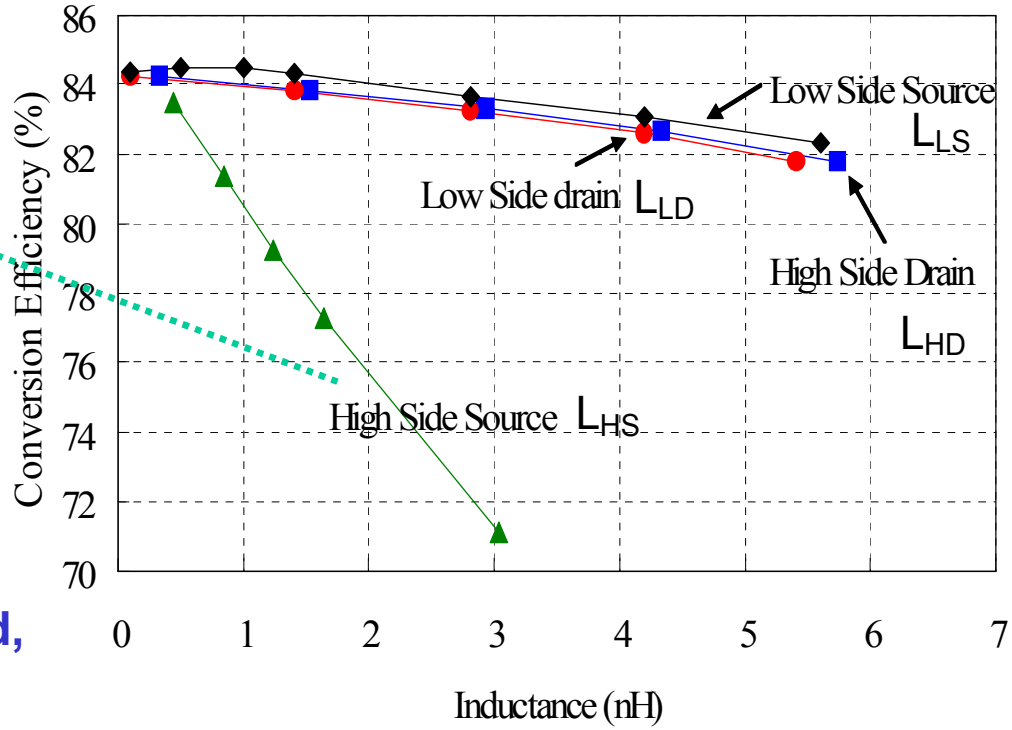
Figure of Merit: $R_{on}Q_{gd}$



Influence of parasitic inductances

Parasitic inductances in the power stage circuit greatly influence the converter efficiency.

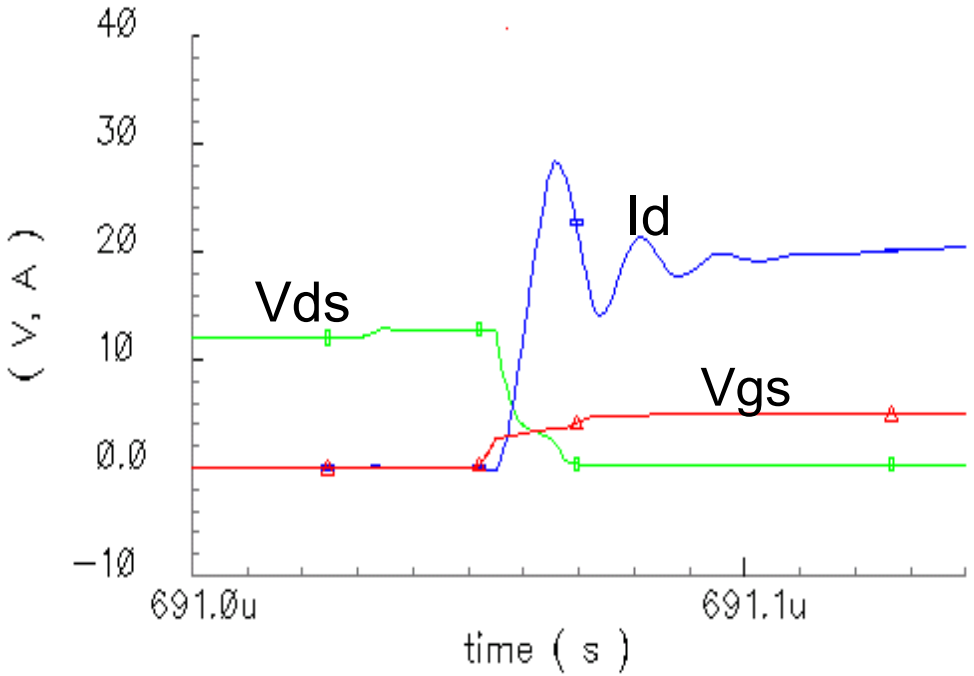




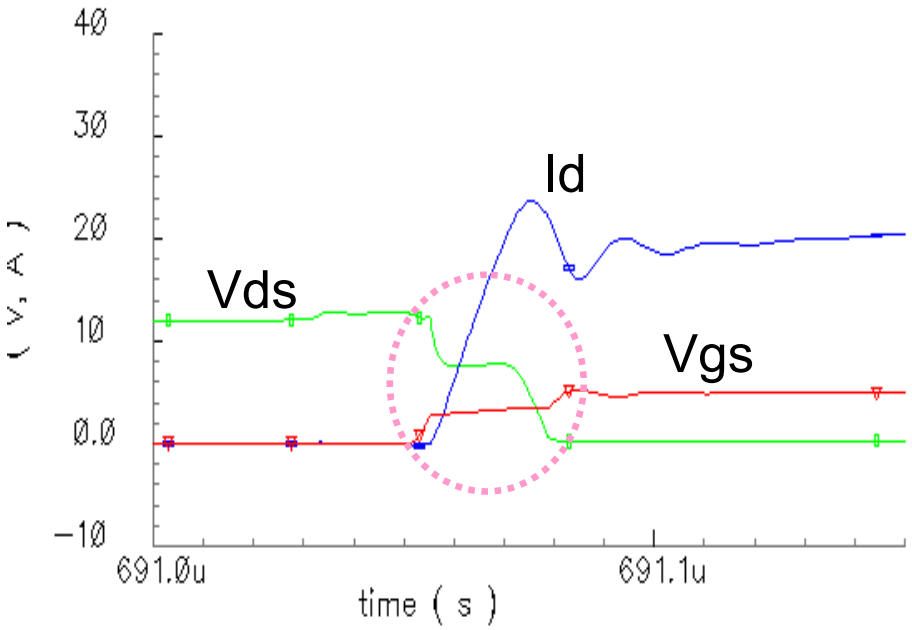
4 parasitic inductances are examined, using circuit simulator.

High side MOS turn-on is delayed by L_{HS}

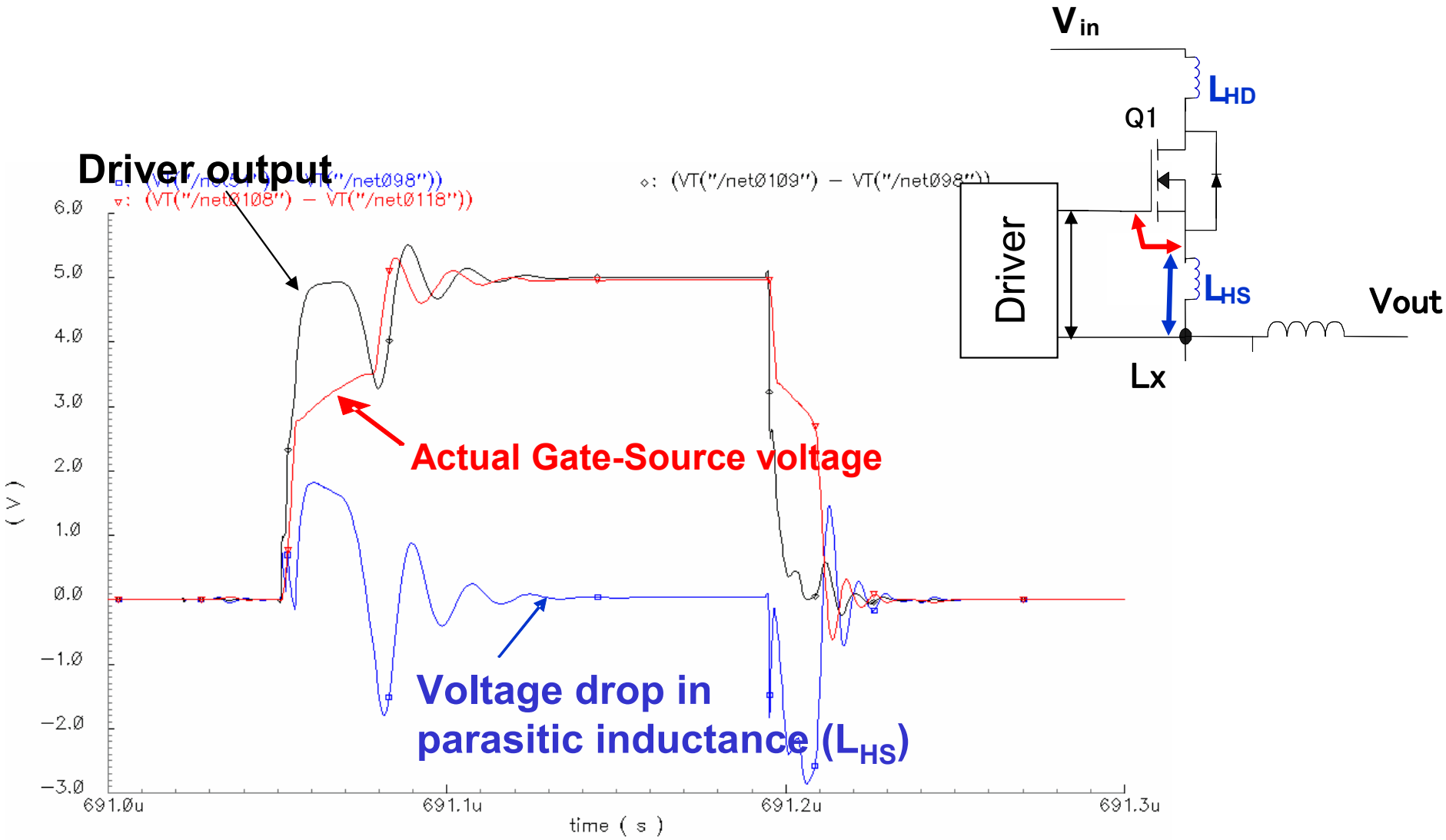
L_{HS}=0.44nH



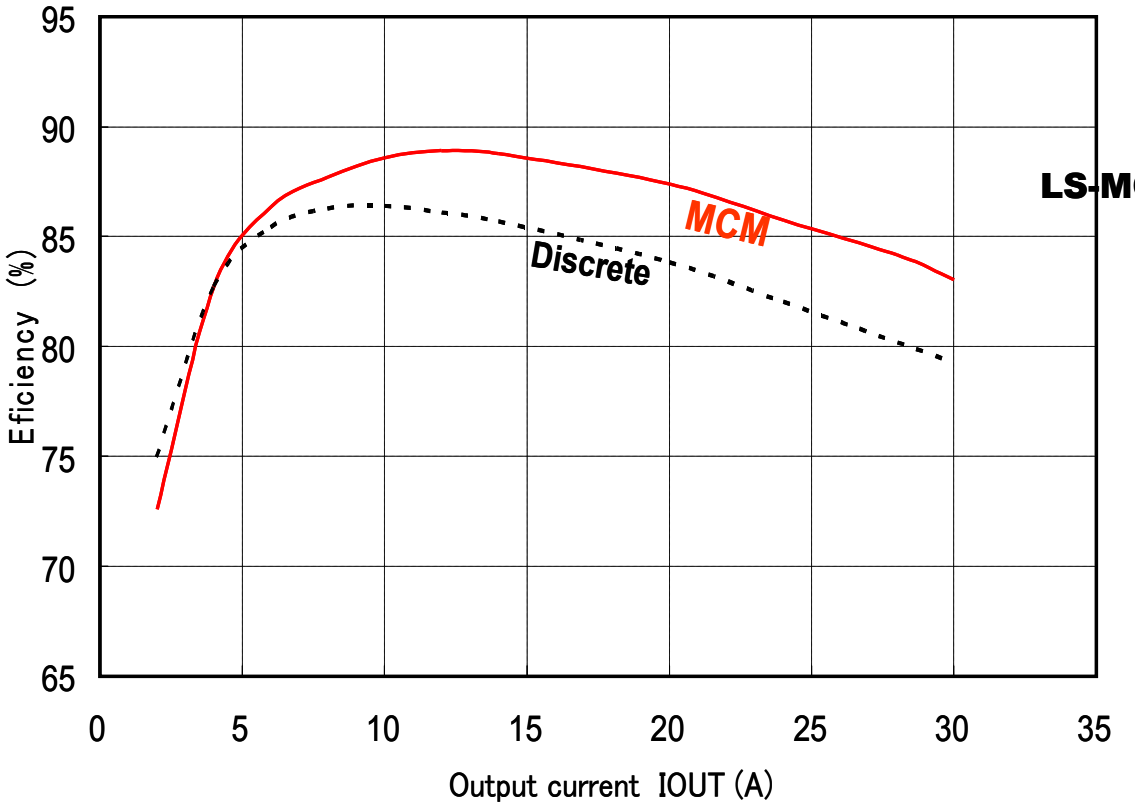
L_{HS}=1.24nH



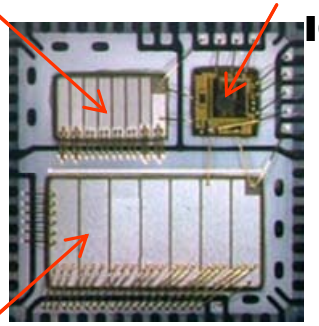
Why turn-on delay occurs?



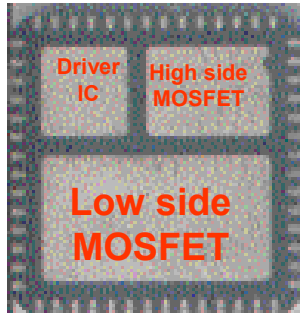
PWSiP: Multi-Chip-Module

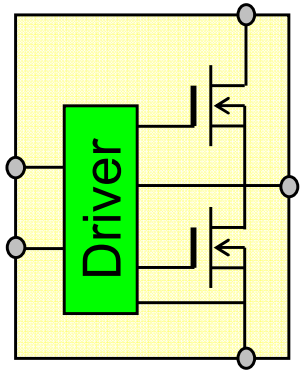


Top view



Bottom view





シリコン限界への挑戦

Theoretical Silicon limit of Switching Speed :

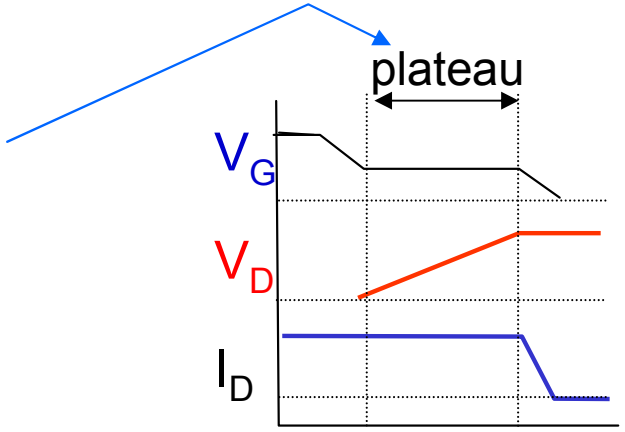
$$t_f = \frac{\text{Stored Charge}\,(Q_{str})}{\text{Drain Current}\,(I_D)}$$

Conventional Switching

Theoretical limit:

$$t_f = \frac{Q_{str}}{I_D}$$

$$\text{Mirror period} = \frac{Q_{gd}}{I_G}$$



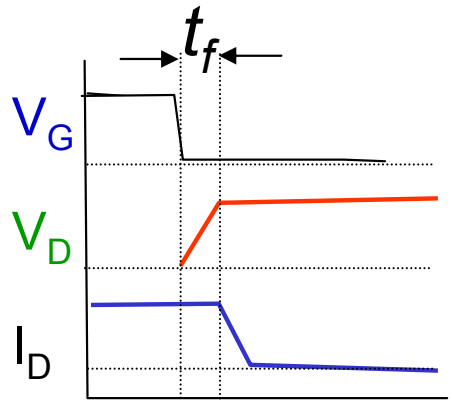
$$P_{loss} = R_{on} I_D{}^2 + V_A I_D \frac{Q_{gd}}{I_G} f + \frac{1}{3} Q_{str} V_A f$$

Major loss

Ideal MOSFET Switching

Theoretical limit:

$$t_f = \frac{Q_{str}}{I_D} \qquad \text{Mirror period} = \frac{Q_{gd}}{I_G} = 0$$



$$P_{loss} = R_{on} I_D{}^2 + \frac{1}{3} Q_{str} V_A f$$

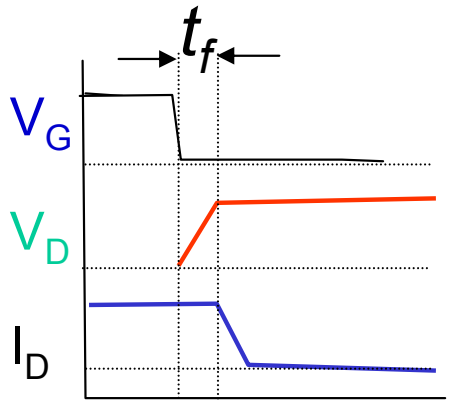
→ Low Impedance gate drive is a key technology
to supply a large gate current
to eliminate mirror period.

Ideal MOSFET Switching

New FOM = $R_{on}Q_{str}$

Theoretical limit:

$$t_f = \frac{Q_{str}}{I_D} \qquad \text{Mirror period} = \frac{Q_{gd}}{I_G} = 0$$

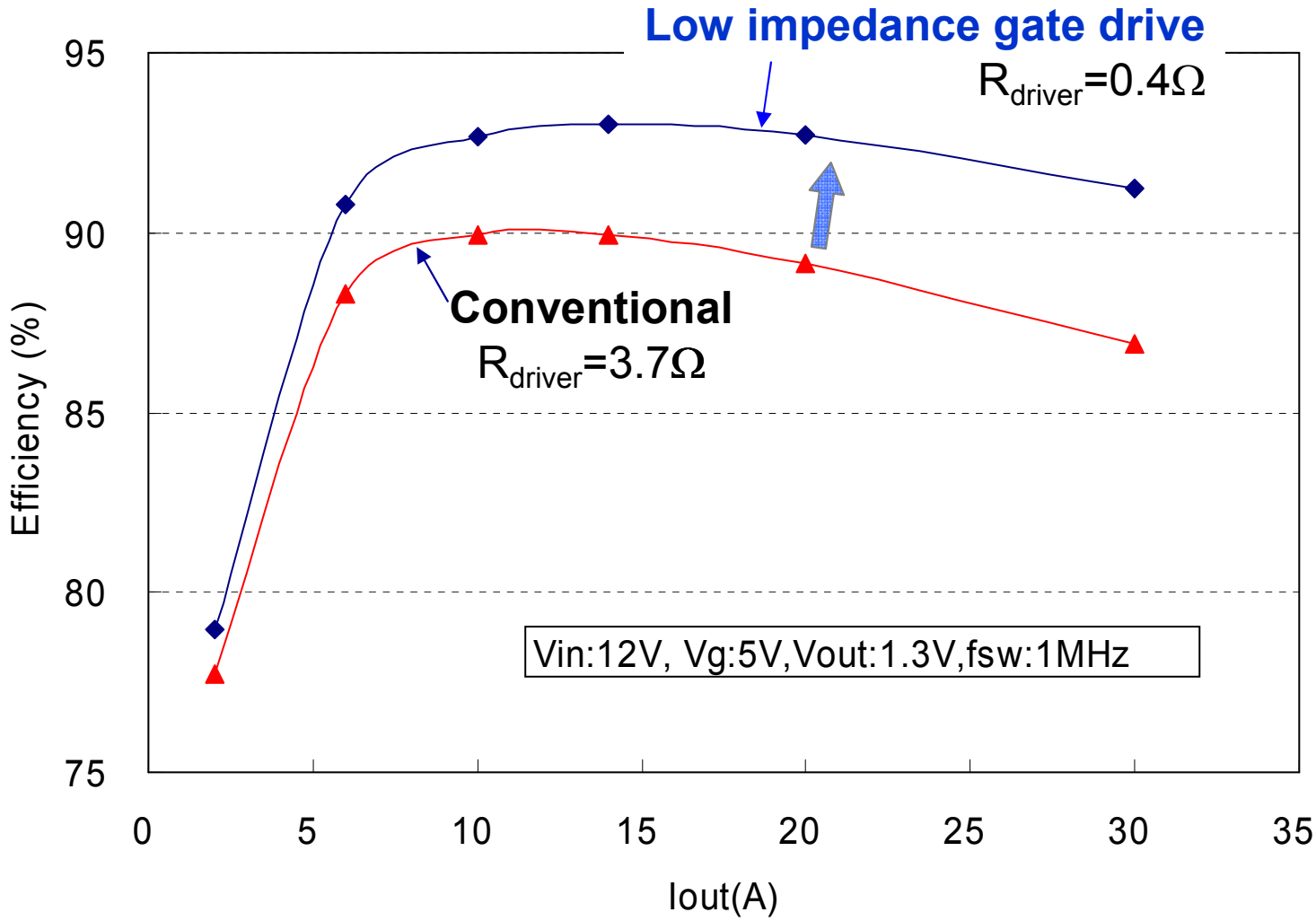


$$P_{loss} = R_{on} I_D{}^2 + \frac{1}{3} Q_{str} V_A f$$

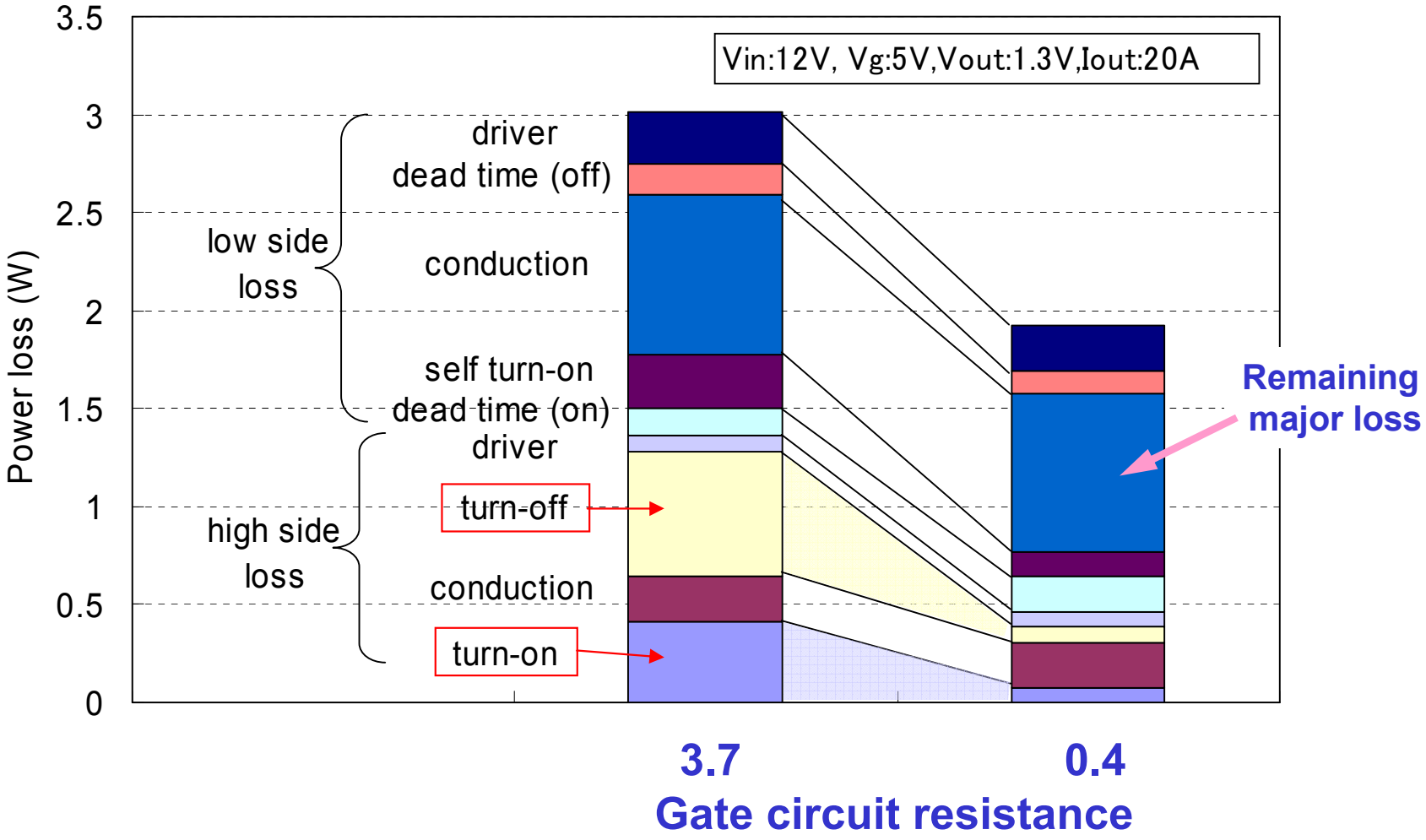
$$= R_{on} I_D{}^2 + \frac{1}{3} Q_{str} V_A f \geq 2\sqrt{\mathbf{R_{on}Q_{str}} \frac{1}{3} I_D{}^2 V_A f}$$

New FOM

Effect of low impedance gate drive

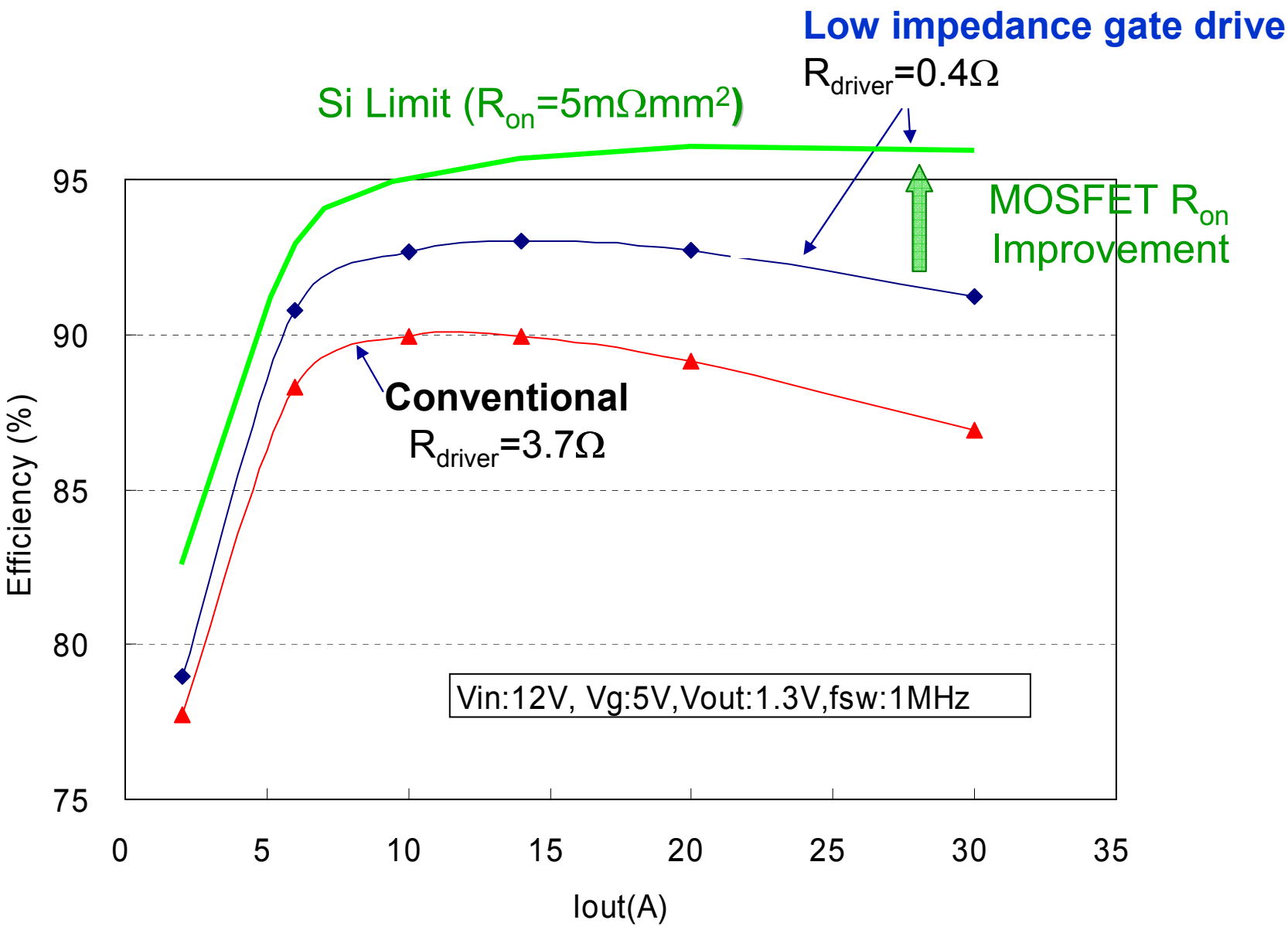


Power loss analysis

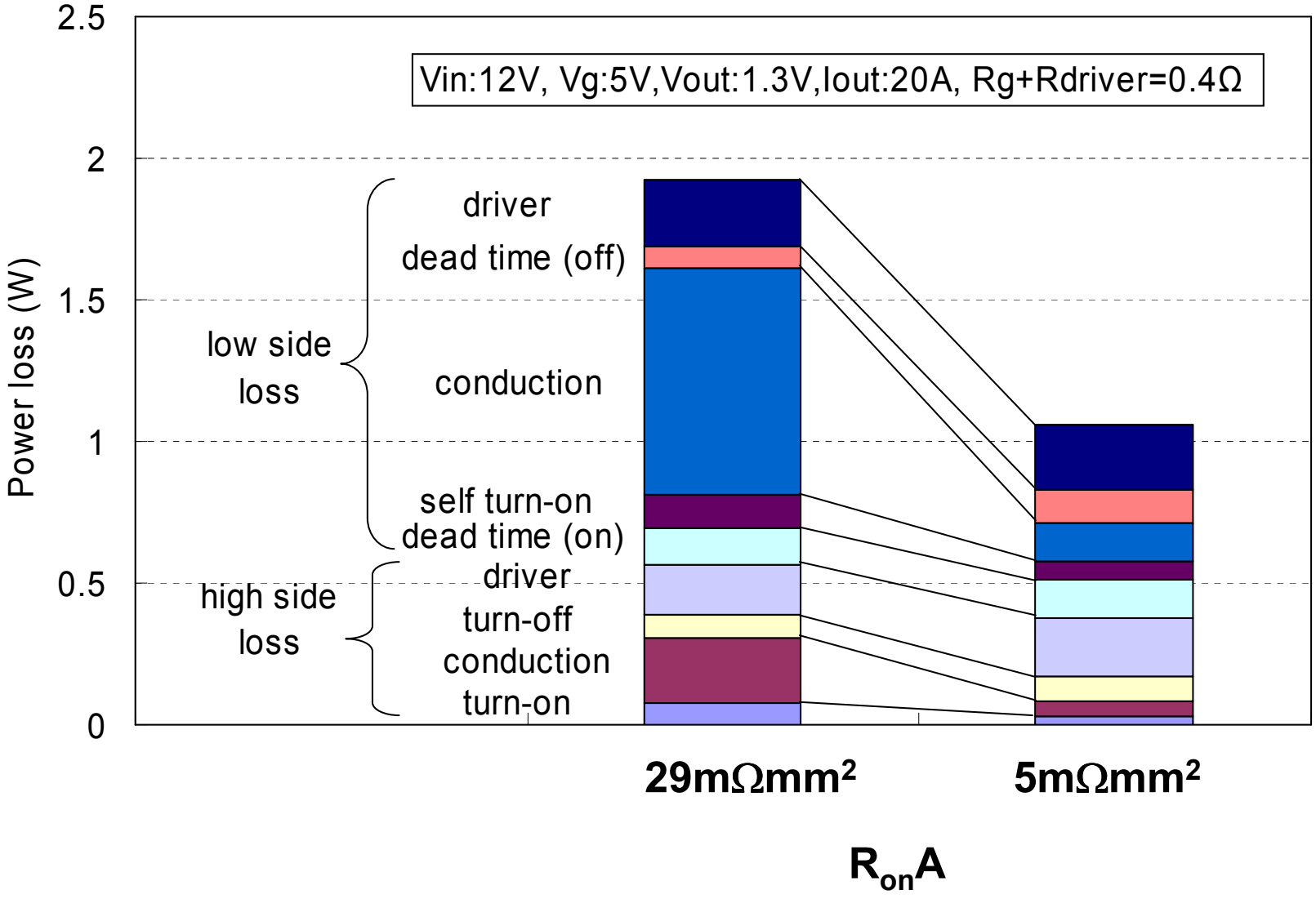


Low impedance gate drive reduces the switching loss of high side MOSFET

Predicted Silicon Limit Efficiency

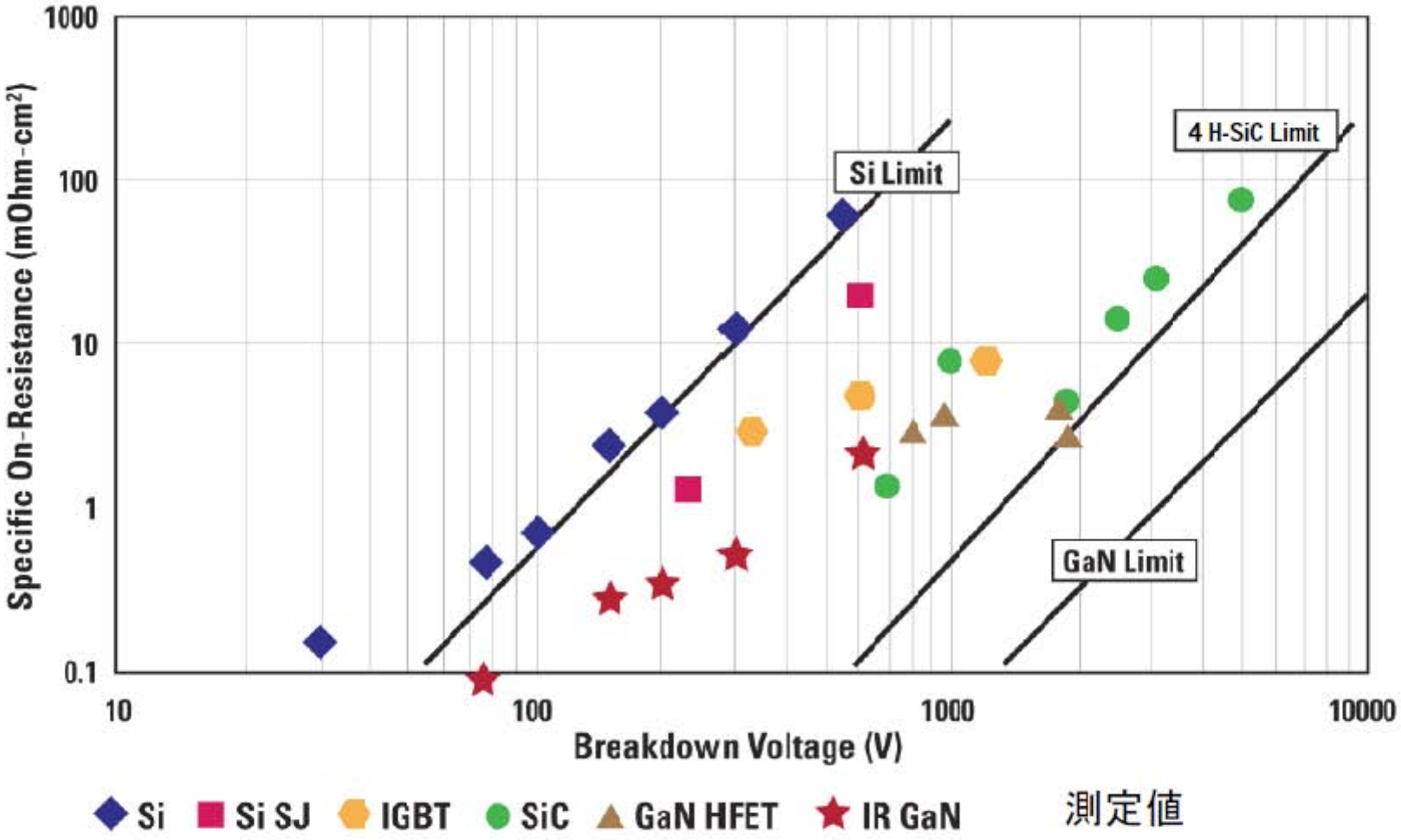


Power loss analysis



飛躍的にパワー・デバイスのFOMを改善

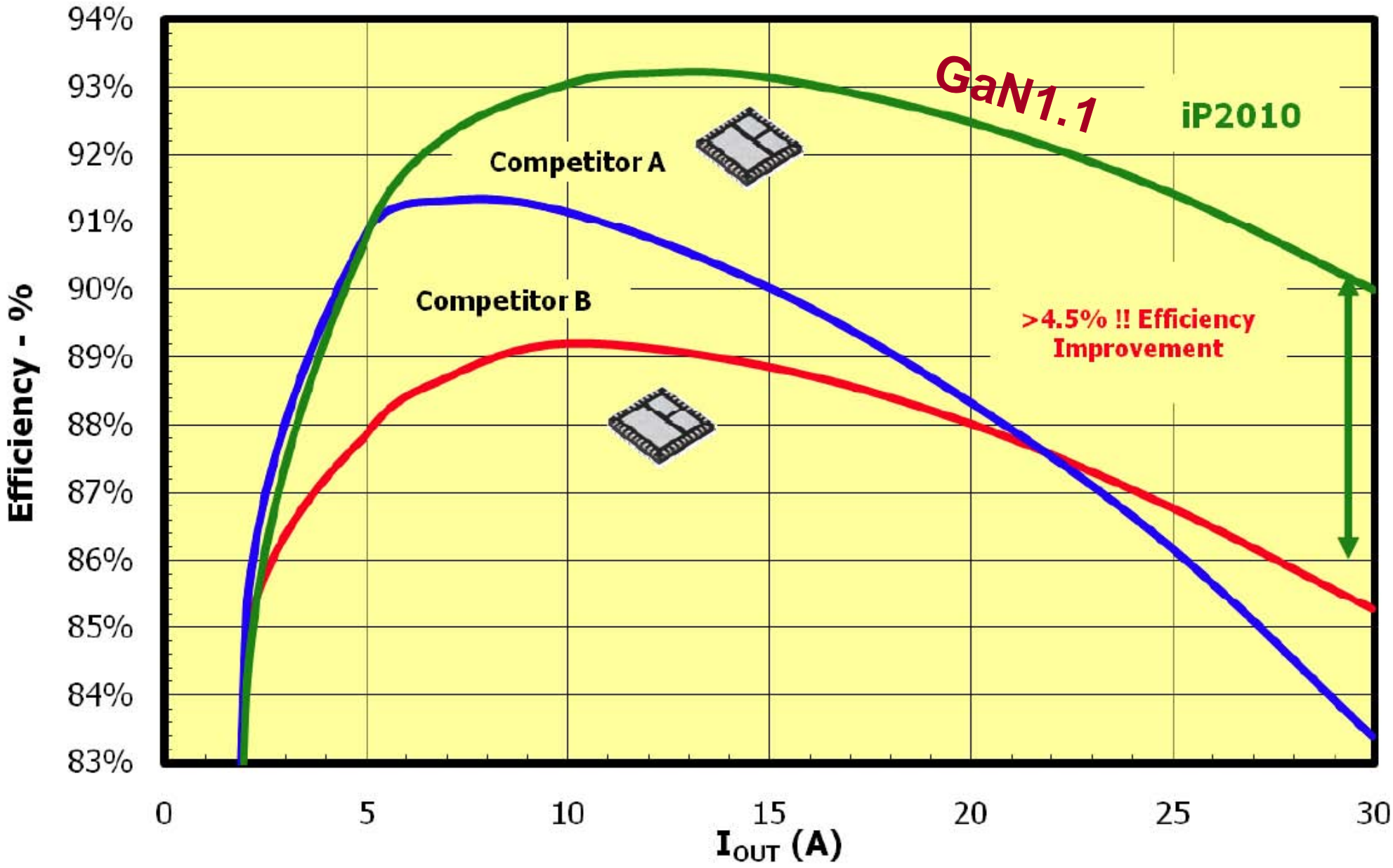
Si, SiC とGaN のR_{on} 比較



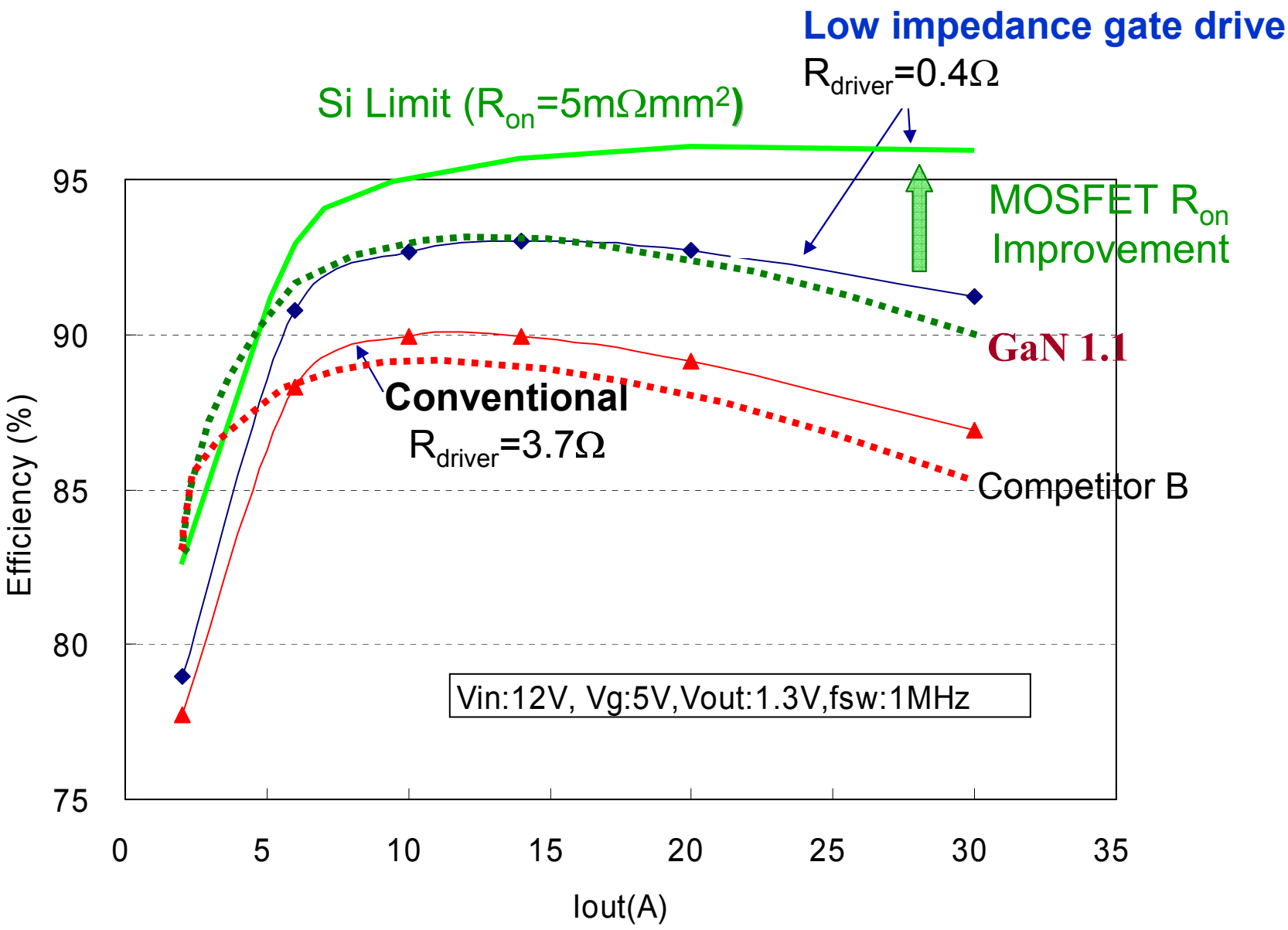
臨界電界 : Si = 20 V/μm , GaN = 300 V/ μm

Ref: N. Ikeda et.al. ISPSD 2008 p.289

Vin=12V, Vo=1.2V @ 600KHz



Predicted Silicon Limit Efficiency



New FOM の導入

$$NFOM = R_{on}Q_{str} = R_{on}J \cdot Q_{str}/J = V_F T_s$$

理想的な場合:

$Q_{str}=\varepsilon E_C$

$Ron=4V_{BD}^2/\varepsilon\mu E_C^3$

$NFOM=4V_{BD}^2/\mu Ec^2 =4V_{BD}^2/BHFOM$

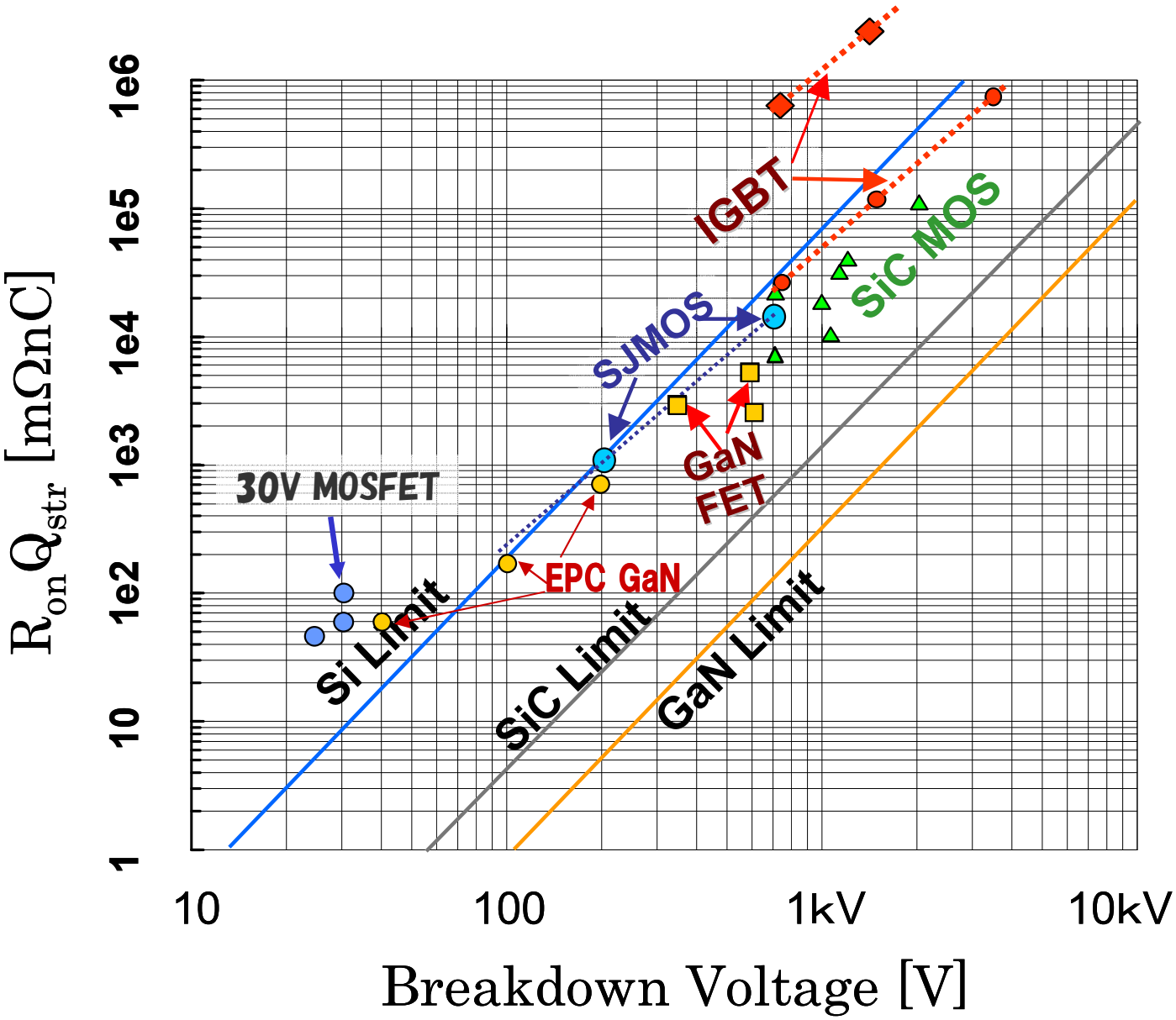
この場合、NFOMはBHFOMと逆比例。

NFOMは個々の素子で定義、BHFOMは材料で定義！

SiC と Si の比較

	SiC	Si
蓄積電荷(εEc)	$1.2x10^{13}q$(6倍)	$2x10^{12}q$
Switching速度Tsが同じになる電流密度	Siの6倍	1
R_{on}/V_{BR}^2	Siの280分の1	1
NFOM 同じTsのオン電圧	Siの46分の1	

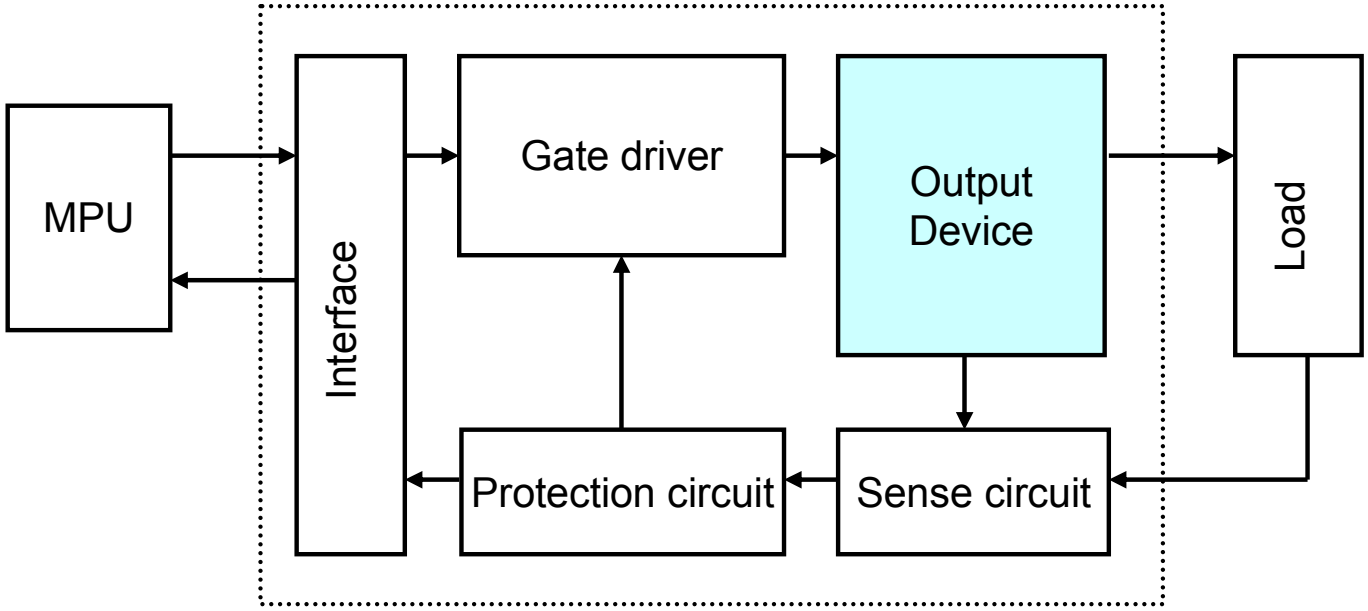
New FOM: $R_{on}Q_{str}$ for high speed switching



パワーIC（BCD技術）
－Single chip DCDC converter

インテリジェントパワーICの古典的定義

保護回路を設けて使いやすくする
マイコンで直接制御可能



システムパワーIC

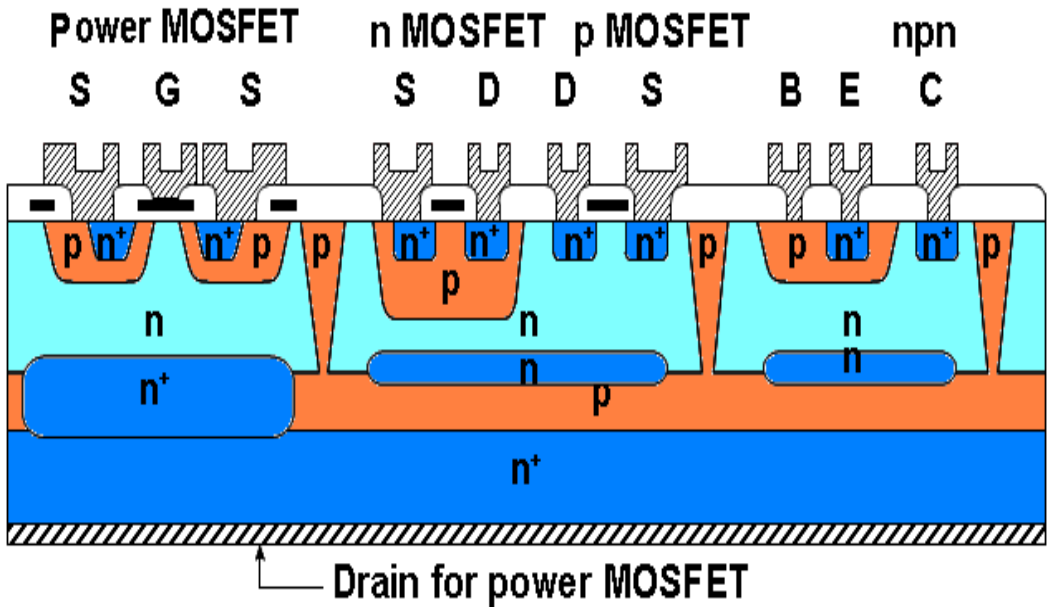
LSI優先

プロセッサやシステムLSIとの集積

パワー素子優先

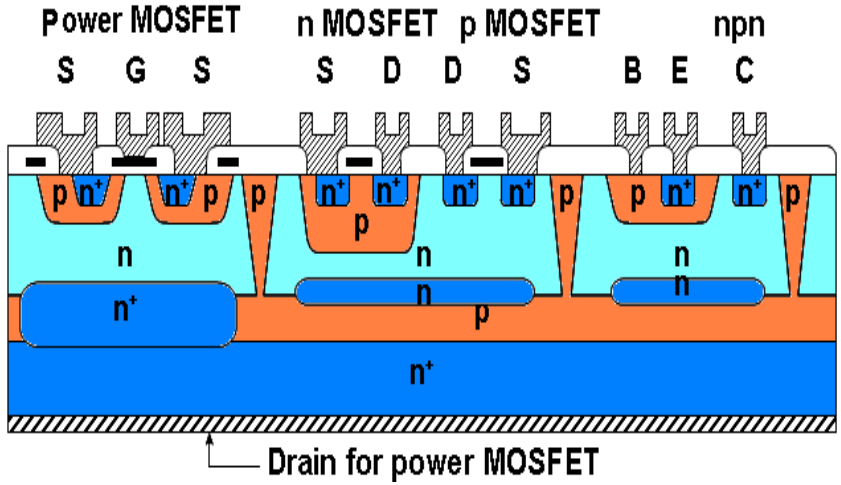
インターフェイス，保護回路，アナログなど
比較的小規模な回路との集積

- Smart Power Concept in early 1980's

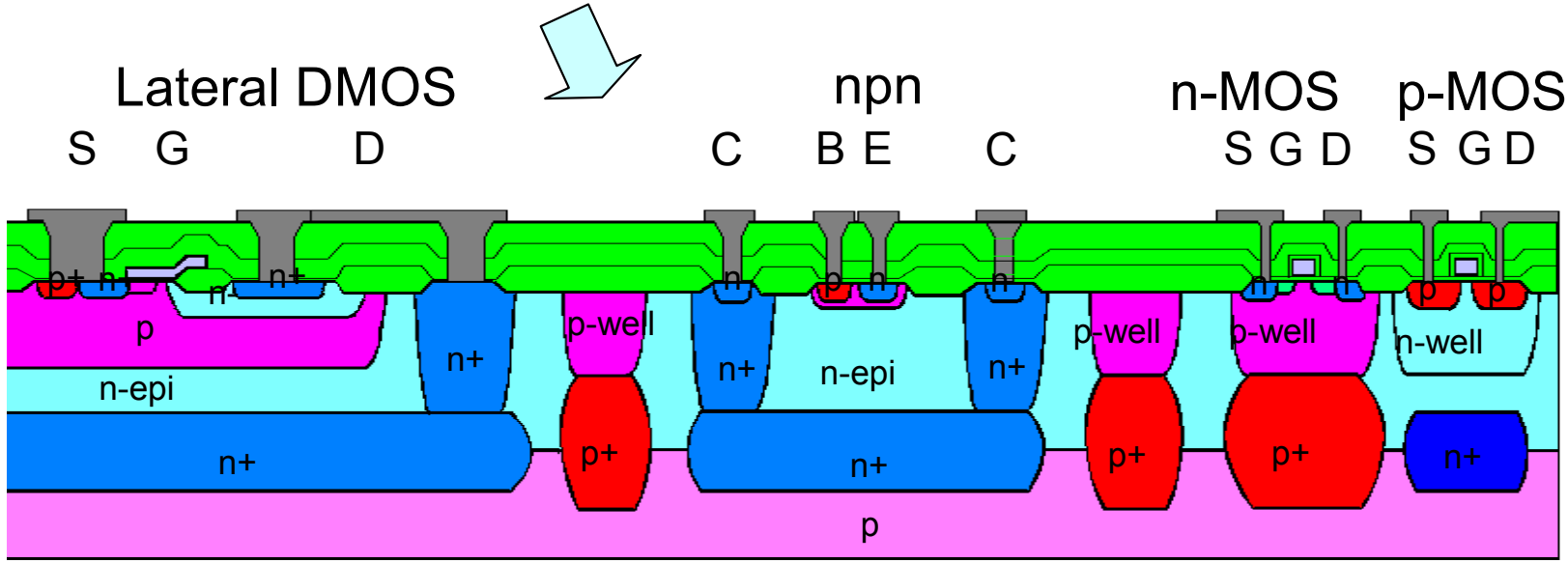


Smart Power　縦型DMOS + 制御回路

Smart Power: Vertical DMOS
has lost advantage.

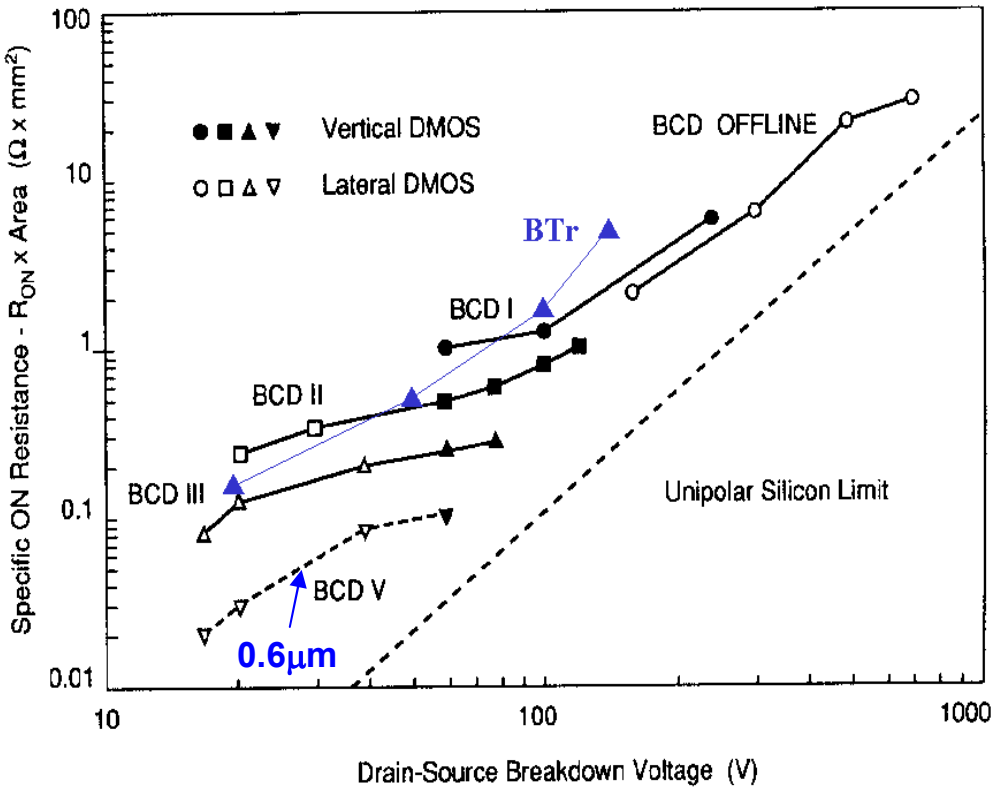


BCD: Lateral DMOS :
reasonable cost
large current
multi-output



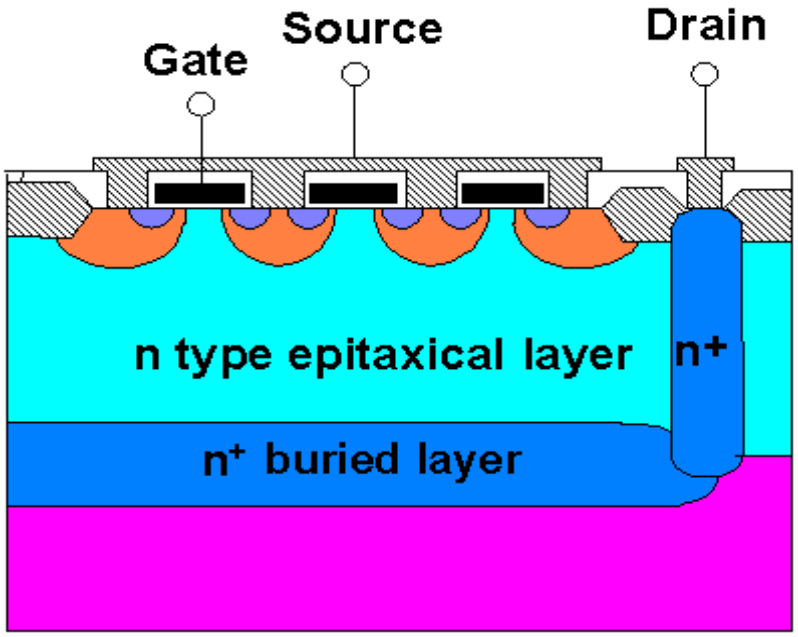
BCD技術　横型DMOS + 制御回路

- Smart Power Concept
- BCD Technology
  0.6μm design rule

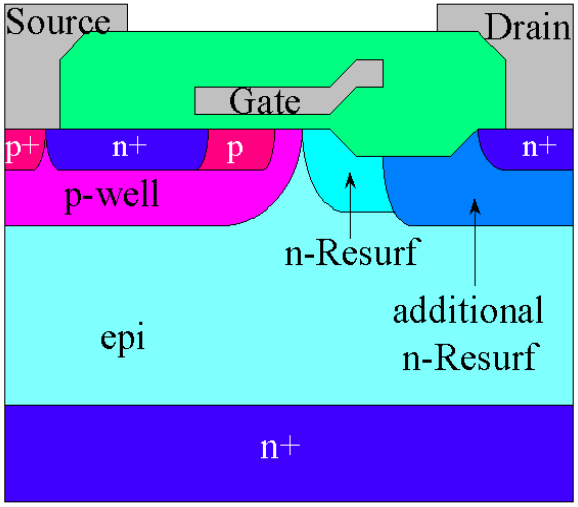


Vertical DMOSからLateral DMOSへの移行

- LDMOS: Rds(on) is simply reduced depending on design rule
- ゲート酸化膜が薄く二重拡散が困難

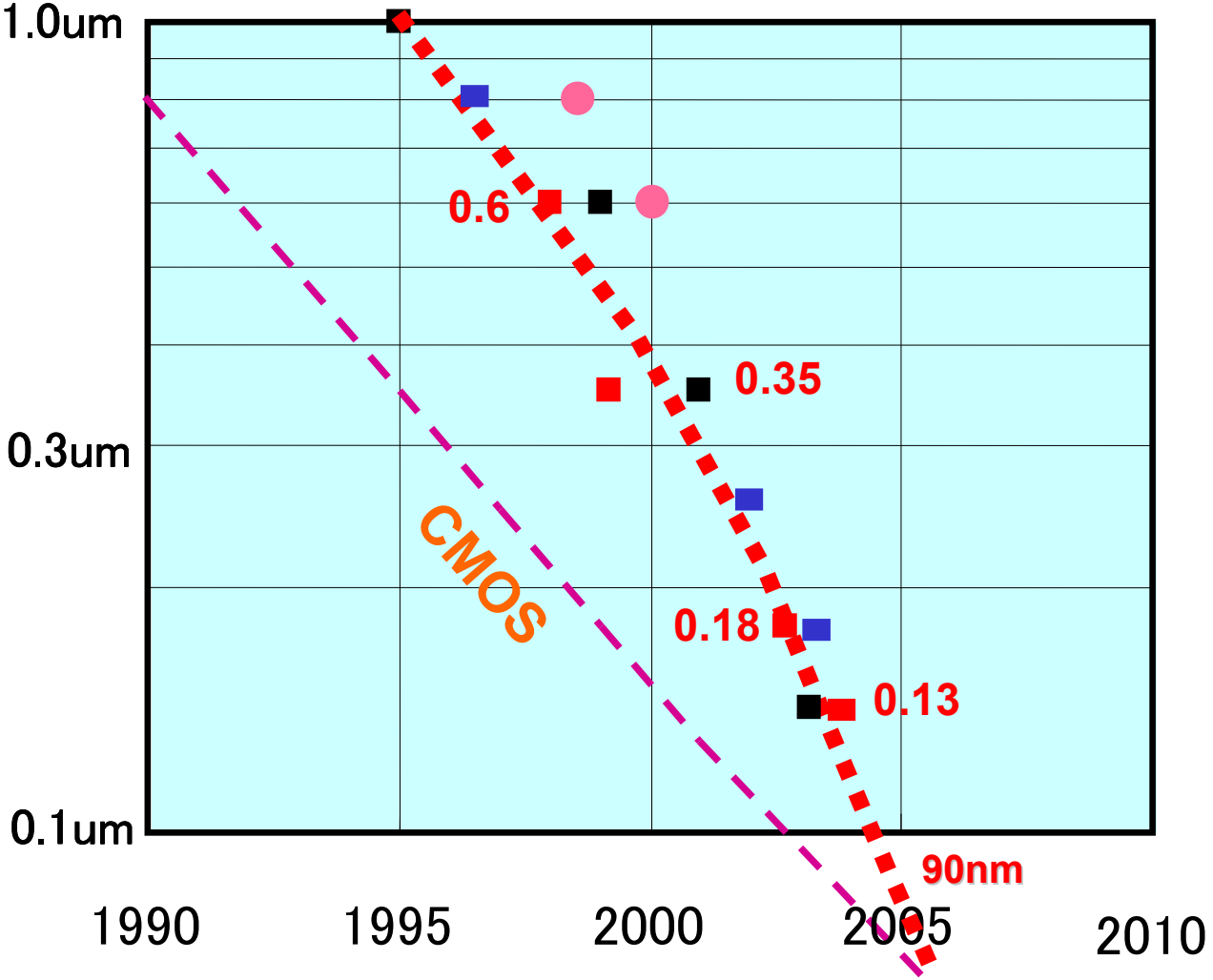


Up Drain vertical DMOS

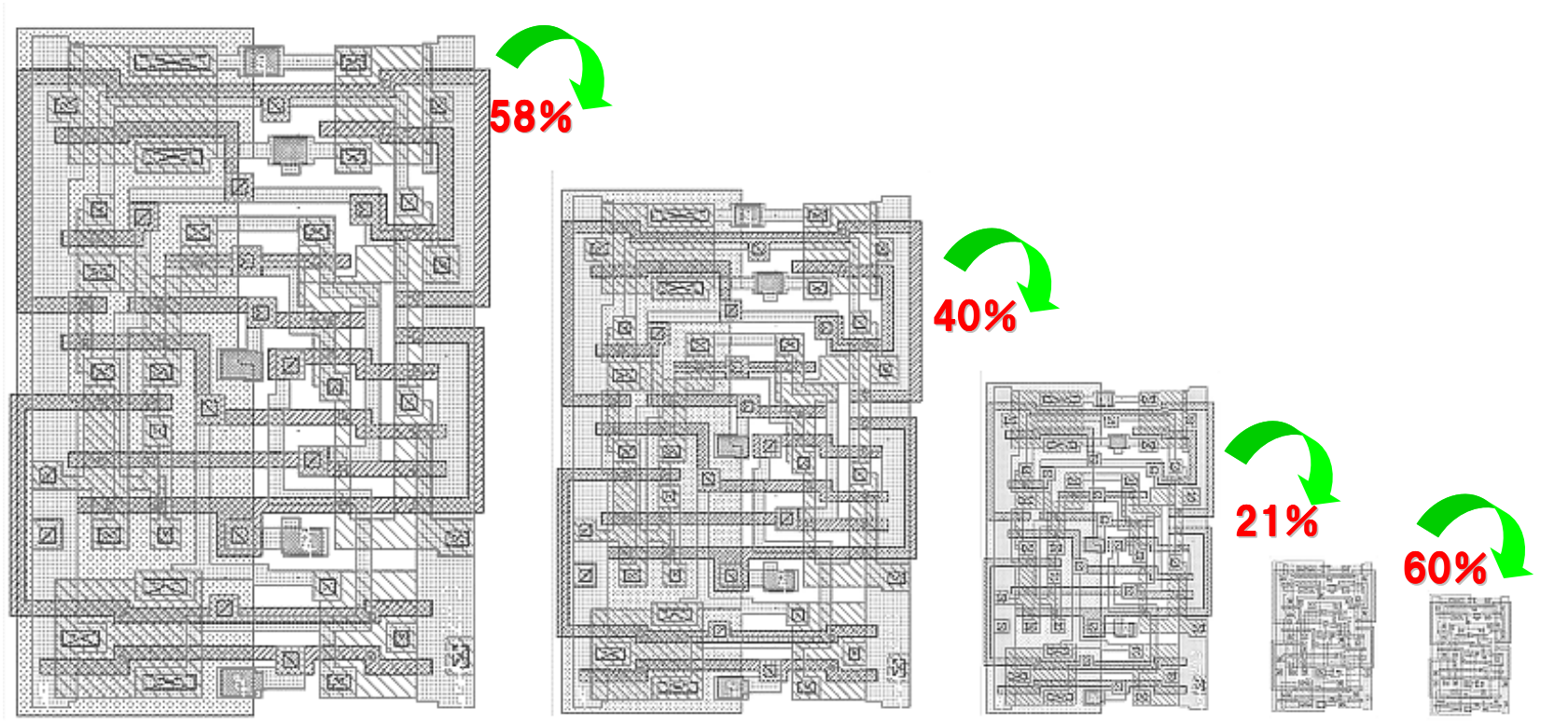


LDMOS

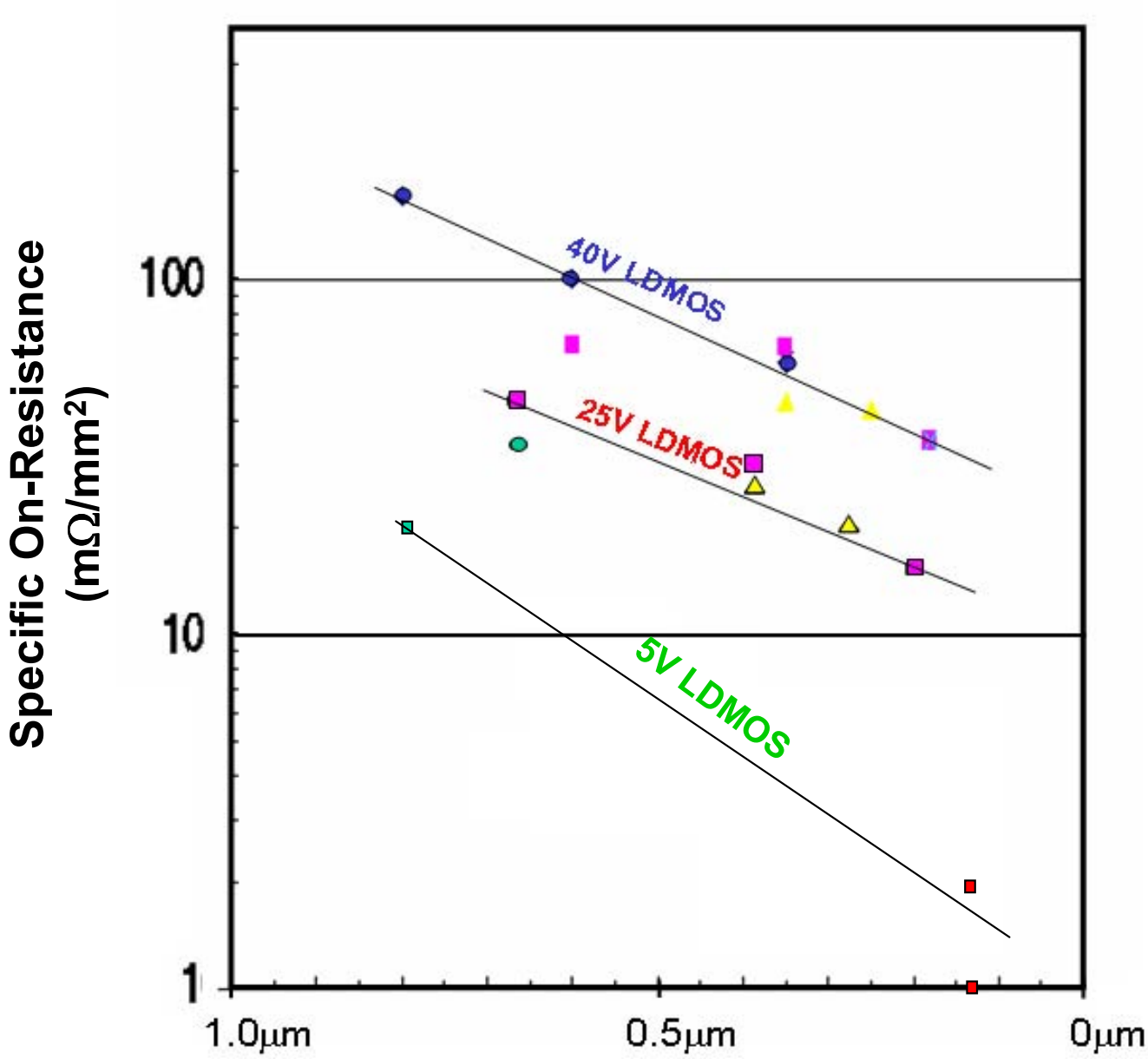
微細化するパワーICプロセス



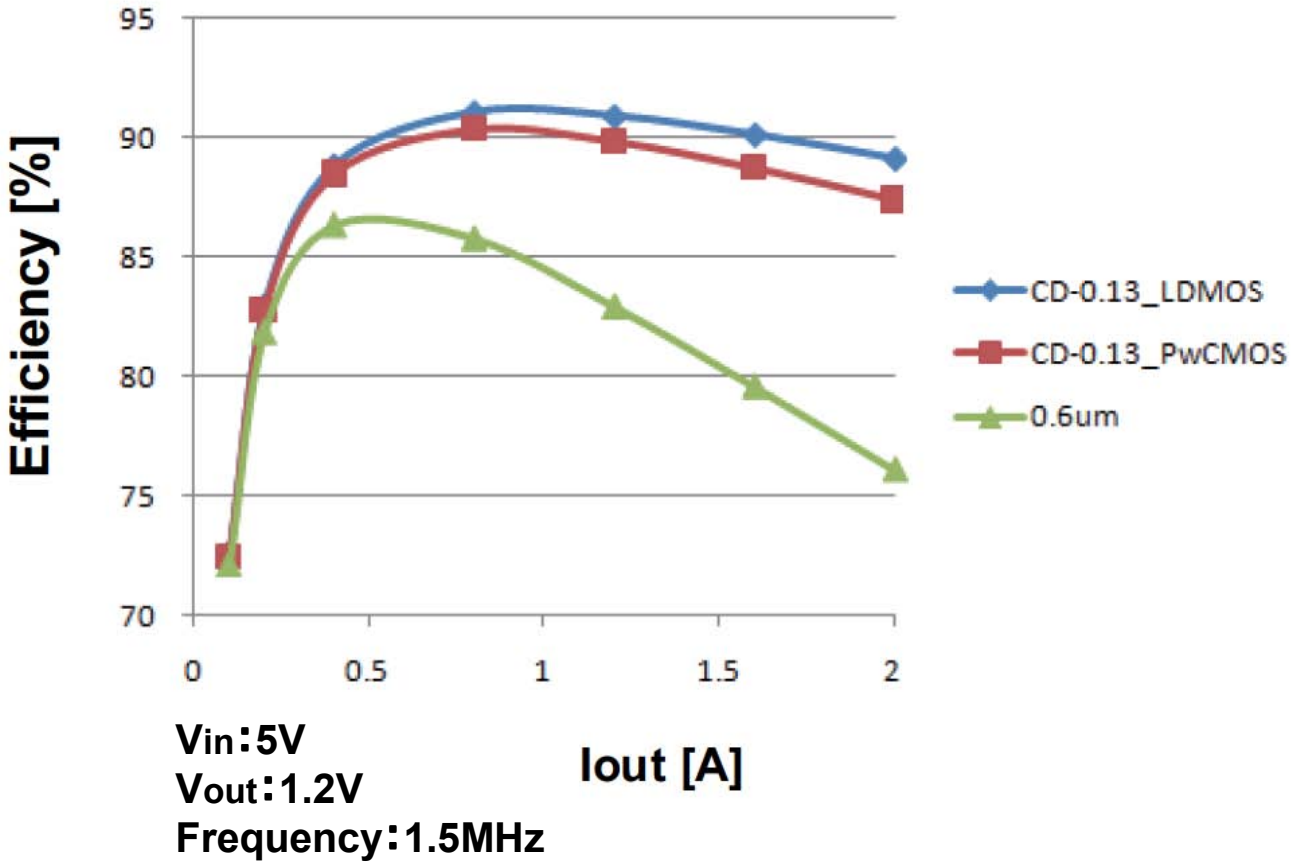
CMOS Logic area reduction



なぜ微細化なのか？

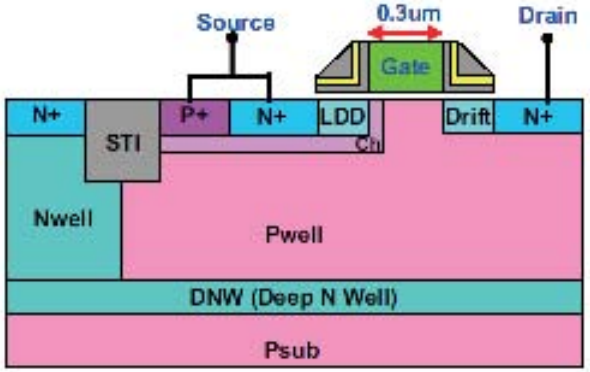

Specific On-Resistance
(mΩ/mm²)
100
10
1
40V LDMOS
25V LDMOS
5V LDMOS
1.0μm
0.5μm
0μm

0.13μmデザイン 8V LDMOS



Vin：5V
Vout：1.2V
Frequency：1.5MHz

ゲート長：0.3μm

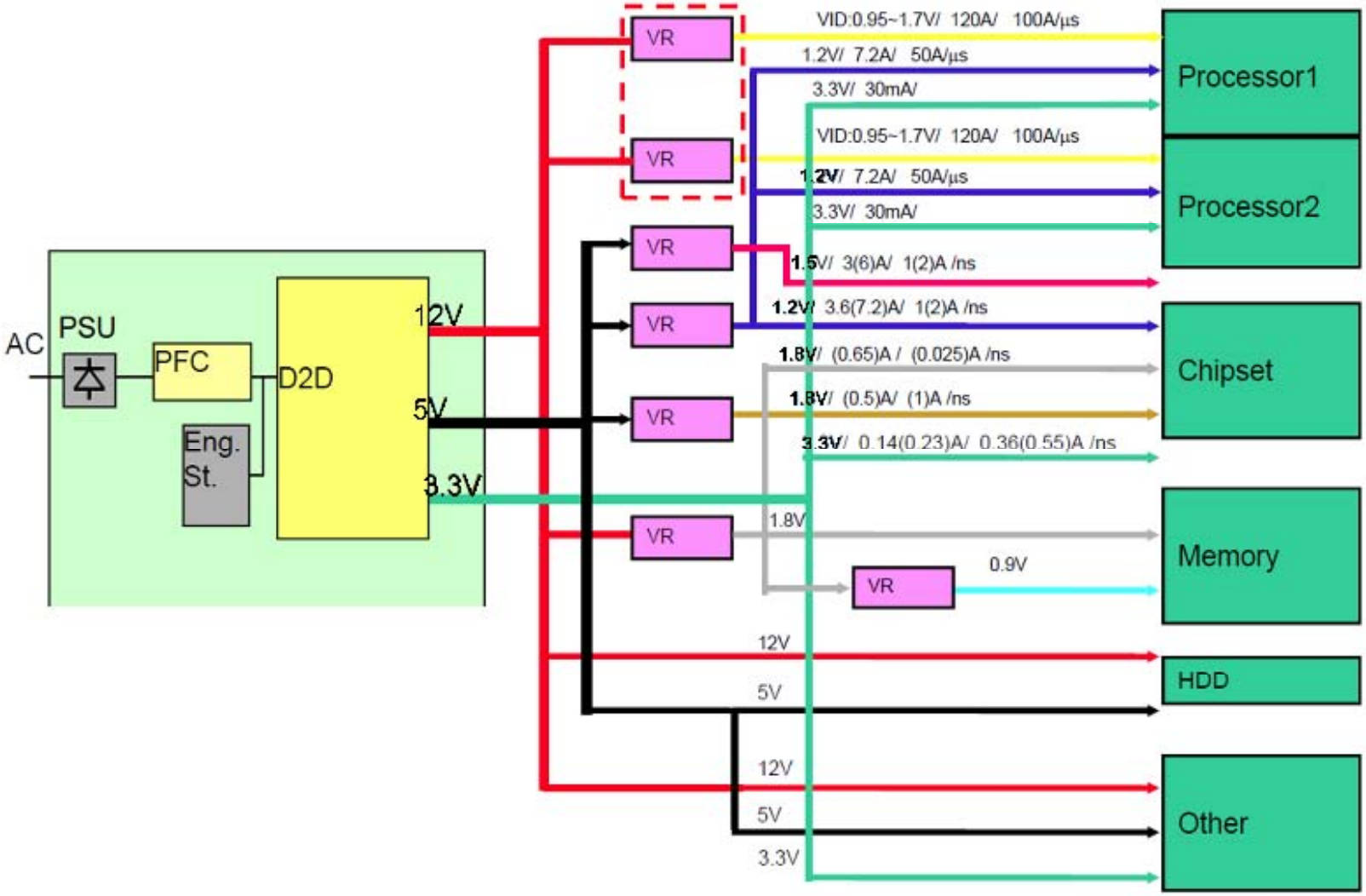


Tomoko Matsudai et al., ISPSD11, Hiroshima

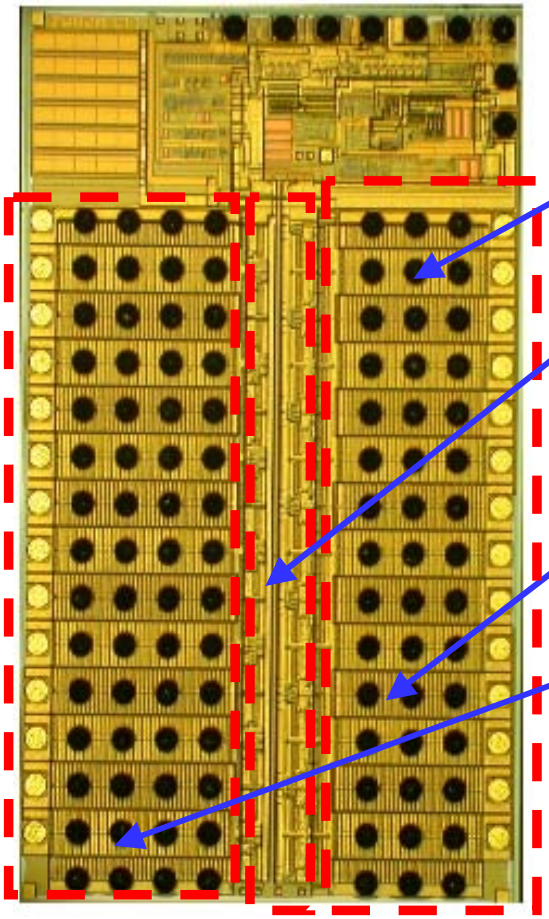
多種の電源電圧→電源の効率向上!!

Present Server Power Architecture

F. Lee PWRSoC'08



12V 10A DCDC Converter chip



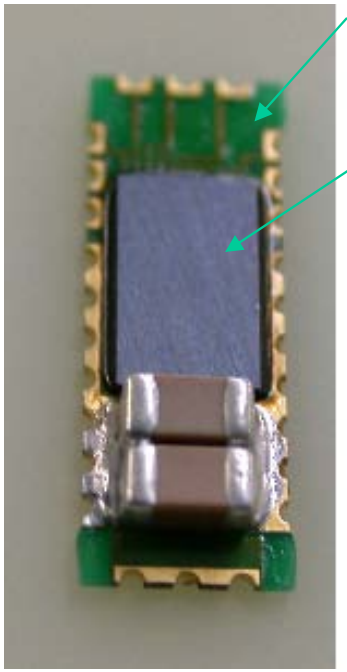
Bump ball

Driver Circuits

Pch LDMOS

Nch LDMOS

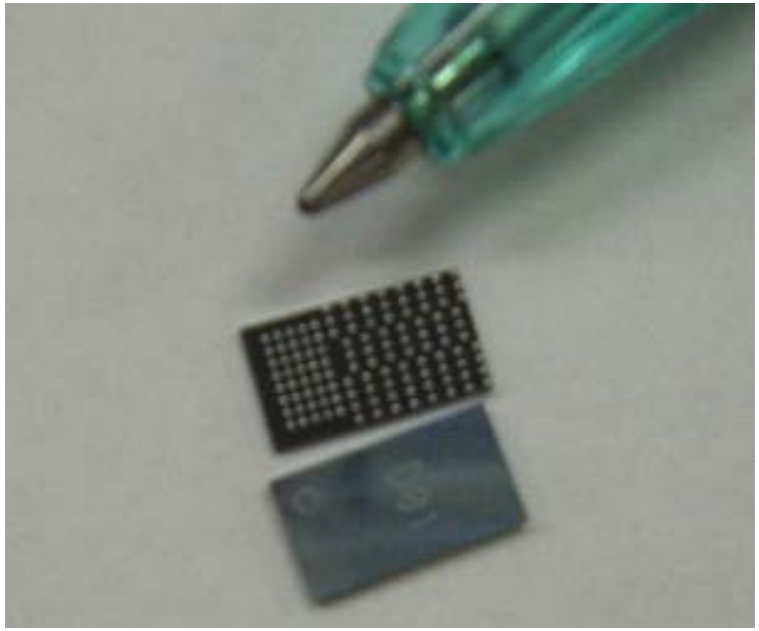
The chip size：20.3mm^2

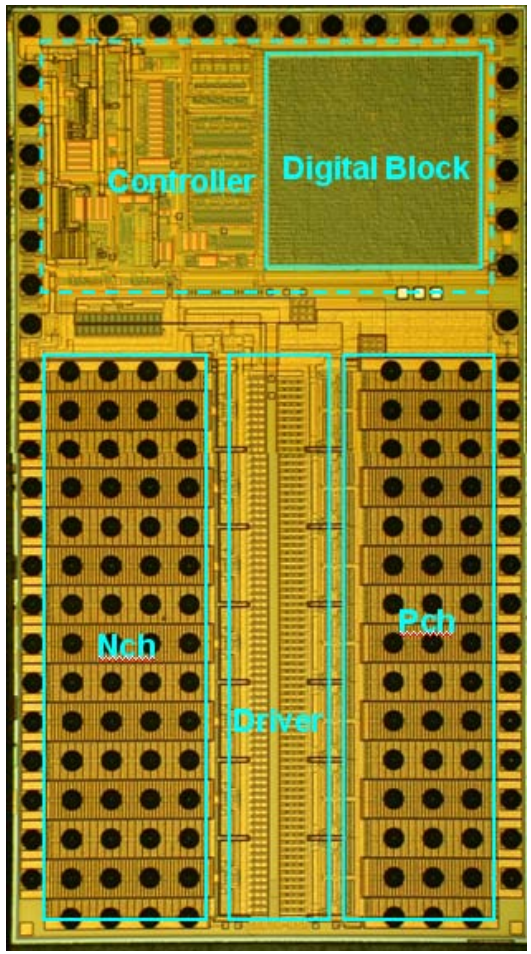


Evaluation PCB

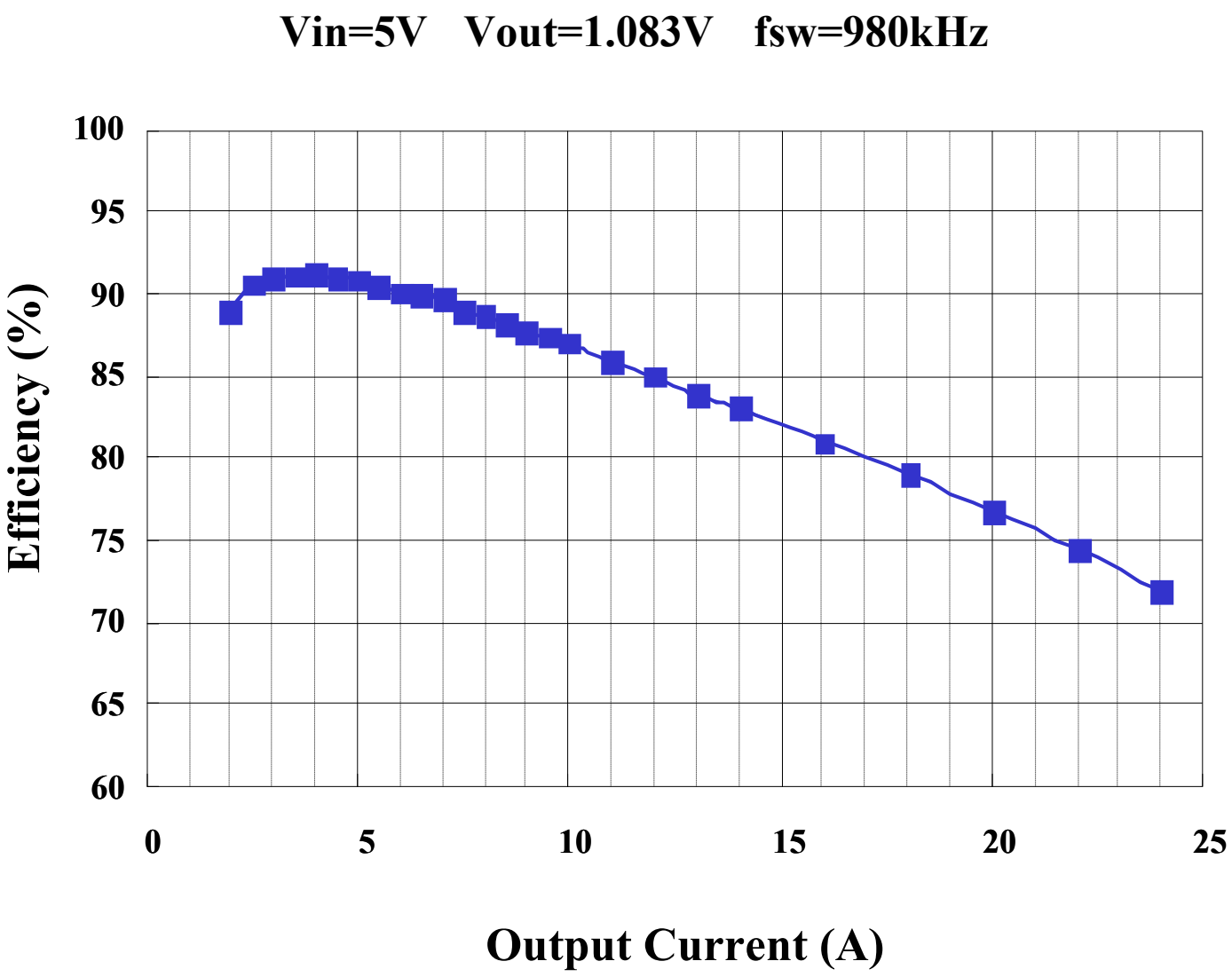
Chip

5V 20A 1chip DCDC Converter

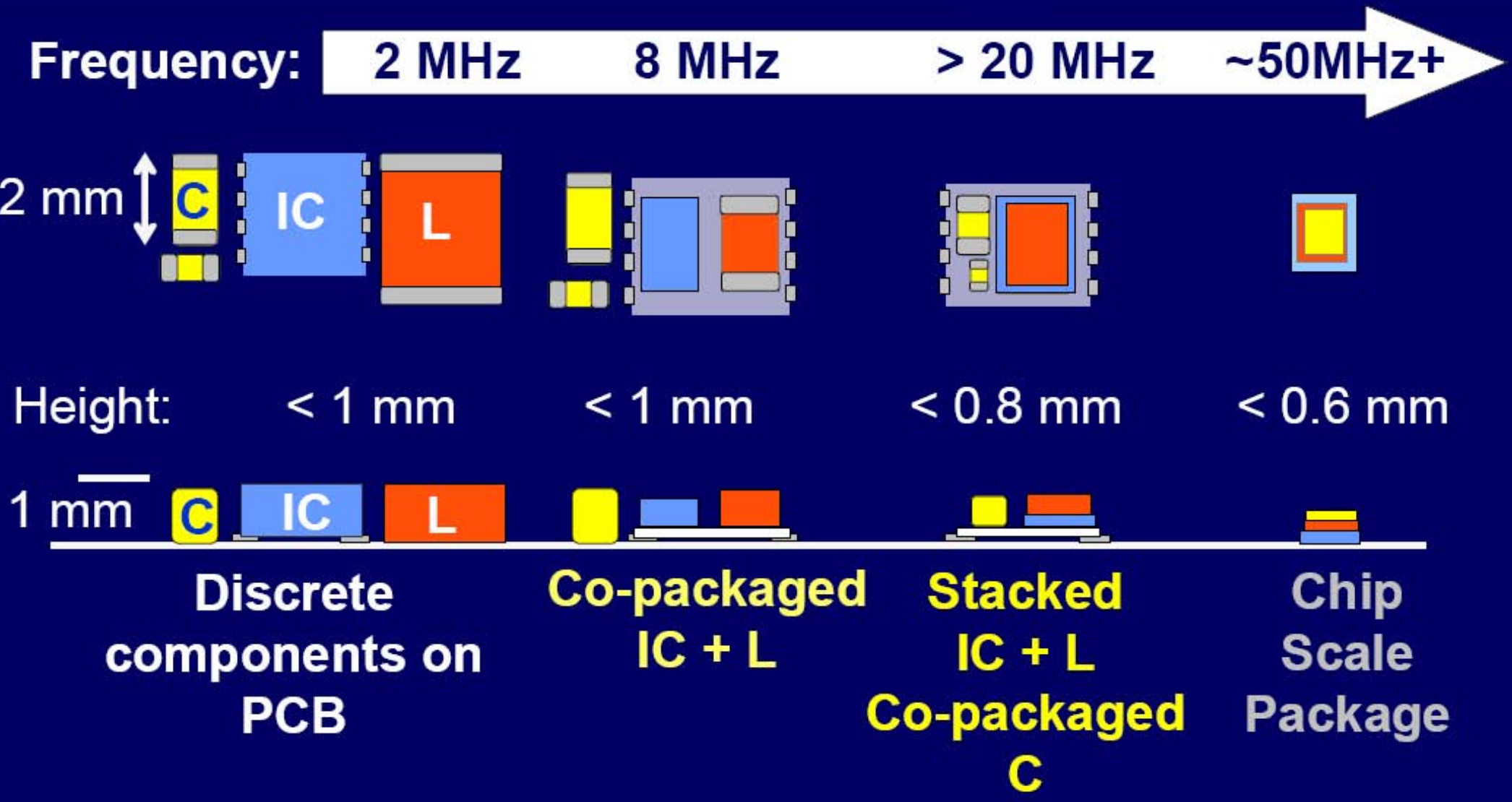




20A operation



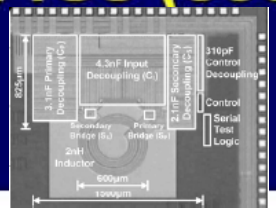
高周波化で小型になる電源



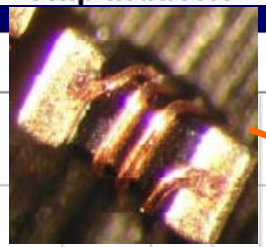
APEC2009 Plenary “Power Supply on Chip Has the Ship Come In?”
Cian O Mathuna, Tyndal National Institute

Multi-MHz Switched-Mode Converters on System ICs (350nm to 90nm)

Tyndall National Institute



Off-chip Air-Core Chip Inductor



Novel Multi-Phase Topology
2nH Coupled Inductor
Air-Core

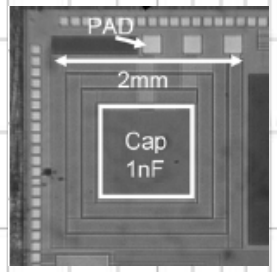
- Intel 2004
- U Minnesota 2008
- KU Leuven 2008
- U Tokyo 2007
- Freescale 2006
- U Brit Columbia 2007
- NXP 2008
- ST Microelectronics 2008

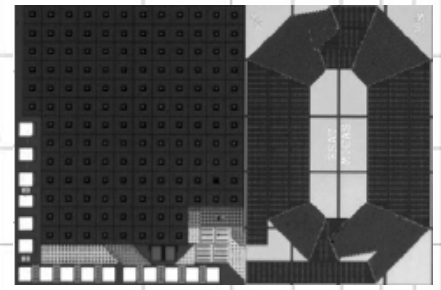
Efficiency %

100
90
80
70
60
50
40
30
20
10
0

10
100
1000
10000

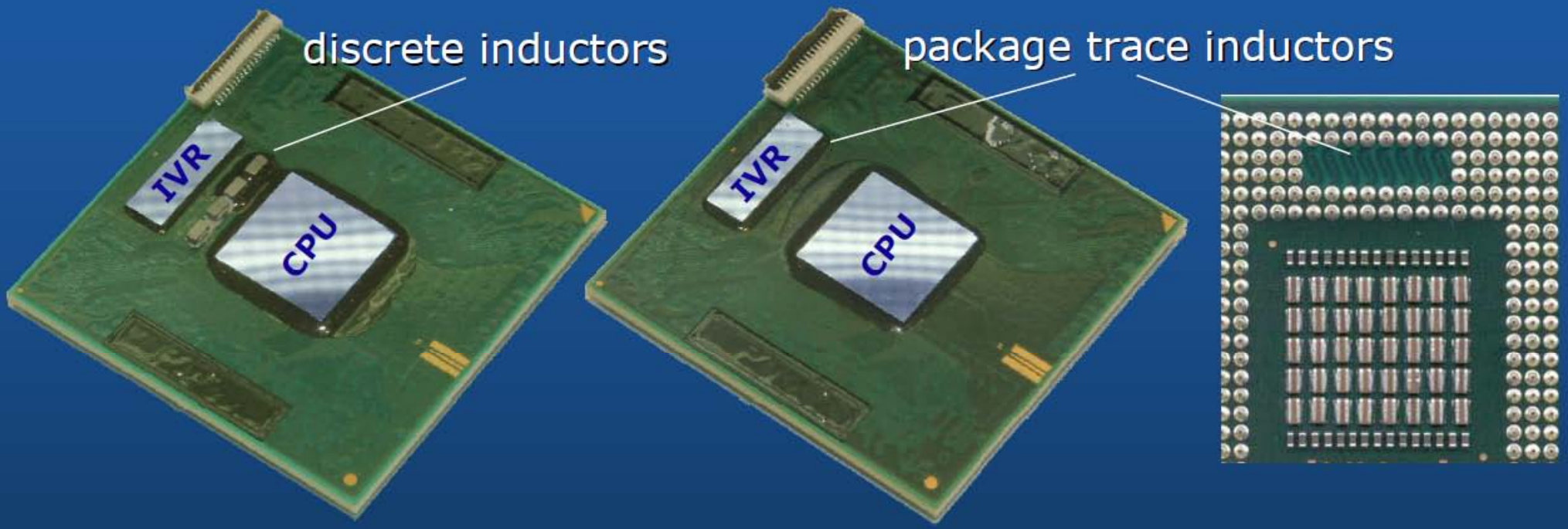
Switching Frequency (MHz)





On-chip
Air-core Inductor

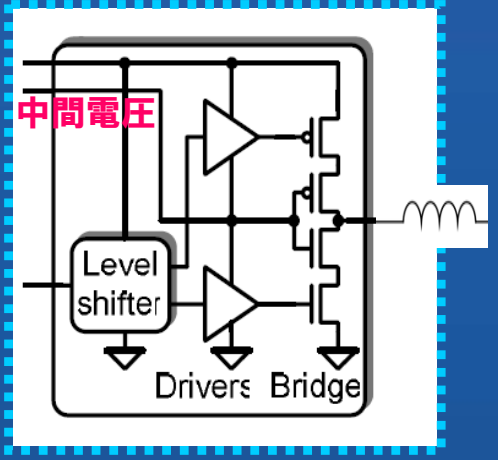
Package-Integrated VR with Intel® Core™2 Duo Processor



- Vin=3.3V, Vout=0...1.6V (VID), 10MHz...100MHz, TDC=50A / 75A peak, size=37.6mm², 130nm CMOS
- Inductors: 0508-size discrete powdered iron core or package-trace air core

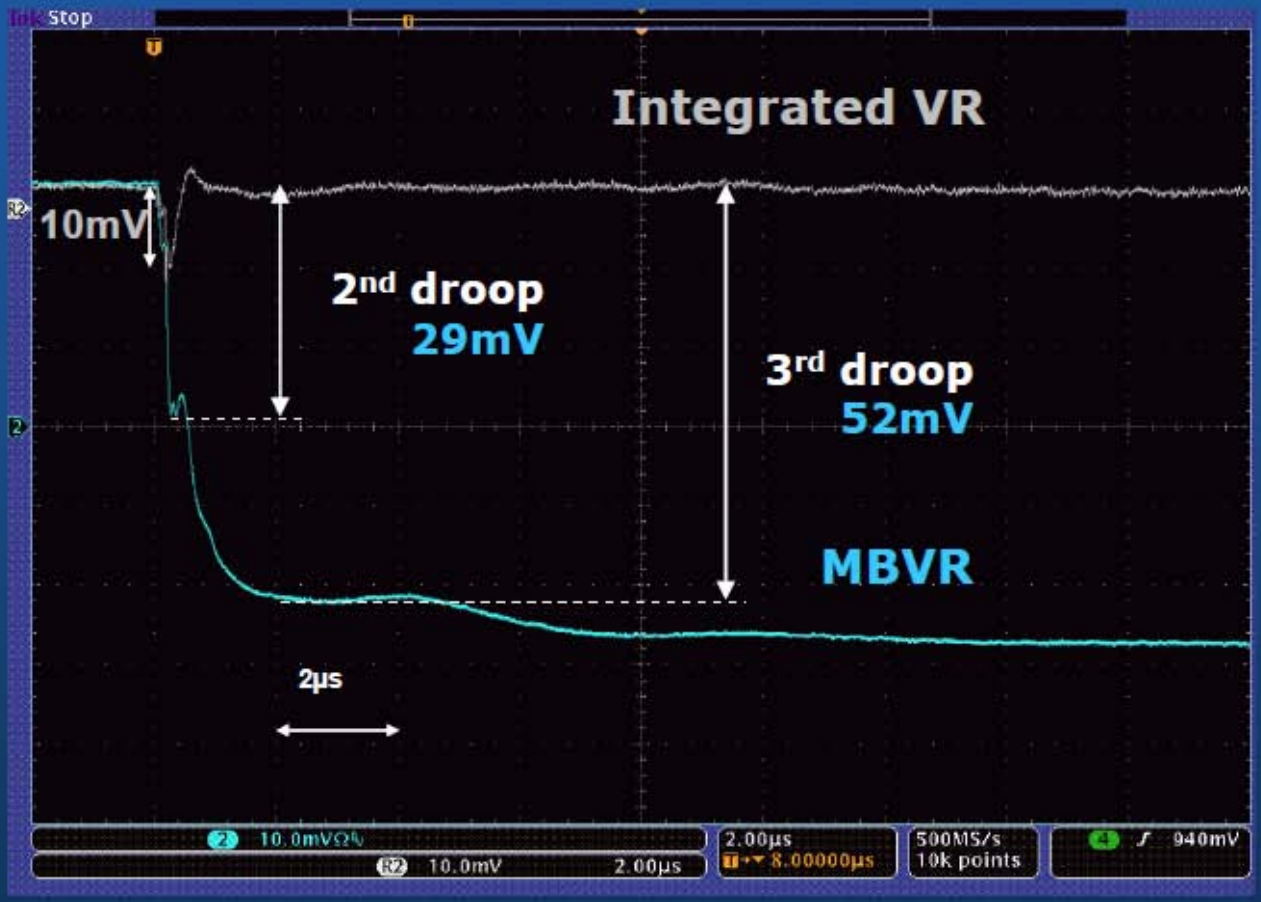
APEC 2010 Special Session 1.4.2
A 60MHz 50W Fine-Grain Package Integrated VR Powering a CPU from 3.3V
G. Schrom, F. Faillet, J. Hahn, Intel, Santa Clara, CA

Package-Integrated VR Proof of Concept



- Advantage of on-package 2nd VR stage
  - Single 3.3V input, lower current going into the package
  - 2-stage conversion is more efficient
  - Near-load VR allows fast response, reduced load line
- VR test chip on the CPU package (MCP)
  - VR chip/w cascode bridges manufactured in 130nm CMOS
  - 60MHz switching frequency allows miniaturization
  - Mounted on modified CPU package/w package trace inductors or powdered-iron core inductors

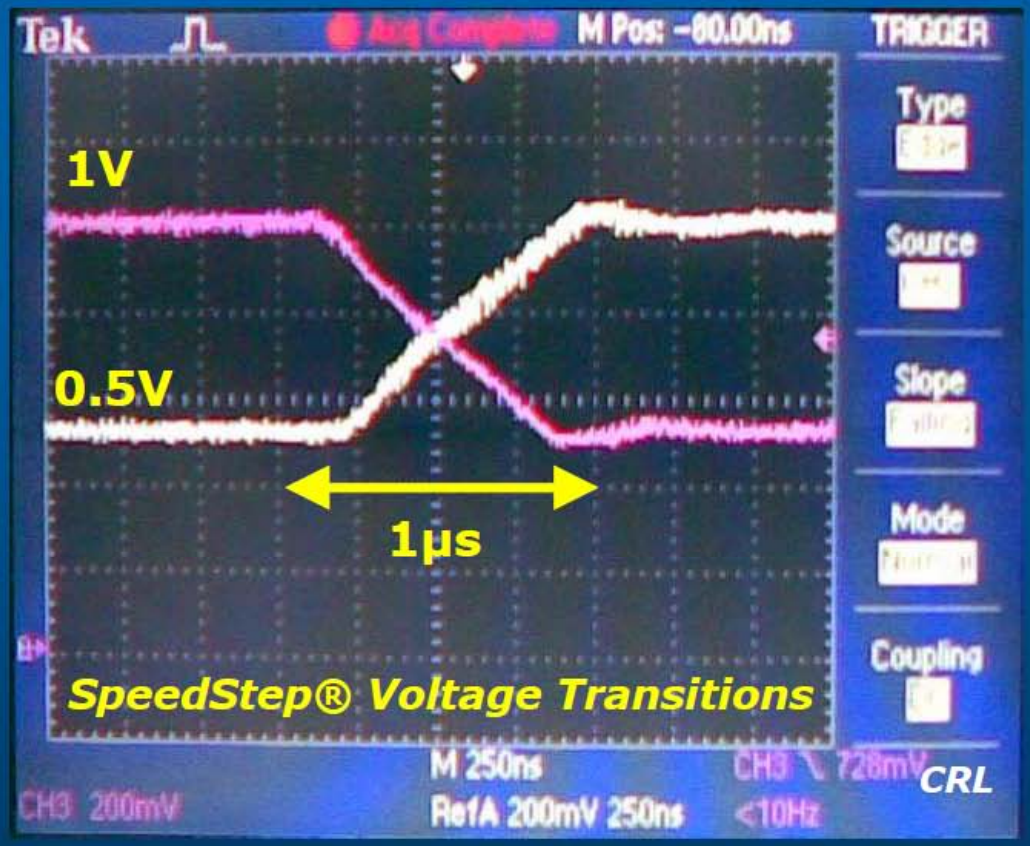
Transient Performance

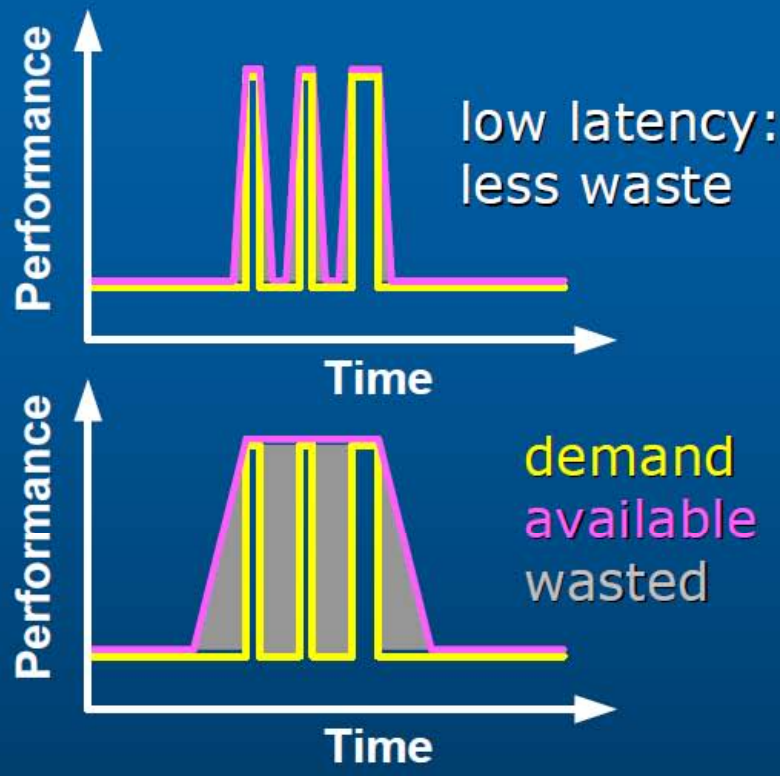


Load-line set to "0"

- 2nd droop: reduced to 10mV
- 3rd droop: eliminated
- Reduced load line saves power

Output Voltage Ramp Rate





- Fast output voltage ramp rate: >500mV/µs
- Time-domain fine-grain power management saves power

シリコン限界が取りざたされる中、

シリコンパワー素子は更なる性能向上が見込まれ、

エネルギー需要を支えるために
今後ますます重要になって行くと
予想されます。

今日のファイルはここからDownloadできます。
http://www.ne.jp/asahi/capri/ocean/