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Theoretical Investigation of Silicon Limit Characteristics of IGBT

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Abstract IGBTs have evolved rapidly as key power devices for high power application. The present paper theoretically investigates, for the first time, the silicon limit of IGBTs, and proposes a new trench gate IEGT/IGBT, realizing the theoretical limit. It is shown that almost one order of magnitude improvement in on-resistance will be expected. The author also proposes, for the first time, a theory to achieve extremely large short-circuit withstanding capability.

I. THEORY OF SILICON LIMIT OF IGBTs

This section proposes a theory to achieve the lowest forward voltage drop in IGBTs, adopting asymmetrical conduction: "all of the current flows by electrons." Holes contribute only to the conductivity modulation. From the assumption of no hole current flow, the following equations are valid under the high injection condition (n = p).

$$J_p = qD_p \frac{\partial p}{\partial x} - q\mu pE = 0 \qquad \text{----Eq.(1)}$$

$$J_n = J_{Total} = 2 \times qD_n \frac{\partial n}{\partial x} \qquad \text{----Eq.(2)}$$

$$E = \frac{kT}{q}\frac{1}{n}\frac{\partial n}{\partial x} \qquad \text{---- Eq.(3)}$$

The condition is satisfied by assuming that the carrier density distribution is approximately a linearly decreasing function from cathode to anode as shown in Fig.1. The current density - voltage relation of the silicon limit IGBT can be derived by integrating Eq.(2) with boundary values n_0 and n_W , and using the equations shown below [1]:

$$D_n = \frac{a}{n+b}, \quad J=qD_E n_0^2/Q, \quad V_F = V_i + V_{diff},$$

$$V_i = (kT/q)\ln(n_w/n_0), \quad V_{diff} = (kT/q)\ln(n_0 n_w/n_i^2)$$

$$V_F = \frac{2kT}{q}\ln\left[\frac{1}{n_i}\left\{\left(\sqrt{\frac{QJ}{qD_E}} + b\right)\exp\left(\frac{JW_N}{2qa}\right) - b\right\}\right] + R_{ch}J, \qquad \text{---Eq.(4)}$$

where R_{ch}, Q and W_N denote the channel resistance, the p-emitter dose and n-base width, respectively. a and b are constants (a=3.7e18, b=9.39e16). See Fig.1 for the definition of n_o and n_W.

Calculated current-voltage (J-V) curves are shown in Figs. 3-5, comparing with those of conventional IGBTs. The proposed asymmetrical conduction IGBTs drastically improve IGBT characteristics.

II. NEW IGBTs FOR ENHACED INJECTION EFFICIENCY

The author proposes a new IGBT/IEGT structure, shown in Fig.2, to realize extremely high electron injection efficiency in MOS gate structure. If the trench to trench distance (mesa width) is comparable to the thickness of the inversion layer, the two channel inversion layers on the both trench side walls merge and constitute a high concentration N-type layer in the narrow mesa, serving as a barrier for holes. If the mesa width is less than 40nm, the induced electron density is greater than $1\text{x}10^{17}\text{cm}^{-3}$ (see Fig.6), realizing over 0.9 electron injection efficiency, Γ_e in the MOS gate structure. The calculated V-I curves by TCAD, shown in the figures 3,4 and 5 well agree with the above theory although a discrepancy is seen for 4.5kV devices. The proposed narrow mesa IGBT realizes a low forward voltage even with the p-emitter of very low injection efficiency. Figure 7 shows forward voltage at 500A/cm^2 as a function of Γ_e. For practical application, Γ_e of 0.8 is sufficient and extremely narrow mesa is not required.

Figure 9 shows V-I curves with mesa width as a parameter. The lowest forward voltage is obtained for 40nm mesa width. The forward voltage of the device with 20nm mesa increases more rapidly than that of the device with 40 nm mesa. The carrier density increases rapidly in the n-base near the trench mesa as the current density increases, as shown in Fig.8, because the mobility decreases as carrier density increases. If the carrier density exceeds the induced channel electron density in the mesa, hole current starts to flow and the electric field in the n-base increases. The forward voltage increases rapidly if the device has the p-emitter of very low injection efficiency, as shown by curve E in Fig.9. This is because hole current hardly flows even when the stored charge exceeds the induced channel electron density in the device E. A high electric field appears at the n-base n-buffer junction and forward voltage increases.

The proposed device can be switched-off by applying a negative bias to the gate (see Fig.10). The fall-time is 200nsec. A hump appears in the voltage waveform when the gate voltage decreased below the threshold voltage and the channel resistance becomes high for both electrons and holes.

Figure 11 compares the on-resistance of the proposed IGBT with state of the art devices. Silicon IGBTs will realize low on-resistance even below SiC limit for over 2kV range.

III. THEORY FOR LARGE ELECTRICAL SHORT-CIRCUIT SOA

Short-circuit capability was demonstrated, for the fist time, in Non-Latch-Up IGBT by the author's group in 1984[2], and we published the waveforms of Fig.12 in 1987[2]. We also showed, for the first time, in 1988 that the SOA is greatly enhanced if the channel electron current exists[3]. In 1996, Hagino et al. reported very high critical power density of 2MW/cm^2[4] for short-circuit capability. Although

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short-circuit SOA has been analyzed by many authors[5], no theory has been presented, so far, to design a large short-circuit SOA.

In Ref.[6], the author predicted that the space charge becomes zero in the n-base if the saturated collector current, Jc, satisfies the equation:

$$J_C=qN_D/((1-\gamma)/v_e - \gamma/v_h), \qquad \text{-------Eq.(5)}$$

where N_D, v_h and v_e denote the n-base donor density, hole and electron saturation velocities, respectively, and γ denotes the the ratio of the hole current over the total current at the n-base n-buffer junction. The equation means that the flat uniform high electric field can be realized in the n-base under short-circuit condition, if an adequate γ is chosen.

Fig. 13 shows how large current voltage relation depends on the anode efficiency γ of the n-buffer/p-emitter structure. It was found that the optimum γ is 0.385, which is lower than the value, predicted by Eq.(5). The reason is that 2-dimensional effect exists in the actual case. Figure 14 shows the space charge density distribution. The electrons flows into the n-base from the mesa region and the space charge density is negative in the portion of the n-region under the mesa. However, the space charge density is positive in the portion of the n-base directly under the trench gate, where the electron current density is relatively low. Thus, the averaged space charge density as a function of the distance from the surface is substantially low as shown in Fig.15, and the high on-state breakdown voltage is realized for the device of the γ.

The figure 16 shows the calculated I-V curves for extremely high saturation current region. No significant impact ionization occurs in 600V rated IGBTs even for the condition of 10000A/cm^2 current density and 500V applied voltage if an appropriate γ is chosen. Power density is 5 x 10^{6}W/cm^2.

Maximum SOA locus can be predicted by calculating the impact ionization current under the assumption that an optimum γ is chosen and that the flat and uniform electric field is realized in the n-base. The maximum SOA is defined as the area where the impact ionization current density, J_{imp} is limited to below a constant value.

$$J_{imp} \cong \int J_e \alpha_\infty \exp(-\frac{b}{E})\ dx = (1-\gamma) J \alpha_\infty W_N \exp(-\frac{bW_N}{V}) < Const,$$

where W_N denotes the n-base width and the impact ionization by hole current is ignored. If the electric field is constant and sufficiently small, the integral is easily evaluated. The SOA boundary locus is expressed as:

$$J = C/[W_N \exp(-bW_N/V)], \qquad \text{-------Eq.(6)}$$

where W_N is the n-base width, C and b are constants.

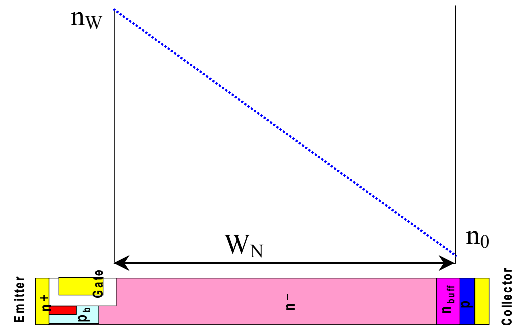

Fig.1 Linearly graded carrier distribution in N-base

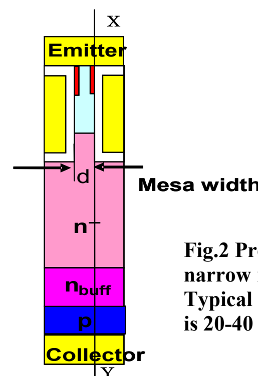

Fig.2 Proposed IGBTs with narrow mesa structure. Typical silicon mesa width, d, is 20-40 nm

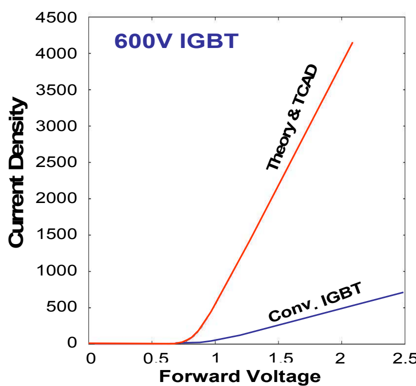

Fig.3 V-I curve comparison between proposed theory, TCAD result and conventional 600V IGBTs. (Theory and TCAD exactly coincides with each other) (a=3.7e18, b=9.39e16)

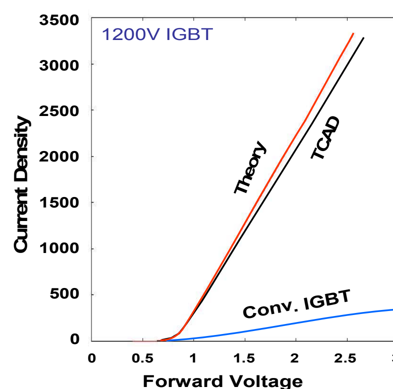

Fig.4 V-I curve comparison between proposed theory, TCAD result and conv. 1.2kV IGBTs.

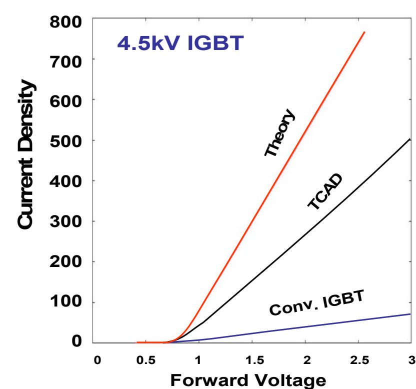

Fig.5 V-I curve comparison between proposed theory, TCAD result and conventional 4.5kV IGBTs.

In Fig.16, the dotted line shows the SOA locus given by Eq.(6) where J_{imp} is assumed to be approximately $200A/cm^2$, which corresponds to the generation rate of $2.5x10^{23}cm^{-3}$. No significant impact ionization occurs within the locus.

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[6] A. Nakagawa et al., Proc. of ISPSD'04, p.103

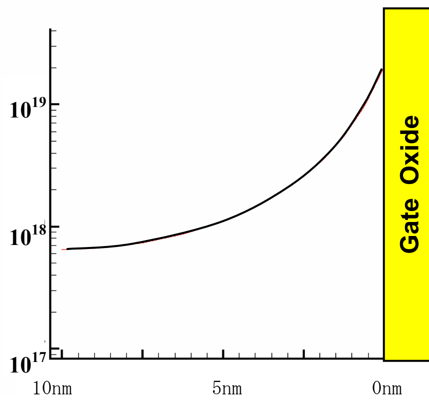


Fig.6 Electron density in the mesa as a function of distance from gate oxide (V_G=15V). Induced high electron density layer works as N+ layer.

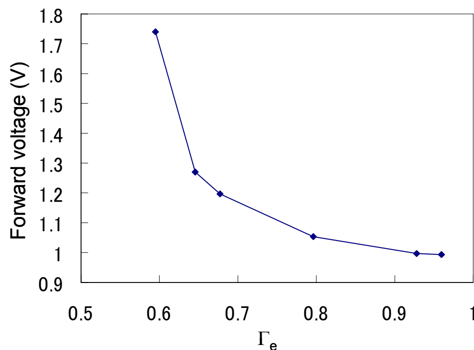


Fig.7 Forward voltage of 600V IGBTs at 500A/cm2 as a function of electron injection efficiency, Γ_e. Γ_e of more than 0.8 is desired.

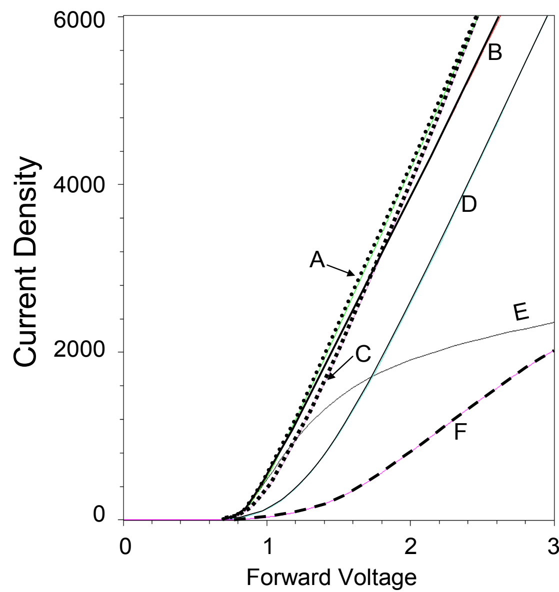


Fig.9 Calculated V-I curves of 600V IGBT with mesa width as a parameter. A:40nm mesa width, B:20nm mesa width, C: mesa width > 40nm, D: 0.5μm mesa width, E:20nm mesa with very low γ, F: 2.2μm mesa width

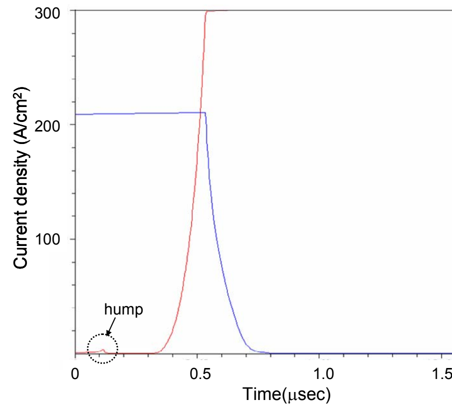
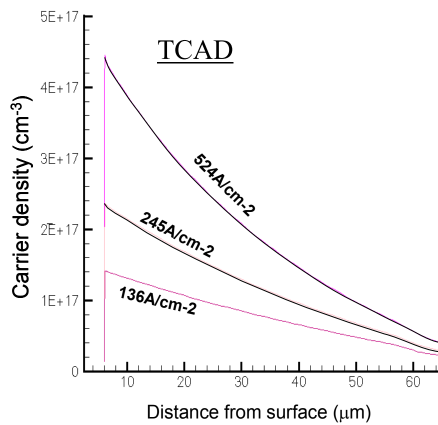


Fig.10 TCAD calculated turn-off waveforms under inductive load. Calculated fall-time is 200ns. A hump appears in voltage waveform when the gate voltage decreased below the threshold voltage and the channel resistance becomes high both for electrons and holes.



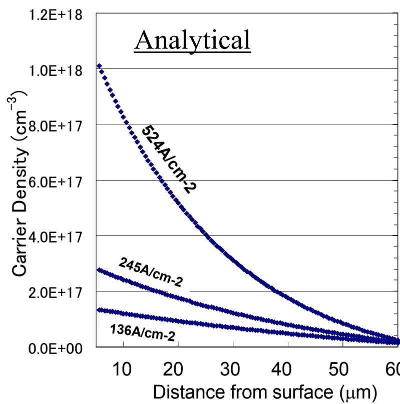


Fig.8
Calculated carrier density distribution in the n-base with current density as parameter. The left figure shows the TCAD results and the right figure shows the results of analytical theory. In the analytical theory, the approximation D_n=a/(n+b) gives excessively lower diffusion coefficient value for more than $1x10^{18}$ carrier density. Strictly speaking, the theory is valid for less than $1x10^{18}$ stored carrier density in the n-base.

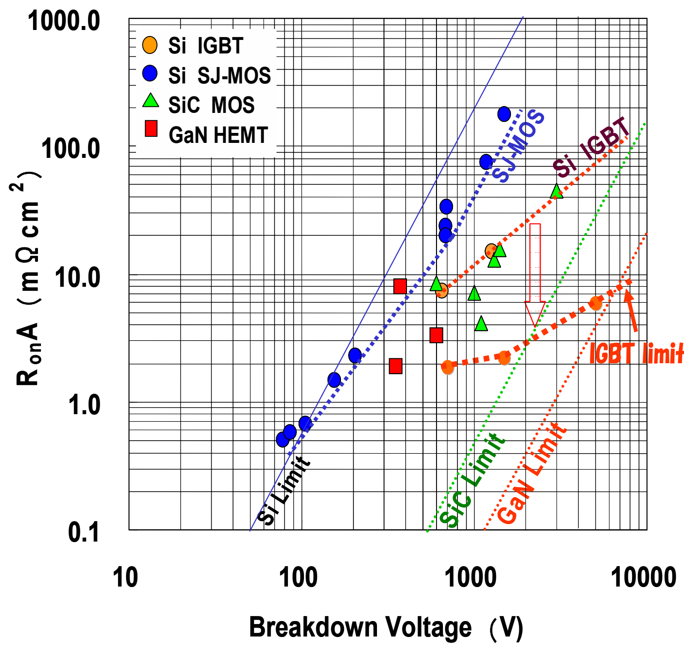


Fig.11 The proposed IGBT, denoted as "IGBT limit," is compared with state of the art devices. Predicted IGBT limit surpasses so called SiC limit for over 2kV range.

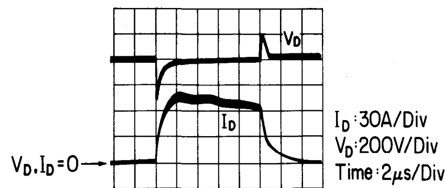


Fig.12 World first demonstration of short-circuit capability in 1200V IGBTs in 1984[2].

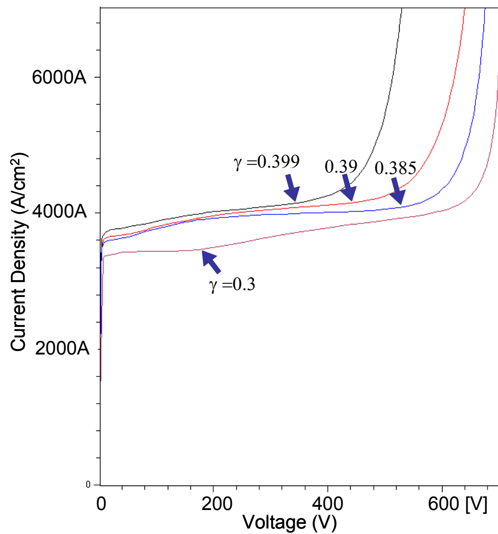


Fig.13 Short-circuit withstanding capability depends on anode efficiency γ of IGBT. For excessively low γ of 0.3, premature breakdown occurs at n-base n-buffer junction. Arrows indicate the voltage, above which significant impact ionization takes place.

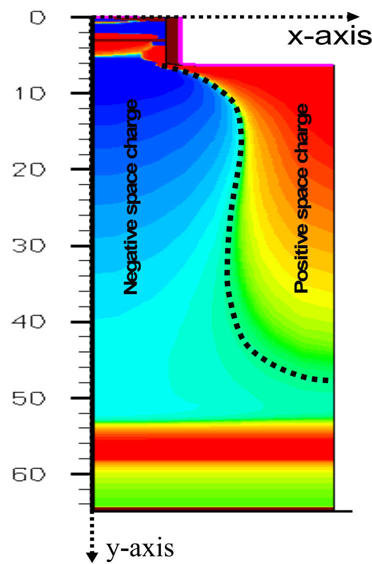


Fig.14 Space charge density in the n-base is shown for the device with γ of 0.385 in Fig.12. The dotted line shows the boundary of negative and positive space charge regions.

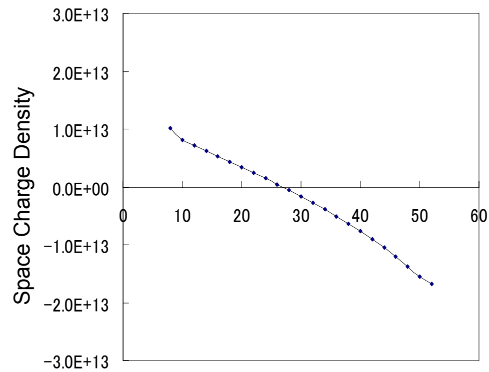


Fig.15 Space charge density of the device in Fig.14, averaged over x-axis, is plotted as a function of distance from surface (y-axis).

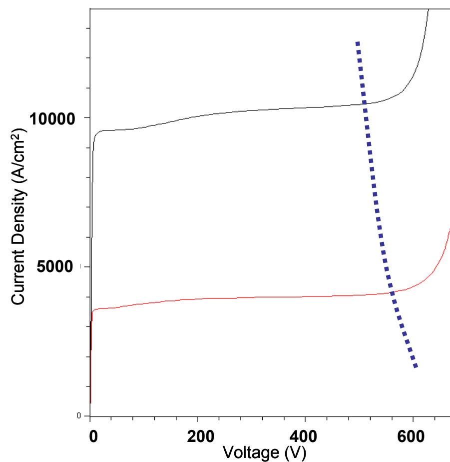


Fig.16 TCAD calculated V-I curves for extremely large saturation region. The device can withstand 500V 10kA without significant impact ionization. The dotted line shows the maximum SOA locus ($J=C/[W_N\exp(-bW_N/V)]$), where no significant impact ionization takes place.