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High density MOSBD (UMOS with built-in Trench Schottky Barrier Diode) for Synchronous Buck Converters

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***Abstract*- We proposed a new MOSBD, which integrates MOSFET and Schottky Barrier Diode (SBD) in a single chip. The features of the device are that the SBD are fabricated on fine mesa of less than 0.2μm, surrounded by trenches and optimally distributed inside the high density UMOS. We show that the distributed layout of the SBD inside the MOSFET cells is effective to reduce the reverse recovery charge (Qrr), output charge ($Q_{oss(SBD)}$) and the forward voltage drop ($V_{f(SBD)}$). In addition, integrated high density UMOS realizes low on-resistance of 18mΩmm^2 at Vgs=4.5V. The developed MOSBD achieved 46% reduction of chip size, compared to conventional MOSBD and low leakage current even in 175°C high temperature condition. The developed MOSBD successfully increases the conversion efficiency, compared to the discrete solution of MOSFET with external SBD.**

Ⅰ. INTRODUCTION

The low voltage, large current, and high current slew rates (di/dt>150A) are demanded for voltage regulator module (VRM) with increase in clock speed of microprocessors in recent years. Generally as for DC-DC buck converters, used for these applications, high slew rate is realized by increasing its operation frequency to 1MHz or higher. In order to satisfy high operation frequency and high conversion efficiency simultaneously, a large number of studies about optimized MOSFETs and improved packages have been carried out [1-4]. For low-side MOSFETs, reduction of the on-resistance is the most important. It is also important to prevent the power loss caused by shoot-through current, or self turn-on of the low-side MOSFET. The authors showed[5] that, in order to prevent a self turn-on phenomenon, it is effective to reduce the reverse recovery charge: Qrr, of the low-side MOSFETs. In addition to the reduction of Cgd/Cgs ratio.

In this paper, we will describe new MOSBD, which integrates low-side MOSFET and Schottky Barrier Diode in a single chip.

Ⅱ. DEVICE DESIGN AND SIMULATION

Figure.1 shows a circuit of synchronous buck converter. A Schottky Barrier Diode (SBD) is laid out parallel to the low side MOSFET in order to reduce the body diode loss. MOSBD integrates low-side MOSFET and SBD in a single chip, thus dose not need an external SBD. The cross sectional view of the developed MOSBD is shown in fig. 2. The SBD cells, fabricated on fine mesa between trench source electrodes, are uniformly distributed inside MOSFET cells. Figure 3 shows the simulated dependence of output charge ($Q_{oss(SBD)}$) and $V_{f(SBD)}$ on SBD mesa Width (Ws). The $Q_{oss(SBD)}$ decreases rapidly as the silicon mesa width becomes 0.4um or less. The decrease in $Q_{oss(SBD)}$ is effective to reduce power loss in DC-DC

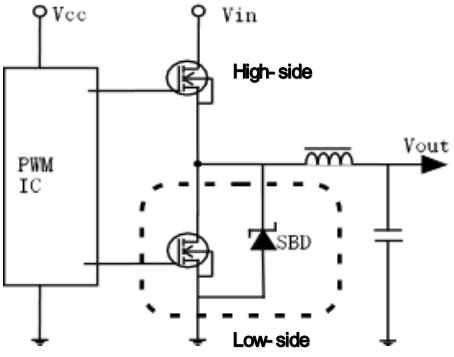

Figure.1 Circuit of Synchronous Buck Converter.

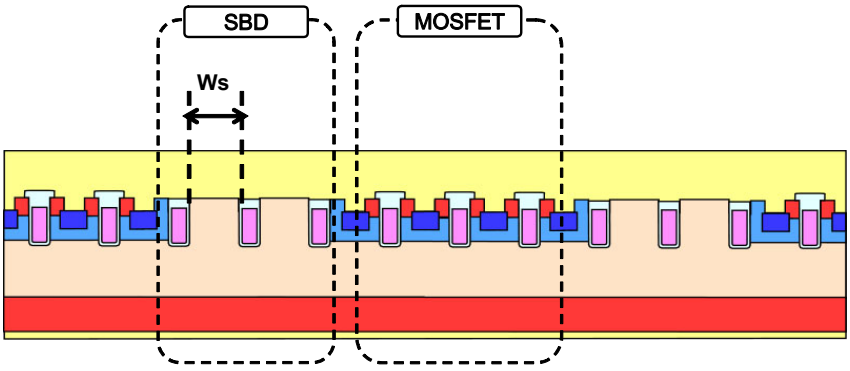

Figure.2 Cross sectional view of developed MOSBD structure.

converter.

We found very important design rule of how to distribute the SBD cells inside the MOSFET cells: "distributed" arrangement and "concentrated" arrangement. "Concentrated" means a larger number of SBD cells are fabricated in a single localized area. Figure.4 shows simulated dependence of electron-current density on SBD arrangement, (a) distributed arrangement and (b) concentrated arrangement under the condition that the total SBD contact area is the same. Forward Voltage ($Vf_{(SBD)}$) of SBD for distributed arrangement is lower than that of concentrated arrangement at the same Ids leakage current level as shown in fig.5, because of its uniform electron-current flow[6].

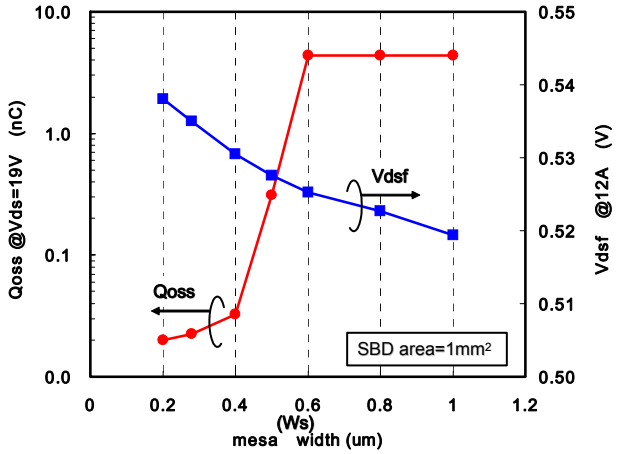

Figure.3 SBD mesa Width (Ws) dependency on output charge ($Q_{OSS(SBD)}$) and $Vf_{(SBD)}$ (simulation). When silicon mesa width is 0.4um or less, output charge decreases sharply.

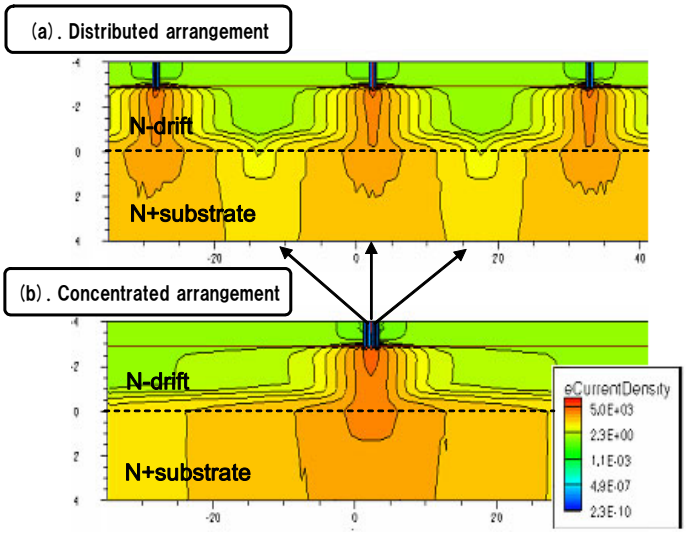

Figure.4 SBD arrangement dependence of the electron-current density by the simulation. (a) Distributed arrangement and (b) concentrated arrangement have same SBD contact area.

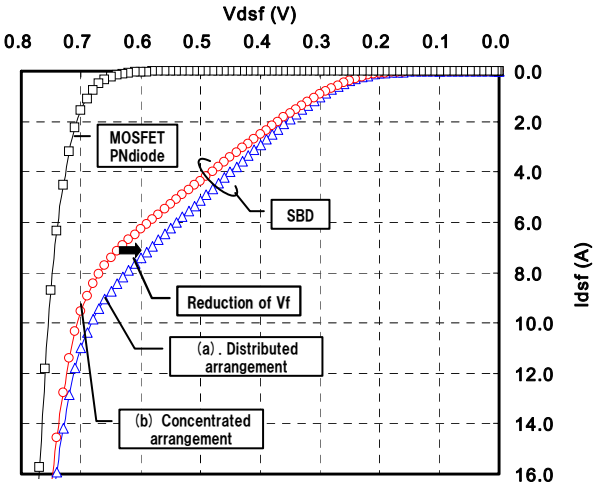

Figure.5 Simulated diode current, Idsf, vs. Vf. (a) Distributed arrangement and (b) concentrated arrangement.

Ⅲ. RESULTS AND DISCUSSION

We have fabricated the high cell density MOSBD which suppressed the total area of SBD by the distributed layout of the SBD cells. The cross-sectional SCM image of the MOSBD device is shown in Fig. 6. Measured $R_{(DS)ON.SP(Si)}$ of MOSFET except for the SBD area is 18mΩmm^2 at Vgs=4.5V. The total SBD area occupies only 17% of the total chip. The small gate resistance of 0.45Ω and Cgd/Cgs ratio of 0.05 at Vds=10V were realized. As for Gate charge: Qg/Activearea, 9.4nC/mm^2 was obtained on condition that Vds=10V and Vgd=24V. Since the poly in the trench surrounding SBD is connected with the source electrode, low gate capacity is obtained.

The characteristics of SBD are excellent. Measured If-Vf curve of MOSFET without SBD and those of MOSBD with (a) distributed arrangement and (b) concentrated arrangement are shown in Fig.7. The $Vf_{(SBD)}$ of MOSBD is successfully reduced and no body diode current of MOSFET flow when the forward current is less than 7 A. Furthermore, superior temperature characteristics are achieved as shown in fig 8. The SBD structure with narrow mesa width(Ws) is excellent in the Ids(SBD-leak) characteristic in 175°C. For this reason, fabricated MOSBD shows a hardly break down at 37V. Figure 9 shows

measured waveform of reverse recovery characteristics. Compared with conventional MOSFET[7], maximum recovery current and trr of MOSBD is decreased. The developed MOSBD shows outstanding avalanche capability of 41.5mJ/mm^2 as shown in Fig. 10.

Developed MOSBD was able to be reduced to a chip size of 46% compared to conventional MOSBD in the condition to which on-resistance and Vf were equal. Figure 11 is an image of this reduction of the chip size by having distributed SBD in high density UMOS.

Figure 12 shows experimentally obtained efficiency vs. load current as compared to the MOSFET with external SBD and conventional MOSBD at 1MHz operation. Developed high cell density MOSBD achieved the improvement in the efficiency for all load current without external SBD.

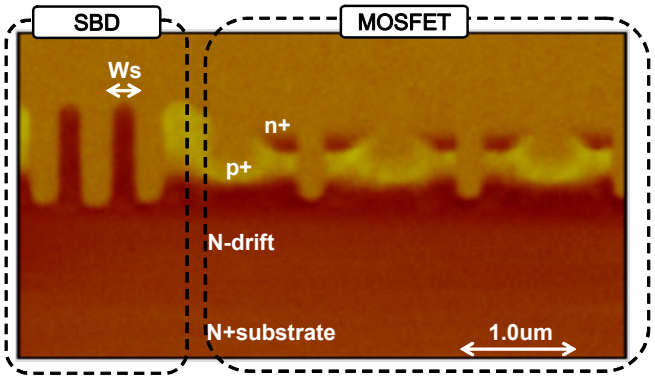

Figure.6 Cross sectional SCM image of fabricated MOSBD.

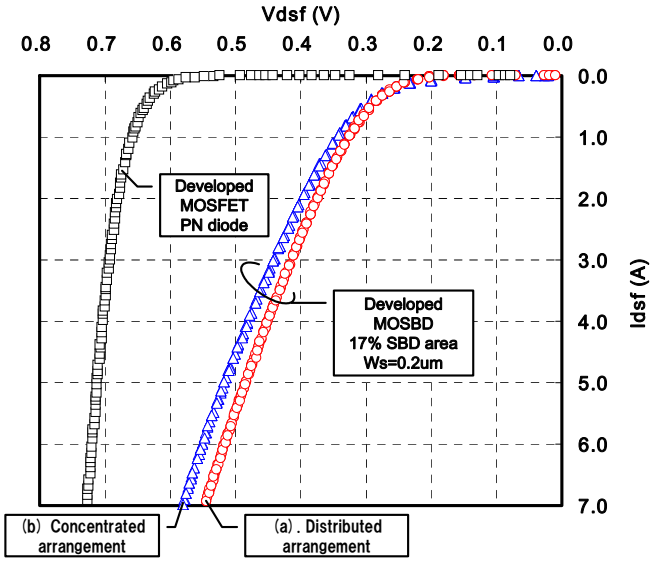

Figure.7 Measured diode characteristics of fabricated MOSFET and MOSBD. Vf of (a) is lower than that of (b) at same leakage level.

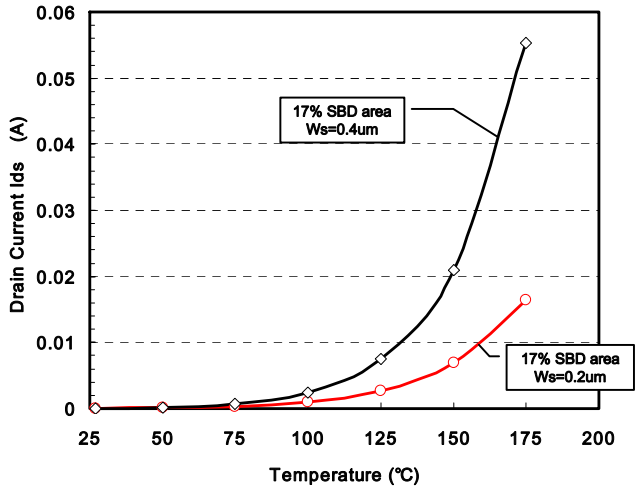

Figure.8 Measured characteristics of Ids(SBD leakage current) of MOSBD as a function of temperature at Vds=24V.

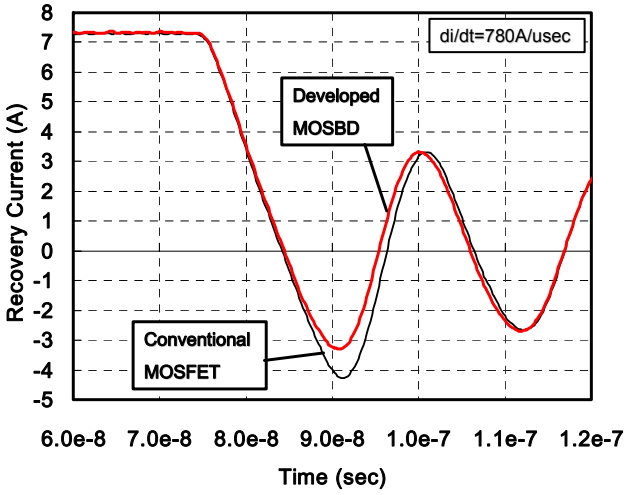

Figure.9 Measured recovery waveforms of conventional MOSFET and MOSBD(17% SBD area) at same active area.

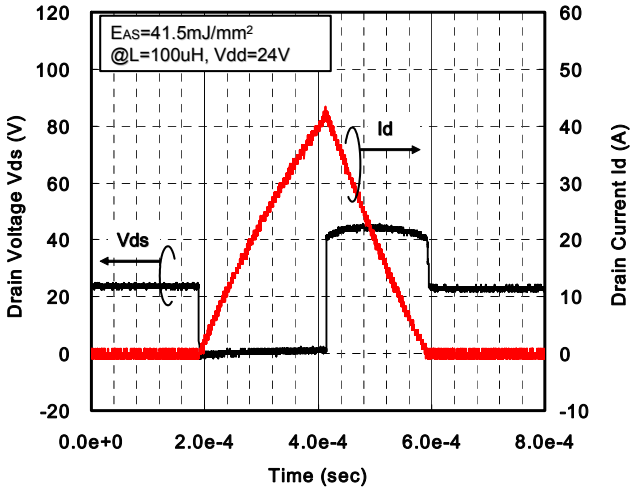

Figure.10 Measured UIS waveforms of fabricated MOSBD (17% SBD area).

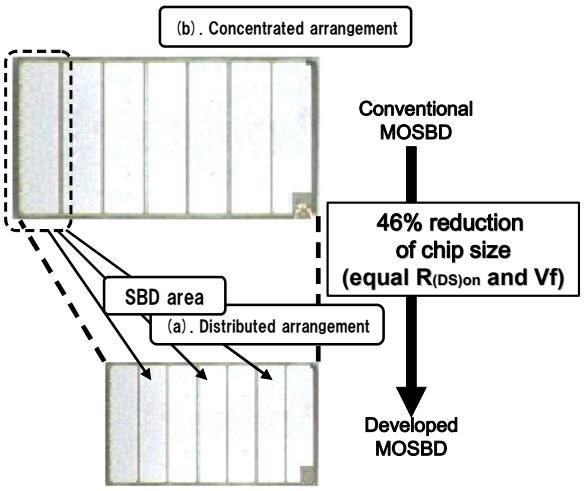

Figure.11 .Reduction of chip size was achieved by fine SBD surrounded by trenches and optimally distributed inside the high density UMOS

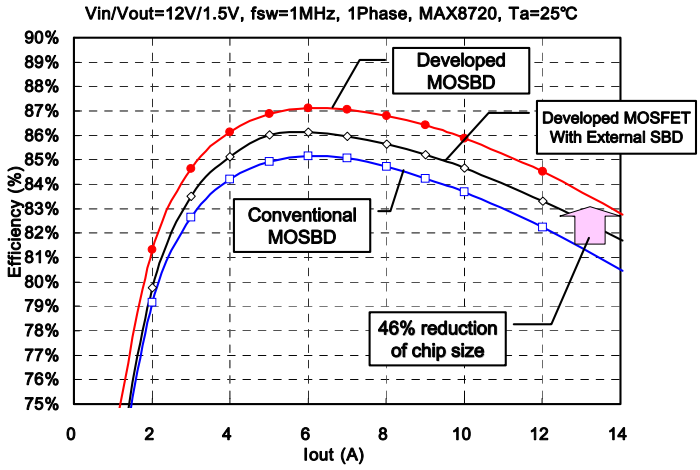

Figure.12 Measured dependence of Efficiency on Output current (Iout).

Ⅳ. CONCLUSIONS

We have developed a new MOSBD, which integrates MOSFET and Schottky Barrier Diode (SBD) in a single chip. The features of the device are that the SBD are fabricated on fine mesa of less than 0.2μm, surrounded by trenches and optimally distributed inside the high density UMOS. We show that the distributed layout of the SBD inside the MOSFET cells is effective to reduce the forward voltage drop ($V_{f(SBD)}$) compared to "concentrated" arrangement. In addition, integrated high density UMOS realizes low on-resistance of 18mΩmm^2 at Vgs=4.5V. The developed MOSBD achieved 46% reduction of chip size, compared to conventional MOSBD and low leakage current even in 175 ^{o}C high temperature condition. The developed MOSBD successfully increases the conversion efficiency, compared to the discrete solution of MOSFET with external SBD.

Ⅴ. ACKNOWLEDGEMENTS

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