Multi Chip Module with Minimum Parasitic Inductance for New Generation Voltage Regulator

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Abstract

This paper analyzes the effects of parasitic inductances over the conversion efficiency of DC-DC converters by using Spice simulator. It was found that the self-turn-on of the low side MOSFET is triggered by large body diode reverse recovery current. A new multi chip module (MCM) has been developed in order to suppress the self-turn-on of the LS MOSFETs and to reduce the parasitic inductances. The MCM also has unique upper surface cooling feature. The MCMs successfully improve the conversion efficiency by using the MOSFETs with reduced body diode reverse recovery. Conversion efficiency can be further improved by reducing the gate resistance and optimizing the dead time.

Introduction

With recent increase in clock speed of CPU, low voltage, large current, high di/dt DC-DC converters is strongly demanded. Many studies of high speed switching MOSFET have been carried out [1, 2]. However, optimization of circuit parameters such as parasitic devices on board is also important.

It is often pointed out that the parasitic source inductances of the high side MOS decreases the conversion efficiency. In this paper, we present the importance of the other parasitic inductance of high and low side MOSFET. It also strongly affects the conversion efficiency. In order to reduce the parasitic inductances, we introduce a new multi chip module (MCM) without bonding wires. Another serious problem of these DC-DC converters is heat radiation. Therefore, the MCM should be designed to radiate the large amount of generated heat in order to improve the conversion efficiency.

Analysis of Energy Loss by Spice Simulator

Figure 1 shows a circuit of synchronous buck converter. In order to design the MCM layout by circuit simulator, trench MOSFETs were modeled as the sub-circuits shown in fig. 2. As the value of Cgd depends on both Vgd and Vds, it was given as a newly developed function to fit the measured characteristics of the trench MOSFETs. DBD represents the body diode in trench MOSFETs. The values of parasitic inductances and capacitances in the MCM circuit board were extracted by electromagnetic simulation and were considered in the circuit simulation, as shown in fig. 3.

The effect of both each MOSFET parasitic inductance, Lhd, Lhs, Lld, Lls, was analyzed by circuit simulation. Transient simulations were carried out for the conditions listed in table 1. When one parasitic inductance value is varied, the other values are fixed. Figure 4 shows the dependence of conversion efficiency on the each parasitic inductance of MOSFETs. As shown in this figure, not only high side source inductance but also the other inductances affect conversion efficiency. In order to explain the detail of energy loss, the dependence of low side MOSFET source inductance on the distribution of each loss is examined. Condition 1 in table 2 represents a MCM case, and condition 2 is a comparing case. Table 3 shows the distribution of each energy loss element. It was found that the turn-off loss of high side MOSFET occupies a large portion of the total power loss. Figure 5(a) and (b) compare the waveforms of the drain-source voltage, gate-source voltage, drain current, and power consumption of the high side MOSFET. During the turn-off transient of the high side MOSFET, 5.6 nH parasitic inductance of the low side MOSFET causes a large surge drain-source voltage, exceeding the breakdown voltage of the high side MOSFET. This surge voltage causes the large power loss.

Another problem in parasitic inductance is enhancement of self turn-on phenomenon. The self turn-on is a phenomenon of the undesired low side MOSFET turn on, caused by the high side MOSFET turn-on in the period that low side MOS must stay in the off-state [3]. Once the self-turn-on occurs, both high side and low side MOSFET are in the on-state, and a large energy loss occurs. This problem has more significant effect on conversion efficiency in the case of higher input voltage. Table 4 shows the dependence of low side MOSFET source inductance on self turn-on power loss. This phenomenon is explained as following expressions. As shown in Fig. 6, which are low side MOSFET waveforms after turning off in the condition 5, the MOSFET body diode recovery current is dominant among the total source current of the low side MOSFET until self turn-on occurs. The large recovery current induces a large voltage drop in the source parasitic inductance of low side MOSFET (L_{ls}). The diode reverse recovery abruptly ceases, and the abrupt reduction of the reverse recovery current imposes a large dV/dt to the low side MOSFET. It is found that low side MOSFET body diode recovery current enhances the dV/dt of the low side MOS source-drain voltage (V_{Lds}), which is steeper than the dV/dt of the Lx node voltage (V_{Lx}). The supply voltage V_{dd} is expressed by V_{Lds}, high side MOS source-drain voltage (V_{Hds}), total inductance from supply to ground $L(=L_{hd}+L_{hs}+L_{ld}+L_{ls})$, and low side MOSFET drain current (I_{ld}) as following expression.

$$V_{dd} = V_{Hds} + V_{Lds} + L \times \frac{di_{ld}}{dt}$$

Therefore, dV_{ds}/dt is determined by the following expression.

$$\frac{dV_{Lds}}{dt} = -\frac{dV_{Hds}}{dt} - L \times \frac{d^2 i_{ld}}{dt^2}$$

Meanwhile, because low side MOSFET self turn-on phenomenon is triggered by dV_{Lds}/dt, total inductance L affects power loss by self turn-on.

As discussed above, it is strongly required to reduce not only high side MOSFET parasitic source inductance but also the other parasitic inductances.

Concept of New Multi Chip Module (MCM)

In order to reduce this parasitic inductance, we have adopted new multi chip module (MCM) shown in fig. 7 (a) and (b). The main features of the MCM are (1)bump connection, substituting for wire bonding, (2)monolithic integration of low side MOSFET and SBD, called as MOSBD, and (3)heat spreader, covering the surface. Minimum parasitic inductance is realized by connecting each chip with bump and monolithic MOSBD, and the heat resistance is remarkably decreased by the heat spreader. One of the good features of the MCM is that the surface cooling package can share the heat sink with CPU.

Optimization of Device and Circuit Parameters

As shown in table 3, the dead time power loss and self turn-on loss are also two major contribution factors. This driver IC is designed to control the dead time as short as 5nsec, which is effective to reduce both the dead time and the self turn-on loss.

Figure 8 shows the experimentally obtained conversion efficiency comparison between discrete MOSFET and the new MCM. The MCM has successfully improved the conversion efficiency because of its minimum parasitic inductances and the low heat resistance.

When the low side MOSFET source inductance is reduced as low as 1.4 nH, the next arising issue is the low side on-state resistance. Condition 3 in table 2 is a comparing case to examine the effect of low side on-resistance, i.e. the area of low side MOSFET. In the case of condition 3 in table 3, the conversion efficiency was not improved although the low side on-resistance was decreased to a half of condition 1 in table 2. Although the low side on-state power loss was reduced, it was found that the high side turn-on loss was remarkably increased. This was because the recovery current of low side MOSFET body diode flew through the high side MOSFET when the high side MOSFET turned-on. Figure 9 shows the waveforms of the low side and high side MOSFET for condition 3 in table 2. Because of its large area of low side MOSFET, a large surge current was brought about by the recovery current, Ibd, of the low side MOSFET body diode. Comparing Fig.9 and Fig. 5 (a), it was found that this surge current caused a large turn-on power loss in the high side MOSFET. In order to further improve the conversion efficiency, it is important to reduce the recovery current of low side MOSFET body diodes. In addition, dead time loss and high side switching loss also occupy large part of total loss in condition 3. Therefore, it is effective to reduce the gate resistance, and to optimize the dead time. Figure 10 shows the comparison of condition 3 and condition 6, improved recovery charge (Qrr), gate resistance and dead time condition. This figure shows that the switching loss and the dead time loss are successfully reduced. It is found that further improvements of device and circuit parameters enable to increase conversion efficiency of DC-DC converter.

We have newly developed low side MOSFETs, based on the analyzed results. Figure 11 shows the preliminary experimental results in the case of 300 kHz for the developed low side MOSFET. The new low side MOSFET improved overall conversion efficiency, especially in the high current region.

Summary

We showed the effect of each parasitic inductance on the conversion efficiency of DC-DC converter by using Spice simulator. It is found that during the turn-off transient of the high side MOSFET, the parasitic inductance of the low side MOSFET causes a large surge drain-source voltage, exceeding the breakdown voltage of the high side MOSFET. This surge voltage causes the large power loss. In addition it was shown that large parasitic inductance trigger low side MOSFET self turn-on phenomenon. We introduce a new multi chip module (MCM) in order to reduce these inductances. This MCM has another feature, an external heat sink designed to radiate the heat from upper surface. It is found that this MCM successfully improve the conversion efficiency.

Reference

[1]M. Darwish et al. Proceedings of ISPSD 2003 pp. 24-27

[2]L. Ma et al. Proceedings of ISPSD 2003 pp. 354-357

[3]K. Murata et al. Proceedings of INTELEC '03 pp199-204

Input Voltage	Output Voltage	Output Current	Frequency	Dead time
12V	1.36V	20A	1MHz	30nsec

Table 1 Condition of conversion efficiency calculation for fig. 4.

	Input Voltage	Output Voltage	Output Current	Frequency	**Dead time**	**Relative on-resistance of low side MOS**	**Source Inductance of low side MOS (Lls)**	**Relative high side gate resistance**	**Relative low side gate resistance**
Condition 1	12V	1.36V	20.0A	1MHz	30nsec	1	1.4nH	1	1
Condition 2						1	**5.6nH**	1	1
Condition 3						**0.5**	1.4nH	1	1
Condition 4	19V	1.5V	5.0A			1	1.4nH	1	1
Condition 5						1	**4.2nH**	1	1
Condition 6	12V	1.36V	20A		5nsec	0.5	1.4nH	**0.41**	**0.58**

Table 2 Condition of conversion efficiency calculation in order to explain the detail of power loss

Condition in table2	relative low side MOS on-resistance	source inductance of low side MOS	Efficiency (%)	Power loss in high side MOS (W)			Power loss in low side MOS (W)				others (driver, etc)
				Turn-on	on-state	turn-off	dead time (off)	self turn-on	dead time (on)	on-state	
1	1	1.4	83.47	0.59	0.66	0.69	0.41	0.26	0.63	1.11	1.05
2	1	**5.6**	81.99	0.01	0.73	1.66	0.46	0.24	0.64	1.06	1.18
3	**0.5**	1.4	83.58	0.92	0.65	0.57	0.37	0.49	0.58	0.55	1.21

Table 3 Calculated conversion efficiency and power loss distributions for the condition 1-3 in table 2

Condition in table 2	source inductance of low side MOS (nH)	Efficiency (%)	High side MOS distributions (W)			Low side MOS distributions (W)				
			Turn-on	on-state	turn-off	dead time (off)	self turn-on	dead time (on)	on-state	others (driver, etc)
4	1.4	83.20	0.52	0.03	0.12	0.04	0.52	0.11	0.09	0.09
5	4.2	81.89	0.29	0.03	0.20	0.04	0.79	0.10	0.10	0.10

Table 4 Calculated conversion efficiency and power loss distributions for the condition 4, 5 in table 2

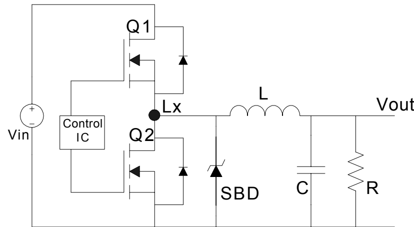
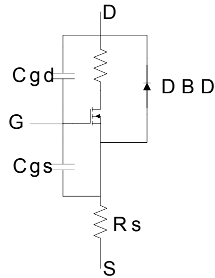


Figure 1 Circuit of synchronous buck converter



$$Cgd = f(Vgs) \cdot g(Vgd) \cdot W \cdot L$$

$$f(Vgs) = 455.5 \times 10^{-6} \times (1.0 + 0.03 \times Vgs^{1.3})$$

$$g(Vgd, Nd, d) = (2.97 \times 10^{14} \times d^2 + 3.52 \times 10^{16} \times \max(0, -Vgd)/Nd)^{-0.45}$$

W: Gate width, *L*: Gate length, *d*: Gate oxide thickness
Nd: Epitaxial layer impurity concentration

Figure 2 Spice model for Trench MOSFET. As the value of Cgd depends on both Vgd and Vds, it was given as a newly developed function to fit the measured characteristics of the trench MOSFETs. DBD represents the body diode in trench MOSFETs

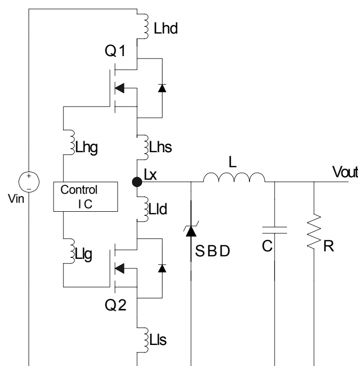


Figure 3 Parasitic devices in DC-DC converter circuit
The values of parasitic inductances and capacitances in the MCM circuit board were extracted by electromagnetic simulation

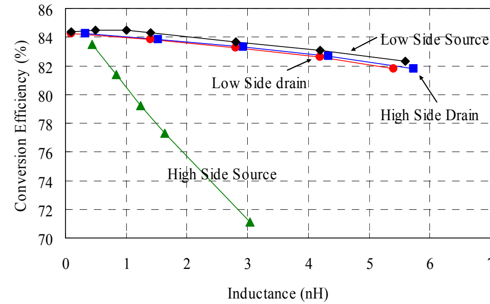


Figure 4 Dependence of conversion efficiency on each parasitic inductance

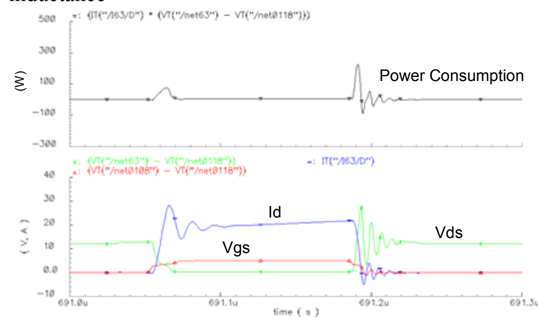


Figure 5(a)

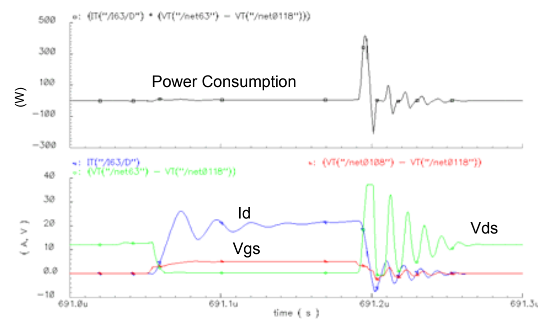


Figure 5(b)

High side MOSFET waveforms of drain-source voltage, gate-source voltage, drain current, and power consumption for the condition of (a)1.4nH and (b)5.6nH of low side MOSFET source inductance (condition1 and 2 in table1). During the turn-off transient of the high side MOSFET, 5.6 nH parasitic inductance of the low side MOSFET causes a large surge drain-source voltage, exceeding the breakdown voltage of the high side MOSFET. This surge voltage causes the large power loss

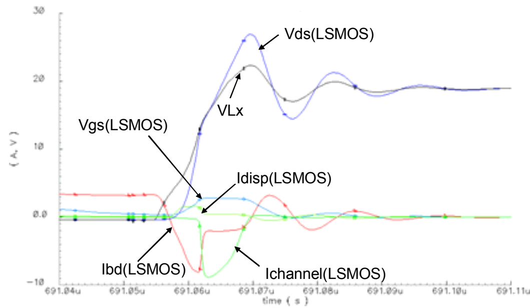


Figure 6 Waveforms of self turn-on phenomenon. Vds(LSMOS), Vgs(LSMOS), Idisp(LSMOS), Ibd(LSMOS), Ichannel(LSMOS) represent drain-source voltage gate-source voltage, displacement current, body diode current and channel current of low side MOS, respectively. VLX represents voltage of Lx node in fig.1. This figure shows that body diode current causes dV/dt enhancement.

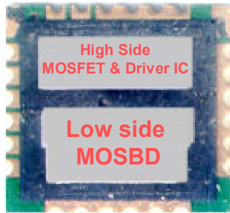


Figure 7(a) Top view of the MCM. The main features of the MCM are (1)bump connection, substituting for wire bonding, (2)monolithic integration of low side MOSFET and SBD, called as MOSBD, and (3)heat spreader, covering the surface.

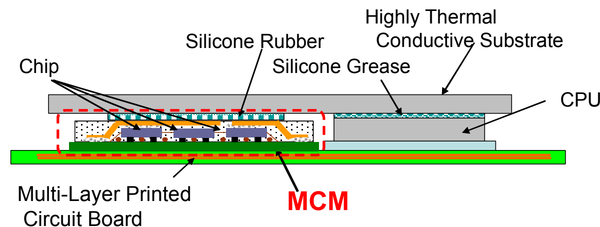


Figure 7(b) Cross-sectional view of the MCM and a mounting method example. One of the good features of the MCM is that the surface cooling package can share the heat sink with CPU.

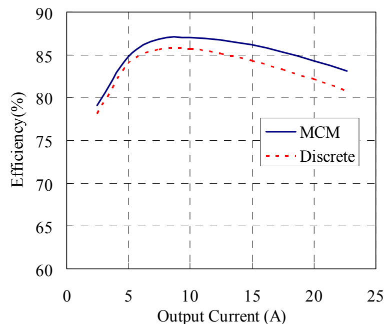


Figure 8 Experimentally obtained conversion efficiency comparisons between discrete MOSFET and new MCM. As shown in this figure, the MCM improve the conversion efficiency because of its minimum parasitic inductance.

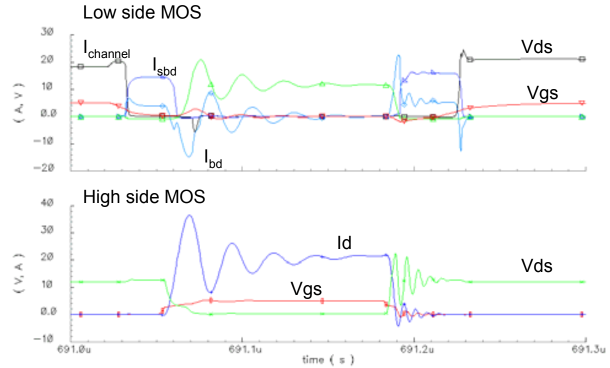


Figure 9 Waveforms of the low side and high side MOSFET for condition 3 in table 1. Because of its large area of low side MOSFET, a large surge current was brought about by the recovery current, Ibd, of the low side MOSFET body diode. Comparing Fig.8 and Fig. 4(a), it was found that this surge current caused a large turn-on power loss in the high side MOSFET

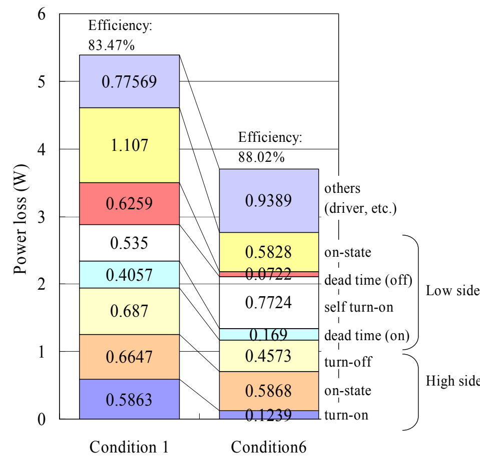


Figure 10 Effect of optimizing device and circuit parameters. The low side on-state loss, high side switching loss and the dead time loss are successfully reduced. It is found that further improvements of device and circuit parameters enable to increase conversion efficiency of DC-DC converter.

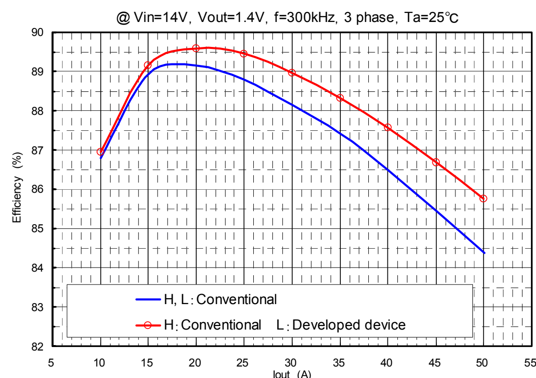


Figure 11 Preliminary experimental results in the case of 300 kHz of the new low side MOSFET. This MOSFET improved overall conversion efficiency