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Optimization of 5V power devices based on CMOS for hot-carrier degradation

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Abstract

We propose "power CMOS," suitable for use as large current output devices. The proposed structure can be fabricated by low cost 0.6um logic CMOS process and assures long-term reliability even under the stress of hot-electrons. The developed power CMOS have achieved low specific on resistances of 8.1mΩmm^2 for NMOS and 21.1mΩmm^2 for PMOS.

Introduction

There is a huge market for mobile power management ICs today and in the future[1]. Fast transient response, efficient performance, small profile and low cost are the most desired features for mobile power management IC. In order to reduce the profile, we need to integrate control circuit, and power devices all in a single chip. In the 5V power ICs, monolithically integrated lateral power devices bring smaller specific on-resistance, comparing with discrete power devices [2]. This is because discrete power devices need thick N+ substrate for wafer handling. The substrate resistance occupies a larger part of the total device resistance, if the breakdown voltage of the discrete devoices is low. Therefore the monolithic integration is particularly important in low voltage applications.

In 0.6um CMOS processes, typical logic CMOS breakdown voltage is over 5V. Although the breakdown is satisfied with the low voltage power applications, logic CMOS devices are not designed for power applications, which require reliable switching operation under inductive loads. The degradation behavior induced by hot-electrons should be considered.

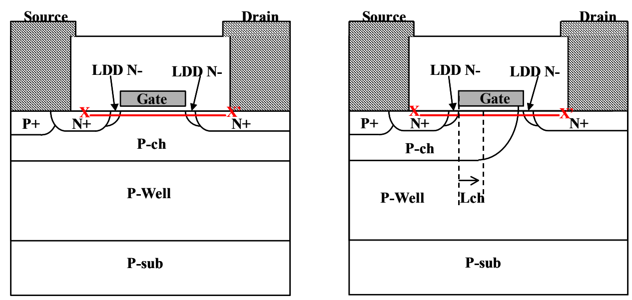
In this paper, we propose "Power CMOS". The proposed structure relaxes the degradation induced by hot-electrons, based on the low cost 0.6um CMOS process. The power CMOS devices have been developed without sacrificing the characteristic of the specific on resistance and without any additional process.

Device description

N-channel MOS has severer problem for hot-carrier degradation than p-channel MOS. Compared with n-channel MOS, the current density of a p-channel MOS is not so high as that of n-channel MOS because of lower carrier mobility. Therefore generated hot-carrier of p-channel MOS is smaller. The focus is on suppression of hot-carrier degradation in n-channel MOS.

Figure 1 shows a cross-sectional view of two studied structures for N-channel MOSFET. Both structures A and B are fabricated by the logic CMOS processes without any additional mask. In structure A, the channel implant layer P-ch is completely formed under the gate electrode, as is logic CMOS. In the structure B, the channel implant layer P-ch does not reach the drain N+ layer. The key parameter: Lch is defined as the length between the edge of gate and the mask edge of P-ch in the structure B.

Figure 2 shows the doping profile along X-X' line in Figure 1(a) and (b). As the impurity concentration of LDD N- region is higher than that of P-ch region, the depletion layer expands from LDD N- region into P-ch region when the drain is positively biased. The net acceptor concentration beside the drain in structure B is lower than that of structure A. Thus, the peak electric field in the drain is lower in structure B.



(a)Structure A (b)Structure B

Figure.1 Cross-sectional view of structure A and B. Both structure A and B are fabricated by the logic CMOS process without additional process.

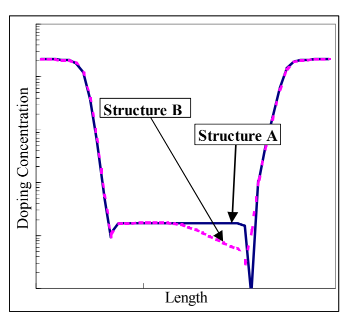


Figure.2 Simulated Doping profile along X-X' line in Figure1(a)(b)

Substrate current considerations

Figure 3 shows the experimentally measured substrate current, Isub, as a function of gate-source voltage, Vgs, for the cases where the gate length Lg are 0.6 and 0.8um in structure A and B. The applied drain-source voltage is 5.5V and the channel width is 54um. It is well known that the magnitude of substrate current correlates to the degree of the degradation induced by hot-electrons. In the structure A, the substrate current Isub(max) can be reduced to 60% when the gate length is changed from 0.6um to 0.8um. In the case of structure B (the gate length 0.8um), Isub(max) is reduced to 30% of that of structure A. In the structure A, the electric field between gate and drain is same regardless of gate length. But the current through the high electric field is smaller as the gate length becomes longer. Therefore the avalanche current is depended on the gate length.

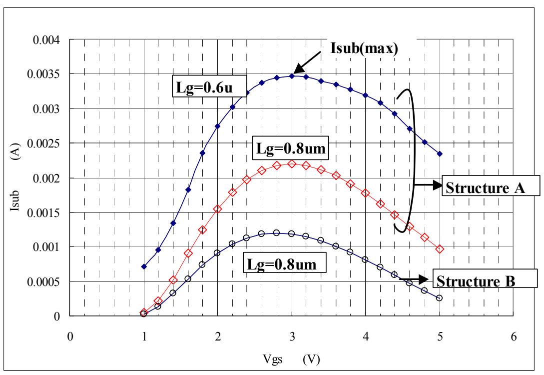


Figure.3 the experimentally measured substrate current Isub as a function of gate-source voltage Vgs. In the structure A, Isub(max) is reduced to 60% when the gate length is changed from 0.6um to 0.8um. In the case of structure B(the gate length 0.8um), Isub(max) is reduced to 30% of that of structure A.

Figure 4 shows the simulated electric potential contours of structure A and B at Vgs=3V, Vds=5.5V. The depleted layer is extended from LDD N- region into P-ch region and the electric field beside drain of structure B is smaller than that of structure A. Because of reduced electric field, the electron and hole ionization rates of structure A are smaller than that of structure B. Therefore the avalanche current of structure B is suppressed.

Figure 5 shows the dependence of Isub(max) and specific on-resistance RonA on the gate length. The Isub(max) decreases, however, the on-resistance increases linearly, if the gate length becomes longer.

Figure 6 shows the dependence of Isub(max) and specific on-resistance RonA on Lch. The Isub(max) decreases without sacrificing the characteristic of specific on resistance, when Lch is reduced.

In the optimized structure B, the blocking voltage, threshold voltage and specific on-resistance is 10.8V, 0.88V and 8.1mΩmm^2 at W=54um, respectively.

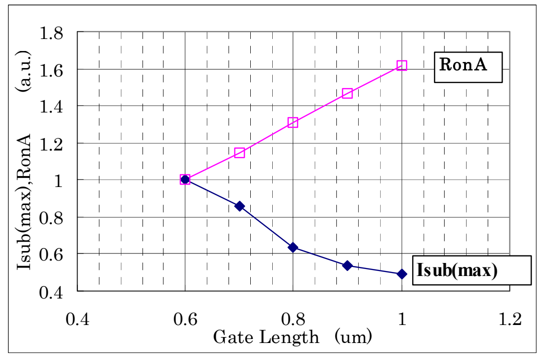


Figure.5 The dependence of Isub(max) and specific on-resistance on the gate length. The Isub(max) decreases and on-resistance increases linearly, as the gate length becomes longer.

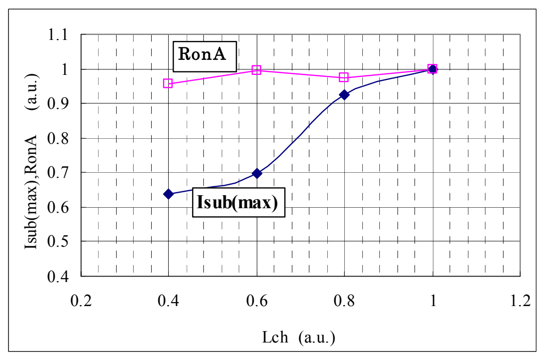
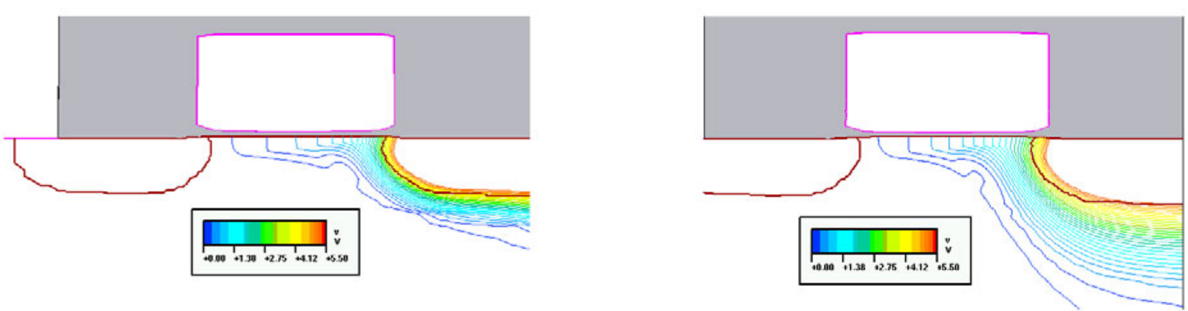


Figure.6 The dependence of Isub(max) and specific on-resistance RonA on Lch, which is defined in Fig.1(b). The Isub(max) decreases without sacrificing the characteristic of specific on resistance, when Lch is reduced.



(a)Structure A (b)Structure B

Figure.4 The simulated electric potential contours of structure A and B at Vgs=3V, Vds=5.5V. Then gate length is 0.8um. The depleted layer is extended from LDD N- region to P-ch region and the electric field beside drain of structure B is smaller than that of structure A.

We adopted the structure A, as shown in figure.1, as to p-channel MOSFET. The p-channel MOSFET in logic CMOS has buried channel to reduce channel resistance. If the structure B is utilized to the p-channel MOSFET, the buried channel does not reach the drain P+ layer and the threshold voltage depends on the doping concentration beyond the drain layer. Both the threshold voltage and the on-resistance in structure B is higher, comparing with structure A. Therefore, we adopted the structure A for p-channel MOSFET.

Degradation characteristic

Figure 7A and B shows the degradation characteristic of threshold voltage shift and drain current Idlin at linear region as a function of stress time, respectively. The device was stressed at Vds=6.5V and Vgs=3.2V.

It is found that both the threshold voltage shift and Idlin degradation of Lg=0.9um are smaller than those of Lg=0.6um in structure A. And those degradations of structure B(Lg=0.8um) are smaller than those in structure A(Lg=0.9um) although the specific on-resistance of structure B(Lg=0.8um) is smaller than that of structure A(Lg=0.9um). The specific on-resistance of structure A(Lg=0.9um) is 9.5mΩmm^2.

If the Idlin degradation is suppressed within 10% in case that the drain voltage is 6.5V, in the structure B(Lg=0.8um), the stress time should be shorter than $4x10^4$sec, while in the structure A(Lg=0.9um), the stress time should be shorter than $2x10^3$sec. In fact, the drain voltage is 5V and the switching time is short in a period. Therefore the lifetime in the structure B is longer than 4 $x10^4$sec.

Comparing with structure A, structure B achieves high reliability without sacrificing the characteristic of the specific on resistance.

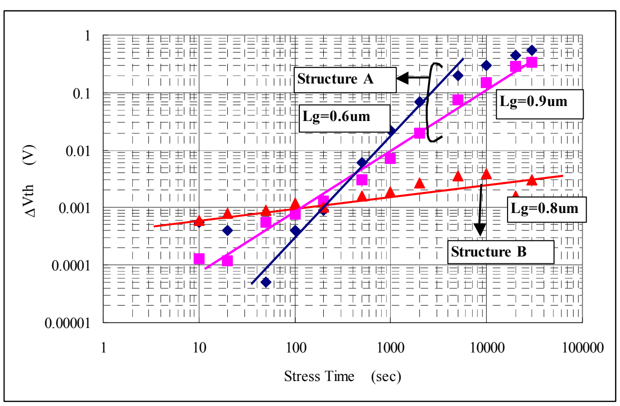


Figure.7A The degradation characteristic of threshold voltage shift as a function of stress time. The device is stressed at Vds=6.5V and Vgs=3.2V. Comparing with structure A, structure B achieves better reliability.

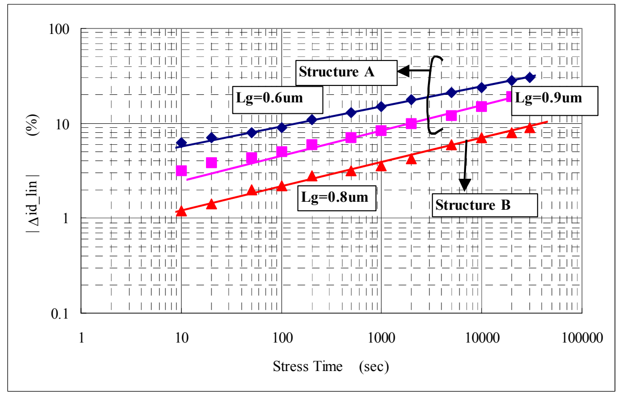


Figure.7B The degradation characteristic of drain current at linear region as a function of stress time. The device is stressed at Vds=6.5V and Vgs=3.2V.

Static and dynamic characteristics of a large area device

Figure 8 shows the micrograph of fabricated Nch MOSFET chip based on 0.6um CMOS process. The effective area is $1.8mm^2$. Three metal layers having 3um thick top metal layer are utilized.

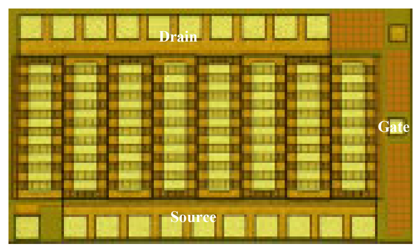


Figure.8 A micrograph of fabricated Nch MOSFET chip based on 0.6um CMOS process. The effective area is 1.8mm2.

Figure 9A shows the output characteristics of a large area Nch device. The on resistance is 8.5mΩ when the drain current and the gate voltage is 6A and 5V, respectively. The specific on-resistance of the device is approximately 15mΩ mm^2. This indicates that the metal interconnect resistance is 7mΩmm^2. The metal interconnect resistance is equivalent to the pure on-resistance of MOSFET.

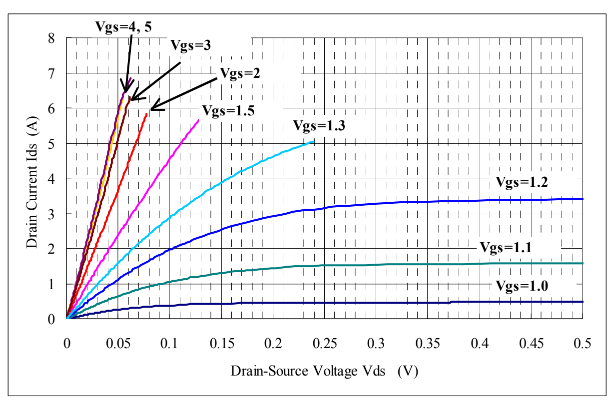


Figure.9A Output characteristics of the structure B. The on resistance is 8.5mΩ when the drain current and the gate voltage is 6A and 5V, respectively.

Therefore it is important to reduce the metal interconnect resistance. Figure 9B shows the output characteristics of a large area Pch device (the effective area 1.8mm^2). The on resistance is 19mΩ when the drain current and the gate voltage is -6A and -5V, respectively.

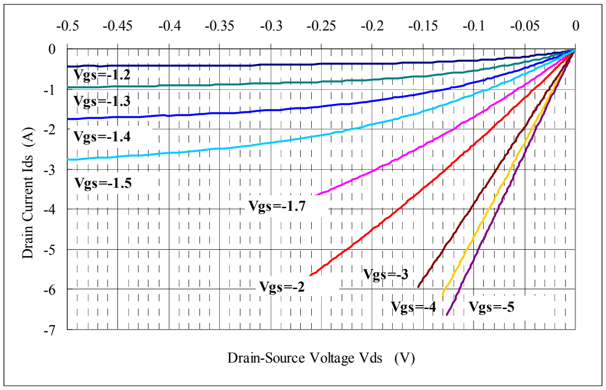


Figure.9B Output characteristics of Pch MOSFET. The on resistance is 19mΩ when the drain current and the gate voltage is -6A and -5V, respectively.

Figure 10 shows the switching characteristics of the structure B at the condition of a resistive load. The device indicates high current switching capability of more than 7A.

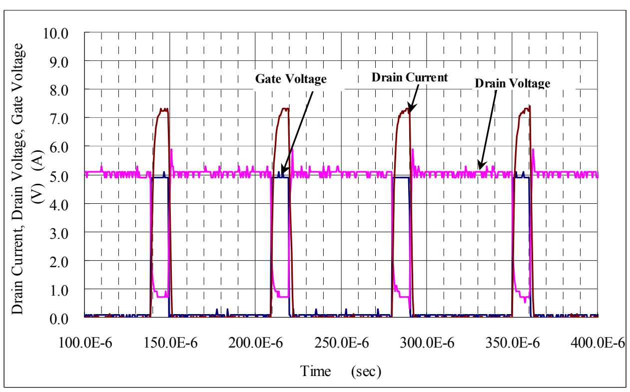


Figure.10 Switching characteristics of the structure B at the condition of a resistive load. The effective area is 1.8mm^2. The device indicates high current switching capability of more than 7A. The on-state drain voltage is high because the wire resistance except the metal interconnect resistance on chip is large.

The specific on-resistance is plotted in Fig. 11, in comparison with the state of the art LDMOS[2-4]. The blocking voltage and specific on-resistance in Pch MOSFET is 8.4V and 21.1mΩmm^2 at W=54um, respectively. Although the hot-carrier degradation is improved, the on-resistance of structure B is still on the same line of the state of the art LDMOS based on 0.35-0.6um process.

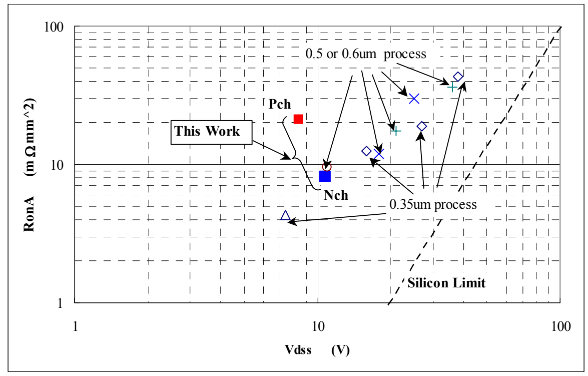


Figure.11 The comparison of the results with those of the state of the art LDMOS in RonA plot. The specific on-resistance of structure B is plotted. The hot-carrier degradation is suppressed in Structure B, and the on-resistance of the structure is the same as that of the state of the art LDMOS.

Conclusion

The developed power CMOS structures have successfully suppressed the hot carrier induced degradation and achieved the 10 years reliability without sacrificing the characteristic of the specific on resistance. It can also be fabricated without any additional process, based on low cost 0.6um CMOS process.

References

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