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Three-Phase Sinusoidal Current PWM Brushless Motor Driver ICs

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Abstract

This paper reports a newly developed single packaged IC, integrating 500V 1A one chip inverter IC and its controller chip. The developed ICs greatly reduce the footprints and realize an optimized solution for sinusoidal current PWM drive of DC brushless motors.

Introduction

Inexpensive and easy drive AC motors have conventionally been adopted for air conditioner fan motors or water pumps for household use. Technical improvement has continuously being made to reduce the power consumption and to achieve silent operation.

DC motors are effective to increase power efficiency. We developed DC motor driver ICs, implementing a PWM technique for sinusoidal current drive in 2000.

In the present paper, we report a newly developed single packaged ICs, integrating 500V 1A one chip inverter IC and the aforementioned controller.

500V SOI 1 Chip Inverter ICs

History and Background

First, we briefly review Toshiba's development history of 500V single chip inverter ICs. The chip photos are seen in Fig.1. The first 500V 1A chip was developed in 1991, using the sophisticated 50um thick SOI layer[1]. Each high voltage device was dielectrically isolated by deep V grooves. Low voltage control circuits were formed in a single isolated island and each low voltage device was isolated by conventional junction isolation within the island. Since the fabrication process included wafer bonding, epitaxial growth, V groove etching, poly-silicon filing etc., it was complicated and not cost efficient.

In 1990, we proposed, for the first time, the high voltage SOI device structure.[2], using trench isolation and a thick buried oxide film. Deep trenches realize dense high voltage device integration with BiCMOS circuits. When a high voltage is applied to the high voltage device, the buried oxide itself supports a large part of the voltage[2,3]. The buried oxide serves as a part of the high voltage device and the structure is widely recognized as SOI Resurf.

In 1994, we successfully developed 500V 1A single chip inverter ICs based on 1.5um BiCMOS technology[4]. At that time, we assumed that the system integration would be the main stream, and that even CPUs would be integrated in high voltage power IC chips in the next generation. High voltage lateral devices were fabricated based on 1.5um CMOS process. We abandoned diffusion self-alignment DMOS process at that time and adopted fully CMOS compatible process for the high voltage MOSFETs.

Recently, however, we have realized that the cost optimization is the first priority and that the high level functionality can be located outside the chip, if logic level interface is provided.

In view of these situations, we have re-developed new simplified low cost SOI power IC families by adopting 30V CMOS analog control circuits. The fabrication processes have been greatly simplified by completely excluding bipolar transistors. The chip includes only five kinds of devices: n-ch lateral IGBTs, Diodes, 30V CMOS, and HVNMOS. Thus, the fabrication process was greatly simplified. The schematic cross section of the power ICs is shown in Fig.2.

Process Optimization for 500V 1A Inverter IC Chip

This section reports development of low cost 500V 1A 3-phase 1 chip inverter ICs.

Excluding bipolar transistors in the control circuits greatly increases the system reliability, because bipolar transistors ofen causes malfunction of the circuits.

The reason why the bipollar devices isn't fabricated is following. The dV/dt current, caused by the low side IGBT turn-off, flows through the buried oxide and may cause malfunction of bipolar device in the high side driver.

Figure.3 (a) and (b) show how the dv/dt current flows and causes malfunction in lateral PNP transistor of high side. Figure.3 (a) shows the deletion layer inside the PNP transistor in a driver circuit for high side IGBTs, when the base emitter bias is zero and the PNP is in the off-state. When the low-side IGBT is turned-off, the voltage of whole silicon islands of the driver circuit is elevated to a high voltage level, and the depletion layer is created from the bottom oxide. Once the depletion layer merges the depletion layer, which is originally created around the p+ collector layer, hole are injected and an hole inversion layer is created on the bottom oxide, as shown in figure.3(b). Alhough the PNP is off-state, the collector current flows and the wrong signal is passed to the next step ciruits.

The influence of the dV/dt current on CMOS devices is less than that on bipolar devices because the active region is only surface in the MOS device.

In the folowing, the developed lateral IGBT characteristics are breifly shown. Figures 4 and 5 show I-V curves and the switching waveforms of 0.5A drain current at room temperature. Forward voltage drop is 2.0V for 0.5 amperes of the drain current. The fall-time is 400nsec.

Figure 9 shows a block diagram of the fabricated inverter ICs. The bootstrapping technique is adopted as the internal high side voltage source. The circuits include drive circuits for LIGBTs, bootstrap diode, logic circuits, PWM circuit and various protection circuits. The protection circuits include under-voltage, over-current and over- temperature protections.

Figure.1 includes a developed 500V 1A single chip inverter IC. The chip size is $4.1 \times 6.6 mm^2$.

Sinusoidal Current PWM Driver IC

Hardware logic implementation of sinusoidal current generation PWM control

Sinusoidal current drive by PWM technique has conventionally been realized by MCU or DSP. The present controller provides the same function by hardware logics based on 12V BiCMOS process, realizing low cost and simplified system, eliminating firmware design.

Figure 9 also shows the block diagram of the whole ICs. The controller output signals are generated based on the hall-IC signals, detecting the rotor position. Using the divided clock signals, every 60 degree electric angles, detected by three hall ICs, are counted by up-counters. The counted numbers are held by latches, and then used as initial values in down-counters, in order to predict and create the next 60 degree angles for the motor drive. Two-phase modulation waveforms are generated by 5bit D/A converters, which convert the counted/held numbers into analog voltage. The voltage amplitude is determined by the external input signal. The final two-phase PWM signals are obtained by comparing the generated two-phase modulation waveforms and the triangular waveforms, simultaneously generated by D/A converters.

The controller also provides dead time control of high and low-side LIGBTs, lead angle compensation function for the current phase delay by the motor induced voltage, user selection capability of triangular wave frequency.

Figure 6 compares the fan motor noise levels of air-conditioner as a function of rotation speed, when the motor is controlled by the sinusoidal wave current, using the present driver ICs. The noise level is decreased by 10dB for 600rpm, as compared with the noise level which generated by the conventional 120 degree square-wave drive.

Figure 7 compares efficiency of the drive methods. 3 % improvement was obtained by optimizing the LIGBT switching timing using the lead angle compensation function.

We developed original TB6539 controller in 2000, low voltage version of TB6551 in 2002, and TB6556 implementing automatic lead angle compensation function.

2 in 1 package

Single package solution is strongly effective to reduce the device footprint, eliminating the wirings between the controllers and the high voltage power ICs. The total mounting area consumption can be greatly reduced. Although one chip solution using the SOI process is possible, the total chip size becomes larger, and the two-chip solution is more advantageous from the cost point of view.

We have developed 1 package solution, integrating 500V 1A high voltage SOI inverter chip and TB6551 in HZIP-25 package. Figure 8 illustrates the over view of the package. There are two beds in the metal frame, where the two chip are mounted. The wirings between the two chips are made by direct wire bonding, reducing the pin counts to 25. The metal frame is directly connected the package fin, achieving the low thermal resistance.

Conclusion

We have developed 1 package solution, integrating a 500V 1A high voltage SOI inverter chip and a sinusoidal current PWM driver, TB6551 in HZIP-25 package. Next step will be implementation of automatic lead angle compensation function and an increase in the current rating of SOI power ICs.

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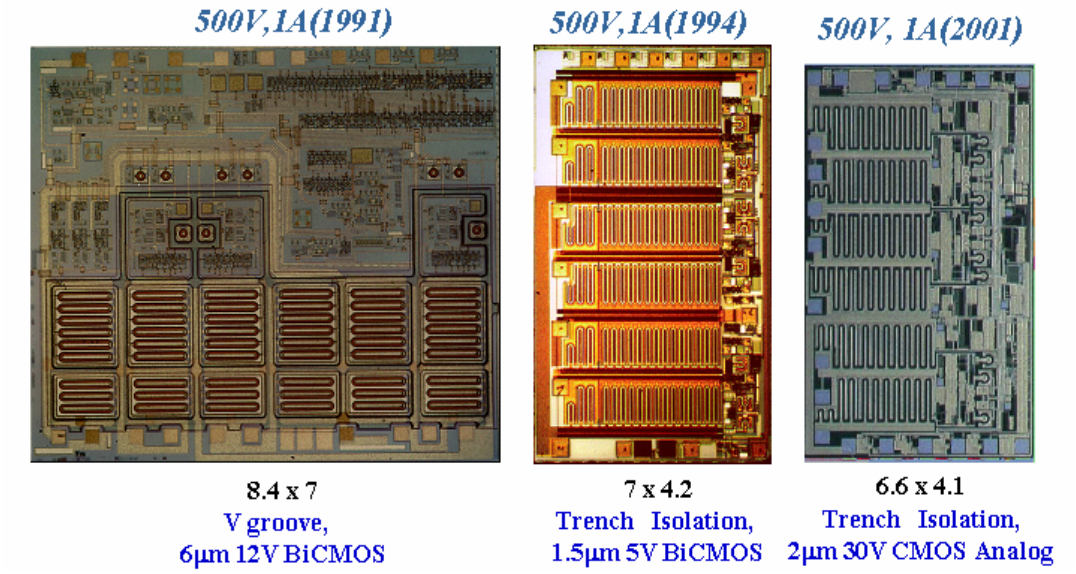

Fig.1 Evolution of 500V 1A 1 chip Inverter ICs

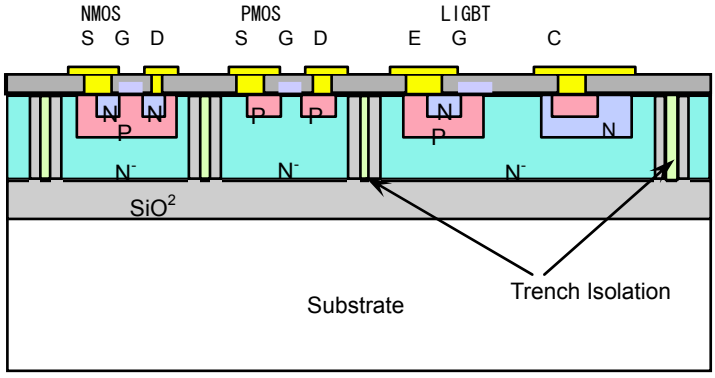

Fig.2 Schematic cross-section of 500V SOI devices

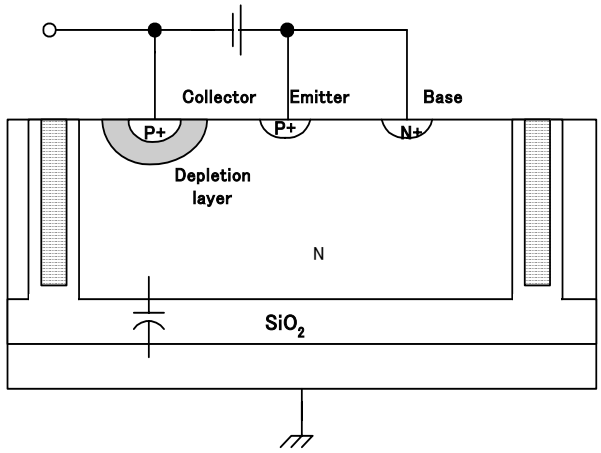

Fig3(a) Off-state of PNP in high side driver

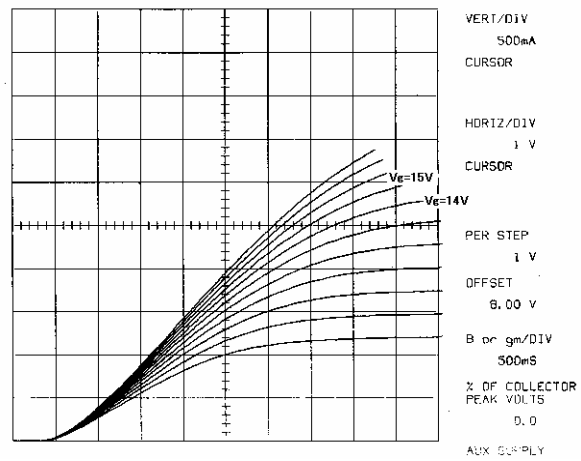

Fig.4 Current Voltage Curves of 500V LIGBT
(Current:500mA/Div, Voltage: 1V/Div)

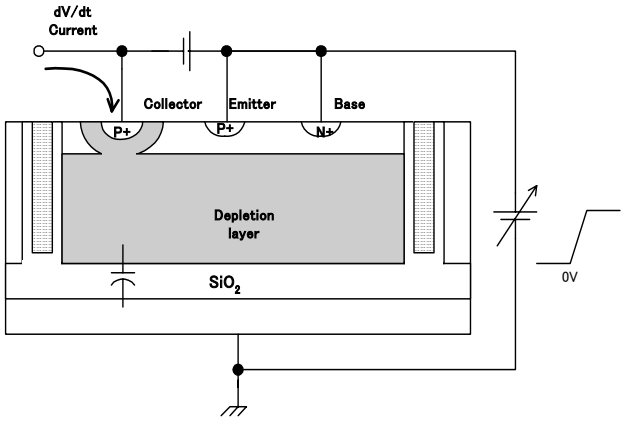

Fig3(b) Merged depletion layer due to elevation of silicon island voltage.

Fig.3 dV/dt current flowing mechanism in a trench isolated island

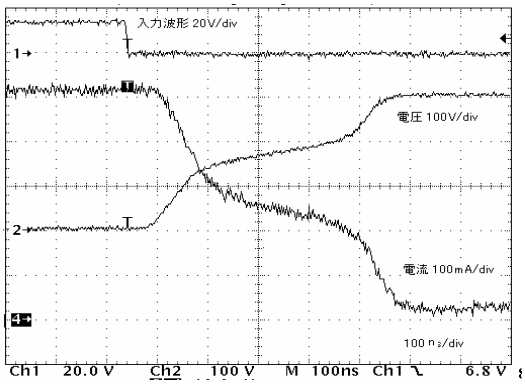

Fig.5 Switching Waveforms of LIGBT
(Voltage: 100V/Div, Current: 100mA/Div)

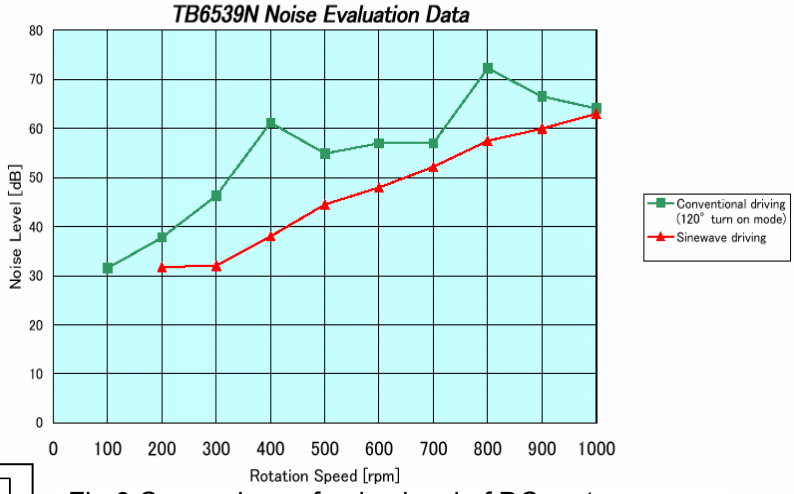

Fig.6 Comparison of noise level of DC motors between sinusoidal drive and conv. drive.

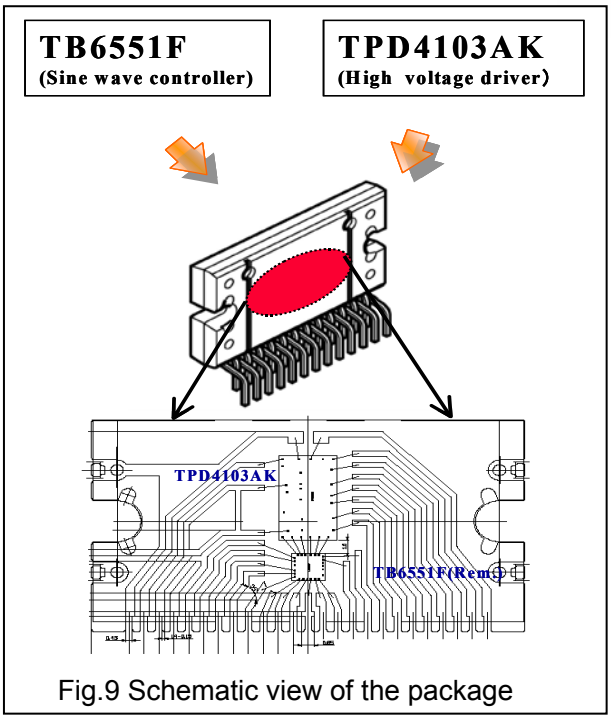

Fig.9 Schematic view of the package

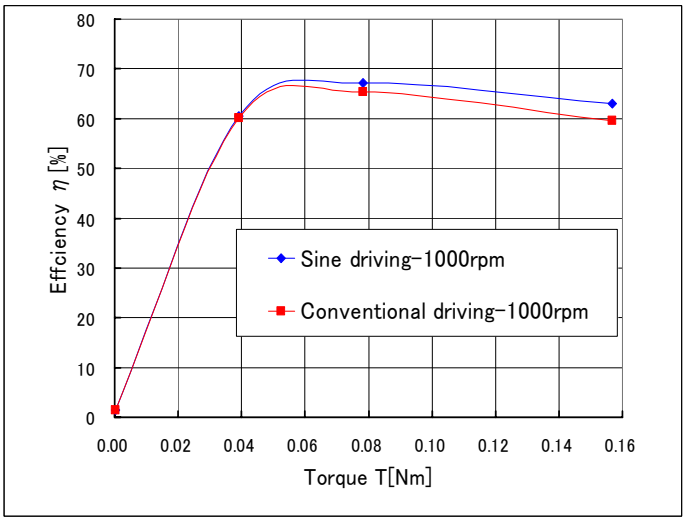

Fig.7 Efficiency comparison between sinusoidal drive and conv. drive

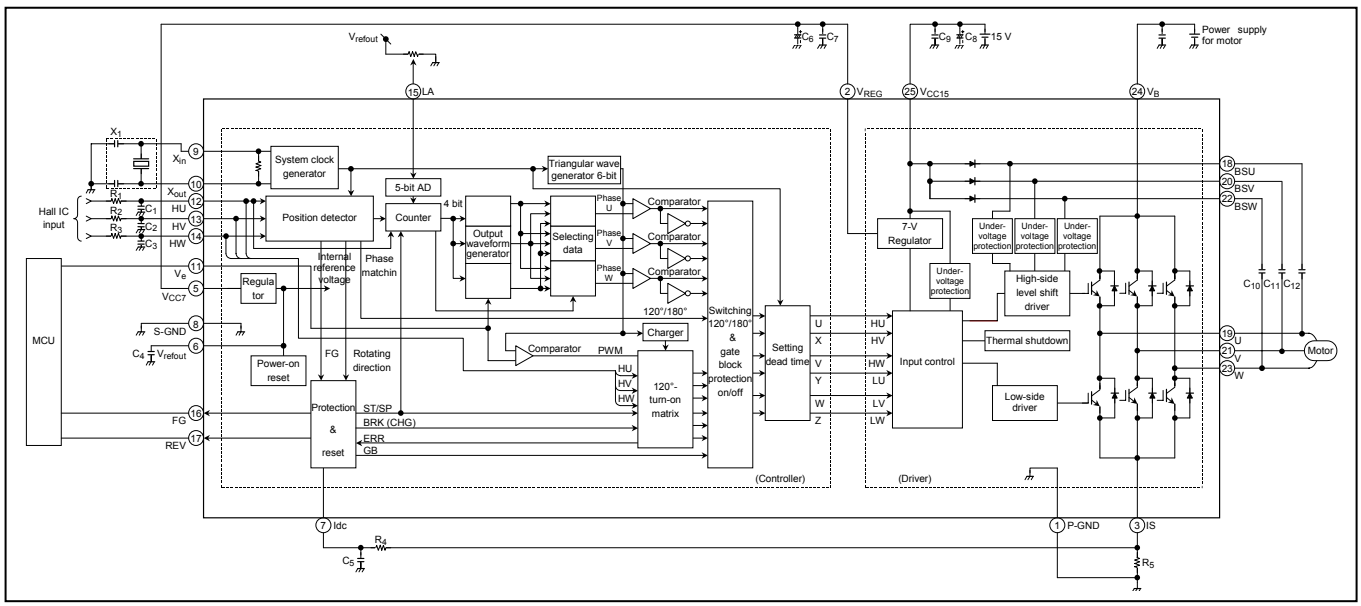

Fig.8 Circuit block diagram of controller and 1 chip inverter.