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30V Sub-micron Shallow Junction Planar-MOSFET for DC-DC Converters

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ABSTRACT

We present Sub-micron Shallow p-base Planar-DMOSFET (DMOS: Double Diffused MOSFET type) for DC-DC converter application. The shallow junction depth is quite useful to reduce the device on-resistance. It was found that the gate-drain feedback charge can effectively be reduced by adopting very narrow and shallow JFET region with very high JFET donor concentration, based on the charge compensation theory.

An experimental planar DMOSFET with p-base depth of 0.8um exhibited a breakdown voltage of 34V, a Ron*Qgd of 14.9mΩnC, and good UIS capability. This is the best value, ever reported for 30V planar DMOSFET structure.

I. INTRODUCTION

Clock speed of CPU is increasing year-by-year, and the operating voltage and current is expected to be 1 V and more than 100 A in 2006. In order to reduce the loss in high frequency operation, it is quite important to improve switching characteristics of MOSFET to meet the requirements for such DC-DC converters. The product of on-resistance (Ron) and gate-drain feedback charge (Qgd) is conventionally used as figure of merit for high speed MOSFETs. Recently, many studies about MOSFET for DC-DC converters were carried out and most of them adopted trench structure [1-2]. Main challenge of trench MOSFET for DC-DC converters is to reduce its gate-drain charge.

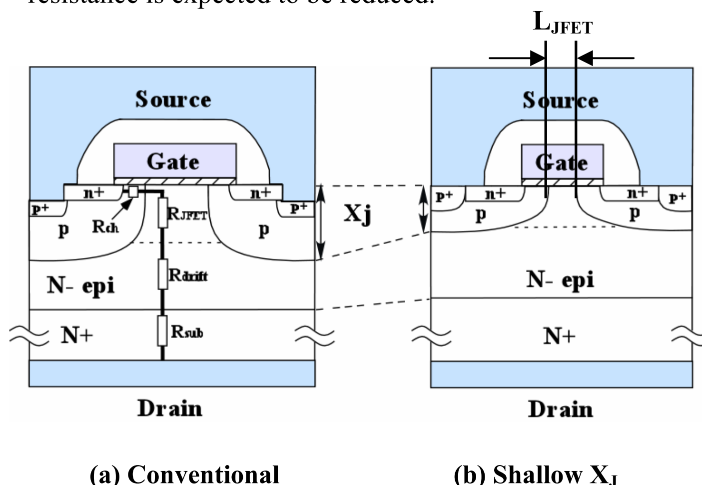
LDMOS is characterized by the low gate-drain charge because of the minimized overlap of gate poly and drain region by the self-alignment method. The disadvantage in LDMOS structure is relatively high on-resistance and its complicated fabrication process [4-5].

Planar MOSFET can reduce gate-drain charge although its on-resistance is relatively high because of the JFET resistance. The advantage is that the structure does not require the complicated fabrication processes as compared with trench MOSFET or LDMOS.

In this paper, we experimentally examine, for the first time, the high speed switching capability of planar MOSFET for DC-DC converter application when the p-base junction depth is decreased to the level of sub-micron regime.

II. DEVICE DESIGN AND SIMULATION

Figure. 1 shows a cross-sectional view of a conventional and developed sub-micron shallow p-base junction (X_J) planar MOSFET, respectively. As shown in the figure, on-resistance is mainly consists of channel, JFET, n-epitaxial layer (drift), n+substrate and package. Generally, on-resistance of planar MOSFET is higher than that of trench MOSFET because of its large JFET resistance. However, when JFET width and JFET depth decrease and JFET donor density increases, JFET resistance is expected to be reduced.



(a) Conventional **(b) Shallow X_J**

Figure.1 Cross-sectional view of a conventional p-base structure and sub-micron shallow X_J planar MOSFET. As for JFET, impurity dose is (a) < (b), width is (a) > (b).

The maximum donor concentration in the JFET region can be determined by the same equation as the charge compensation devices if the JFET region width (L_{JFET}) is sufficiently small:

$$N_{MAX;JFET} = Q_{RESURF} / L_{JFET} \qquad (Q_{RESURF} : const.)$$

JFET channel resistance R_{JFET} is approximately proportional to the junction depth, X_J:

$$R_{JFET} \propto X_J / (N_{MAX;JFET} L_{JFET}) = X_J / Q_{RESURF}$$

Thus, planar MOSFET with shallower p-base junction and narrower and higher dose JFET region is expected to improve its on-resistance. The gate-drain charge can simultaneously be decreased by decreasing the JFET width.

Figure. 2 shows the dependence of gate-drain charge (Qgd), on-resistance (Ron) and the product (RonQgd) on the p-base junction depth. The data in the figure are simulated results for the optimized structure for each p-base junction depth, i.e., each parameter such as gate length, JFET impurities concentration and epitaxial layer thickness are optimized for each p-base depth. As the depth of the p-base is shallower, both the JFET and channel resistances decrease. RonQgd is expected to be improved by more than 25% by reducing the p-base depth from 2.0um to 0.8um.

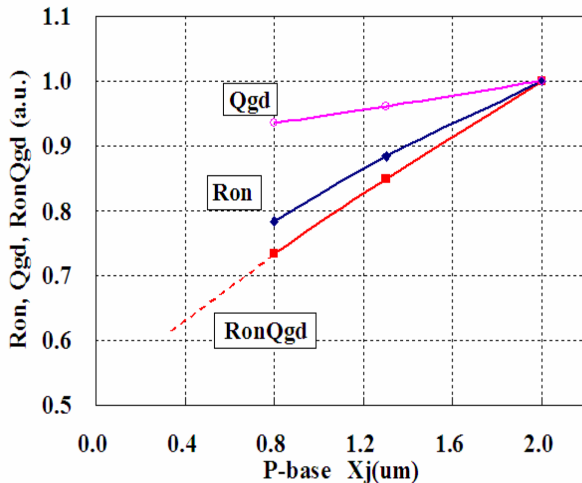


Figure.2 Calculation result of dependence of Ron, Qgd, and RonQgd on the depth of p-base.

III. RESULTS AND DISCUSSION

We have successfully fabricated planar MOSFETs with a p-base as shallow as 0.8um. P-base and n+ source region were formed using the technique of the double diffused self-align process which uses gate poly silicon as a mask, and the shallow junction depth was obtained by controlling implantation method and diffusion time. Figure.3 shows an experimental result of on-resistance and RonQgd as a function of gate length for the each case for 0.8, 1.0, and 1.2um of p-base junction depth. The gate-drain charge decreases linearly, as the gate length becomes shorter. The on-resistance rises rapidly when the gate length decreases to a critical value. RonQgd takes its minimum value when the gate length is an optimum value, which is slightly larger than the critical value. It is possible to simultaneously reduce the on-resistance and the gate-drain charge as p-base junction becomes shallow.

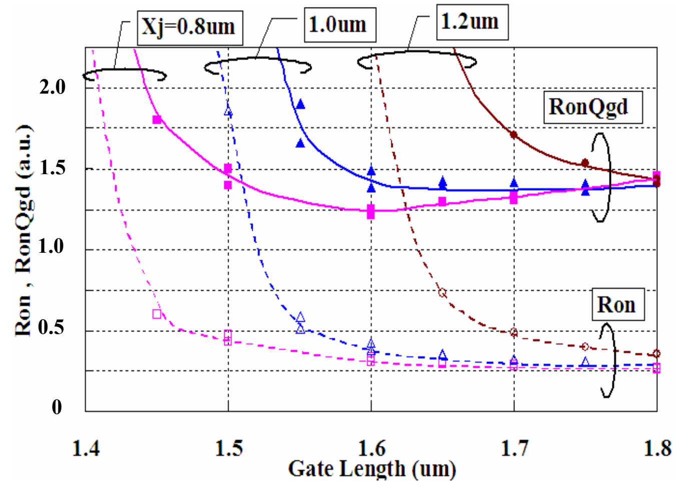


Figure.3 Experimental result of Ron and RonQgd as a function of gate length. For each X_J condition, the fabrication process and a cell pitch are fixed.

Figure. 4 shows the optimization of the JFET dose. The solid line represents the characteristics of MOSFETs with higher JFET dose, which is higher than that of the MOSFETs represented by the broken line in Fig.4. The improvement of RonQgd values is accomplished by the narrow and higher concentration JFET region. The gate-drain charge decreases, as the gate length decreases, however, RonQgd value increases rapidly when the gate length is excessively reduced to below the critical value.

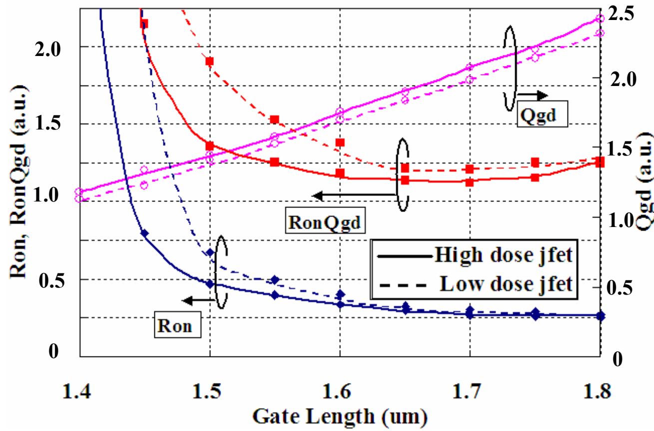


Figure.4 Dependence of the Ron, Qgd, and RonQgd on the gate length. The solid line represents the characteristics of MOSFETs with higher JFET dose, which is higher than the dose of the MOSFET represented by the broken line.

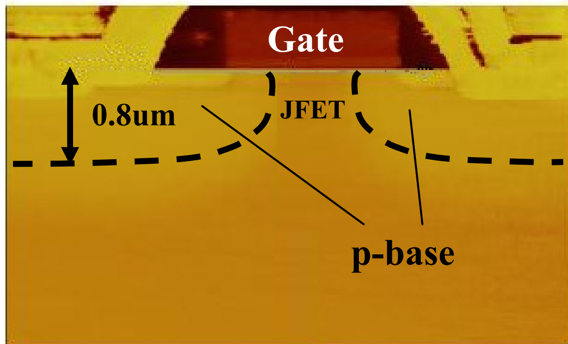


Figure.5 Cross section of fabricated shallow junction planer MOSFET.

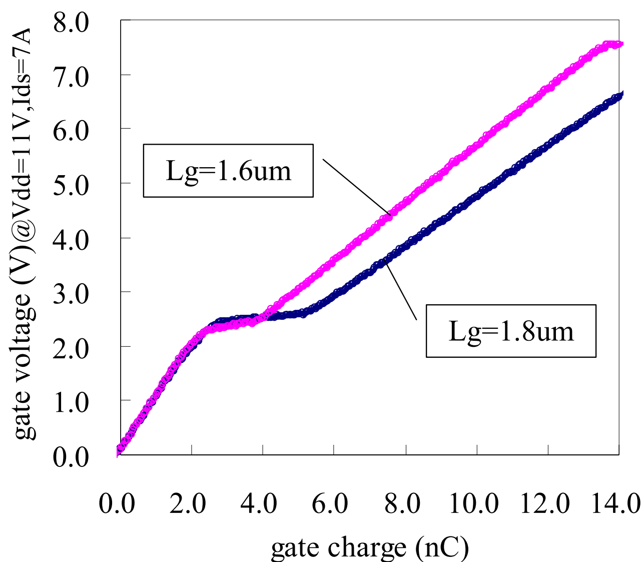


Figure.6 Dependence of gate charge waveform on the gate length for 0.8um of p-base depth.

Figure. 5 shows a cross-section of the fabricated shallow junction planer MOSFET. More than 34V of breakdown voltage is obtained when the p-base junction is as shallow as 0.8um. In case of fixed p-base depth, the breakdown voltage decrease when JFET length decrease because wider JFET region is less depleted and make electric field of this region increase. The waveforms of gate charge in case the gate length is 1.6um and 1.8um are shown in Fig. 6. By narrowing the JFET width, the gate-drain charge is improved from 2.5nC to 1.35nC.

The measured characteristics of developed 0.8um of p-base junction planar MOSFET are shown in Table1. The gate length and the cell pitch of this device are 1.6um and 5.0um, respectively. Although it has high doping concentration JFET region, since its width is formed less than 0.5um, the JFET region is easily deplete when drain voltage is applied. For this reason, low gate-drain charge and high breakdown voltage were achieved. The on-resistance is 11.0mΩ at the case of Vgs=7V. The RonQgd of the developed 0.8um of p-base junction planar MOSFET was achieved as low as 14.9mΩnC.

Although its p-base is shallow, the developed devices have achieved the outstanding avalanching capability under unclamped inductive switching. The measured avalanche capability was more than 30A for the active FET area 4.7mm^2 as shown in Fig.7.

Figure. 8 shows a comparison of the developed planar MOSFET with previous works. Compared with the conventional planar MOSFET, 30% of Ron*AA improvement was shown by forming 0.8 um p-base junction. Furthermore, by adopting narrow and higher concentration JFET region, 25% or more of Qgd/AA improvement was also obtained. The developed device has achieved excellent characteristics, which is comparable to the LDMOS. It was shown that planar MOSFETs with sub-micron shallow p-base junction have a great potential for high speed switching MOSFET for DC-DC converter application.

Table.1 Measured characteristics of the shallow X_J planar MOSFET

Active FET area	4.7 mm^2
Breakdown Voltage	34 V
Gate Threshold Voltage	1.45 V
Ron(Vgs=7V,Ids=7A)	11.0 mΩ
Qgd(Vdd=11V)	1.35 nC
RonQgd	14.9 mΩnC

Ron: on-resistance without PKG

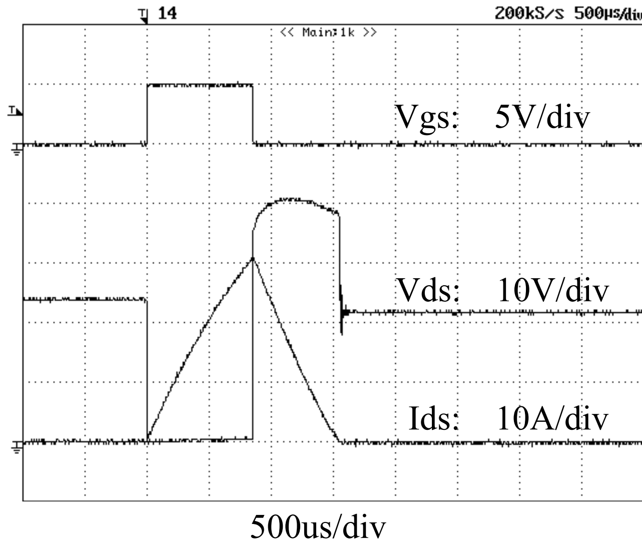


Figure.7 Wave forms of unclamped inductive switching with rg=25Ω and L=500uH about the structure of 0.8um of p-base junction depth.

IV. CONCLUSIONS

We investigated the capability of planar MOSFET with sub-micron shallow p-base junction for high speed switching. It was shown that fabricated planar MOSFET with shallow p-base junction and high doping narrow JFET region achieved 34V of breakdown voltage, 14.9mΩnC of RonQgd, and 30A of UIS turn off capability, this result is comparable to that of trench MOSFET or LDMOS. We demonstrated that planar MOSFETs with sub-micron shallow p-base junction have a great potential for high speed switching MOSFET for DC-DC converter application.

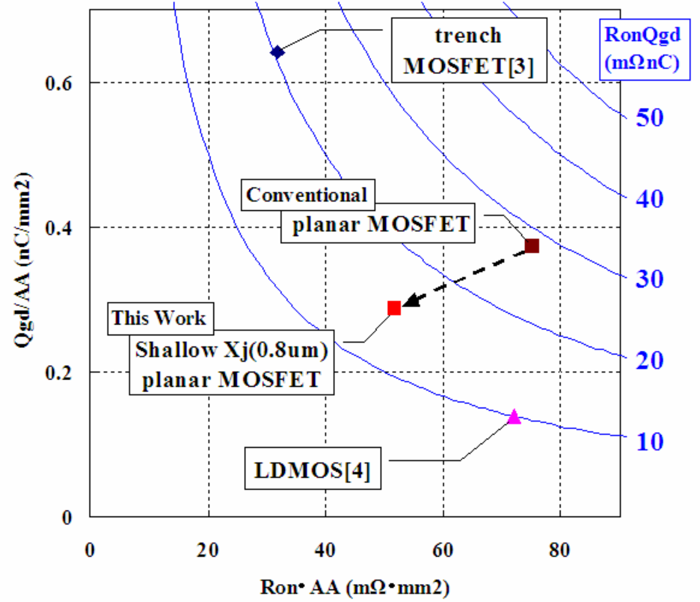


Figure.8 Comparison of the characteristics of developed shallow X_J planar MOSFET with previous works.

V. ACKNOWLEDGEMENTS

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