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MOSFET-mode Ultra-Thin Wafer PTIGBTs for Soft Switching Application --- Theory and Experiments

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Abstract

We have proposed and analyzed MOSFET-mode operation of ultra-thin wafer PTIGBTs in ISPSD'02[1]. The present paper, for the first time, presents analytical theory of MOSFET-mode operation, and shows that the SOA is determined by a mechanism similar to the second breakdown of npn bipolar transistors.

The present paper also experimentally demonstrates, for the first time, that the MOSFET-mode IGBTs are strongly effective for soft switching application. The developed MOSFET-mode 900V 60A thin wafer Trench Gate PTIGBTs have reduced turn-off loss by 55% at 125°C, compared with the conventional (4th generation) soft switching PTIGBTs.

MOSFET-mode Operation

MOSFET-mode operation is defined in such a way that the anode efficiency γ is less than γ_{MOS}, which represents $\mu_p/(\mu_n + \mu_n)$. The anode efficiency γ is defined as the ratio of the hole current over the total current ***at the n-base n-buffer junction***, being identical to the product of p-emitter injection efficiency γ_{PE} and transport factor in the n-buffer α_T. (Please note that γ in the present paper is different from the conventional injection efficiency of the p-emitter.)

The γ_{MOS} value dynamically changes as the electric field changes inside the device because the mobility μ is a function of the electric field. Figure 1 shows γ_{MOS} as a function of electric field. IGBTs may change its operation mode as the forward voltage increases and the electric field inside the device increases.

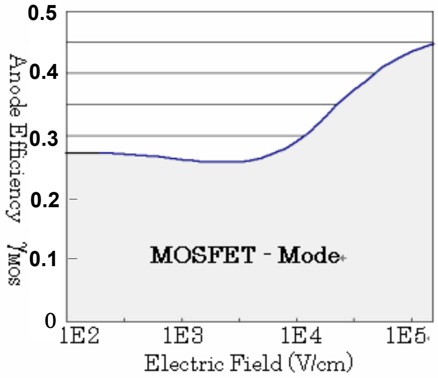

Fig.1 Area for MOSFET-mode operation.

In the MOSFET-mode operation, several unique characteristic features are distinguished. The features are very similar to the operation of pure MOSFETs.

A. Theory of Forward SOA of Thin Wafer PTIGBTs

In a very high forward biased operation, a high electric field initially appears in the p-base n-base junction. However, the high field may appear in the anode side as shown in Fig.2 when the current density is high. The reason is described in the following.

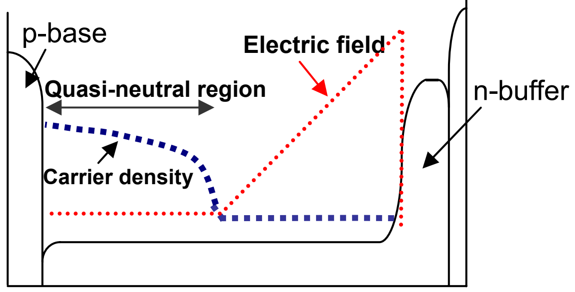

Fig.2 High electric field region appears in anode side for high current density cases.

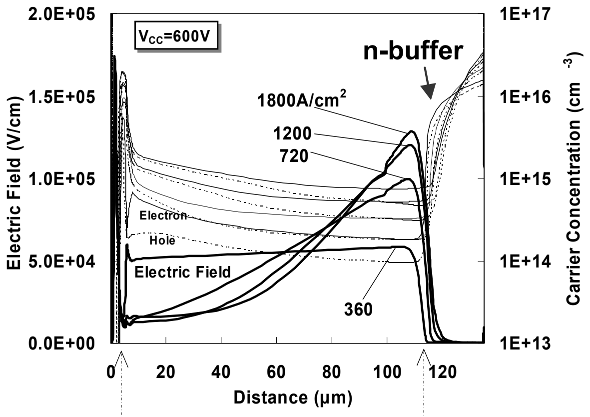

Fig.3-1 Simulated electric field distributions with current density as a parameter when forward voltage =600V. High electric field appears in n-base n-buffer junction.

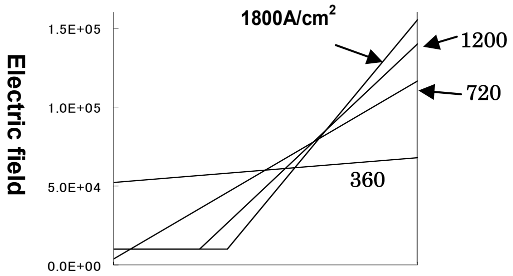

Fig.3-2 Analytically calculated electric field inside n-base. 10E4 is assumed in neutral region, as high current flows.

As the carrier lifetime in the n-base is designed to be sufficiently high in thin wafer PTIGBTs, the ratio of the hole current density(J_p) over the total current density(J) is assumed to be the same throughout the high field region. The ratio is equal to the anode efficiency: γ, if the high field reaches the n-base. The electron and hole densities can be calculated by the following equations in the high field region.

$$\gamma = J_p/J, \quad p = J_p/qv_h, \quad n = J_n/qv_e,$$

where p and n denote hole and electron densities, v_h and v_e denote hole and electron saturation velocities, respectively. The net charge in the high electric field region ρ is given by Eq.(1) with the donor density N_D.

$$\rho = N_D + p - n = N_D + (\gamma/v_h + (\gamma - 1)/v_e)J/q, \ \ldots \qquad \text{Eq.(1)}$$

$$\gamma_{MOS} = \mu_p/(\mu_n + \mu_n), \qquad \ldots\ldots\ldots\ldots\ldots\ldots \qquad \text{Eq.(2)}$$

$$\gamma_{MOS} = v_h/(v_h + v_e) \qquad \text{for high field case} \ \ldots. \qquad \text{Eq.(3)}$$

If γ is lower than γ_{MOS}, the second term (mobile charge) is negative in Eq.(1). The net charge ρ decreases as the current density J increases, and eventually changes its sign when J exceeds the critical current density J_C.

$$J_C = qN_D/((1-\gamma)/v_e - \gamma/v_h) \ \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \qquad \text{Eq.(4)}$$

Once the net charge becomes negative, the peak high electric field shifts toward the n-base n-buffer junction. Figure 3-1 shows the TCAD simulated electric field distributions of 1200V thin wafer PTIGBTs, when the forward voltage is 600V. Analytically calculated results of Fig.3-2 agree well with the TCAD simulation results. The calculation procedure is described later.

The electric field is uniform when $J=J_C$. A very high electric field appears in the n-base n-buffer junction as J further increases. Avalanche breakdown will take place when the peak electric field in the n-base n-buffer junction exceeds the critical value E_C. This phenomenon is very similar to the second breakdown in npn bipolar transistors. The on-state breakdown voltage varies as the current density increases and the resultant net charge ρ changes.

γ value is not constant in actual devices and depends on the operating condition. In Fig.3, γ value changes from 0.28 to 0.36 as the operating current density increases. The reason is that a part of the n-buffer is depleted by the increased peak electric field in the n-base n-buffer junction. This results in increase in the transport factor (α_T) in the n-buffer.

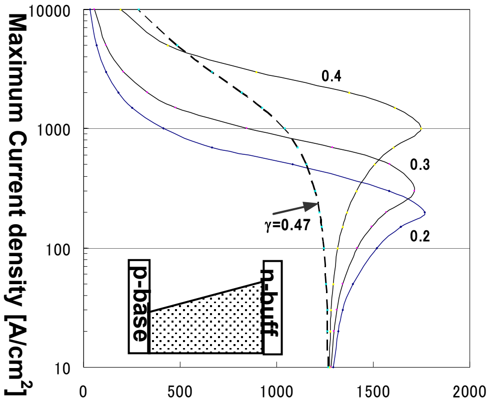

Fig.4 Analytically calculated forward SOA with γ as a parameter.(n-base width:100μm, N_D:7x10^{13} cm^{-3})

Figure 4 shows the analytically determined SOA locus for 1200V thin wafer PTIGBTs with anode efficiency γ as a parameter, when the n-base impurity density N_D of 7x10^{13}cm^{-3} and the thickness of 100μm is assumed. The breakdown voltage was calculated, assuming a step junction $p^+\pi n^+$ diode structure, where the dose of the π-region is assumed to be given by Eq.(1). It was also assumed that the breakdown occurs at the critical peak field E_C of 1.8x10^5 V/cm.

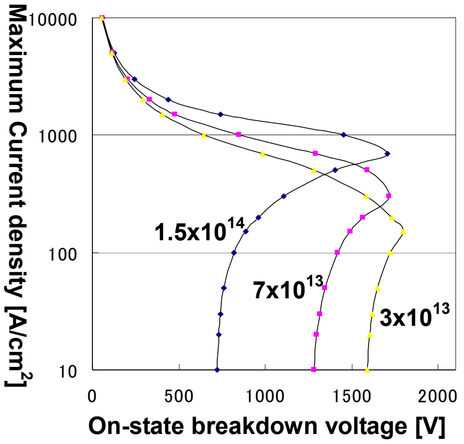

Fig.5 SOA dependence on n-base impurity density (N-base width:100μm)

From figure 4, it is predicted that the on-state breakdown voltage takes its peak value when the current density is equal to the critical current density J_C. It is also predicted that the short-circuit capability is significantly deteriorated for the devices with low γ. In the theory, an infinitely large SOA is predicted when γ is just equal to $v_h/(v_h+v_e)$ (=0.45).

If γ is greater than 0.45, the net charge in the n-base is always positive and the on-state breakdown voltage simply decreases as current density J increases[2].

Figure 5 shows the calculated SOA locus with donor density N_D as a parameter. It is predicted that a higher donor density improves SOA.

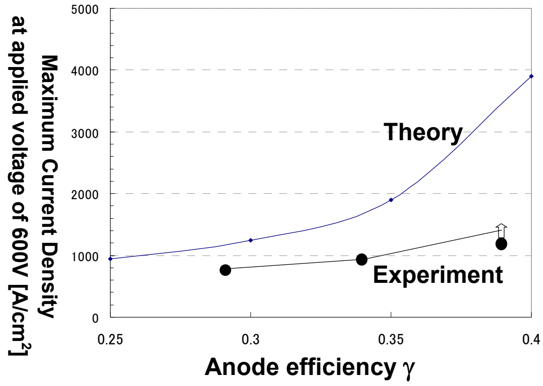

Fig.6 Comparison of theoretical max. current at Vcc of 600V and measured short-circuit withstand capability.

Figure 6 compares the theory and the experiment. It is predicted that short-circuit capability (high voltage forward SOA) becomes large as γ approaches $v_h/(v_h+v_e)$. Experimental results showed the same tendency as seen in Fig.6.

Another way of obtaining approximate breakdown voltage is to use the empirical equation:

$$V_{BD}=60(E_G/1.1)^{1.5}\{((1-\gamma)/v_n - \gamma/v_p)J/q - N_D\}^{-3/4}$$

although it is valid only for non-punch through cases.

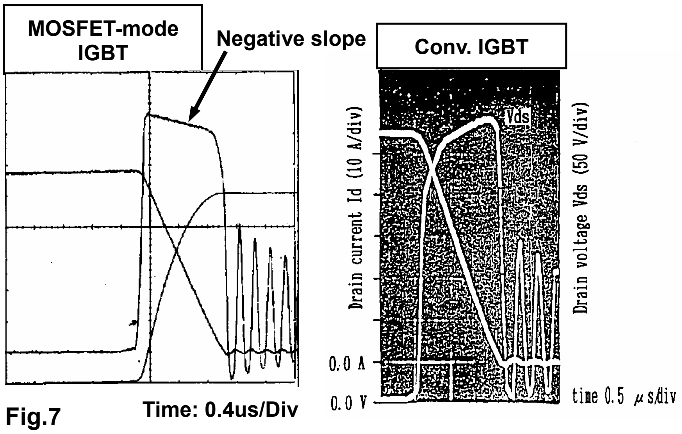

Fig.7 Time: 0.4us/Div
(a)Waveforms for sustaining operation of MOSFET-mode IGBTs. **(b) Sustaining waveforms of conventional IGBTs.**

B. MOSFET-like Sustaining Switching Waveforms

Sustaining (UIS) switching waveforms of MOSFET-mode IGBTs are very similar to those of MOSFET. For conventional IGBTs, the self-clamped voltage value increases as the drain current decreases. On the contrary, the self-clamped voltage decreases as the drain current decreases in the MOSFET-mode operation as seen in Fig.7.

Figure 8 shows the calculated static breakdown current voltage curves. It is clearly seen that the breakdown voltage increases as current density increases in MOSFET-mode devices while the current density is below Jc. This is the main reason for the phenomenon.

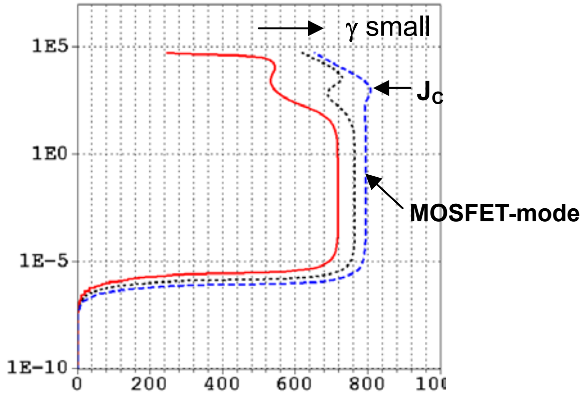

Fig.8 Static breakdown characteristic curves with γ as parameter

C. Degradation of Sustaining Current Capability

Sustaining current or UIS capability was degraded considerably in the MOSFET-mode thin wafer PTIGBTs. The experimental results are shown in Fig.9 for 600V devices. The degradation of the sustaining current capability occurred when the anode efficiency became less than 0.45 as seen in Fig.9. This value coincided with the criteria of γ_{MOS}: $v_h/(v_h+v_e)$ for MOSFET-mode operation[3].

The reason for the degradation is described in the following: The highest electric field appears initially in the center junction (p-base n-base junction) in the turn-off transients (see Fig.10), since the operating current density is lower than the critical current density Jc. The critical current density is sufficiently larger than the operating current density in 600V devices as the typical N_D is chosen to be above 10^{14}cm^{-3}. After sufficient avalanching phenomena take place, the current concentration may occur and the local current density exceeds the critical current density Jc. Then, a high electric field also appears in the n-base n-buffer junction, as shown in Fig.10, in the current concentrated area. This spatial change of the high electric field region accelerates the current crowding.

Fig.11 compares the critical current density J_C and the sustaining current density capability. The failure occurred well below the critical current. This implies the current crowding.

In the conventional IGBTs, the peak electric field always exists in the p-base n-base junction for any current density. Thus, the sustaining current capability is not degraded.

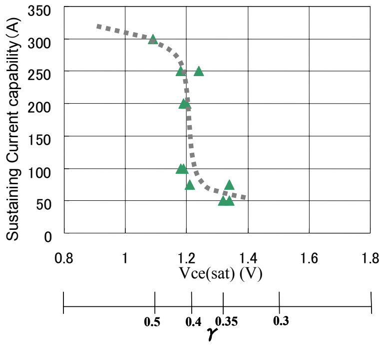

Fig.9 Sustaining current capability degraded as anode efficiency γ decreases. Data for 600V thin wafer PTIGBTs.

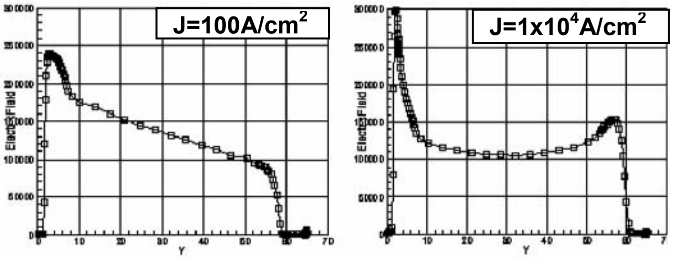

Fig.10 The electric field distribution inside 600V MOSFET-mode device. The peak electric field initially appears at the center junction (left hand figure.) A high electric field appears also in the n-base n-buffer junction as current density exceeds J_C as seen in right hand figure.

It should be noted that the difference between the short-circuit operation and the sustaining mode operation is the origin of electron current. In the short-circuit case, the electron current is supplied by the channels and is uniformly distributed throughout the chip area. In the sustaining mode operation, the electron current is created by avalanche phenomenon, and, thus, is not uniform.

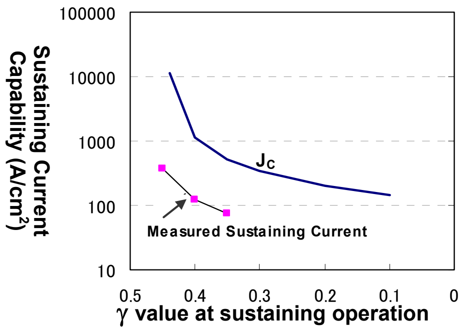

Fig.11 Measured sustaining current capability and J_C are compared as a function of γ

Development of MOSFET-mode Thin Wafer Trench Gate PTIGBTs for Soft Switching Application.

The present paper, for the first time, experimentally demonstrates that the MOSFET-mode IGBTs are strongly effective for soft switching application. We have developed 900V 60A thin wafer Trench Gate PTIGBTs with very low anode efficiency.

Figure 12 compares the current voltage curves between the developed MOSFET-mode IGBTs and conventional devices.

The tail current was significantly reduced in ZVS (zero voltage switching) circuits, adopted for microwave ovens, as shown in Fig.13. This is because the stored carriers are removed in the storage time period, in the MOSFET-mode operation, as explained in the ISPSD02 paper [1]. Thus, the tail current is reduced. The measured turn-off loss was reduced by 55% at 125°C, compared with the conventional (4th generation) soft switching PTIGBTs, as shown in Fig.14.

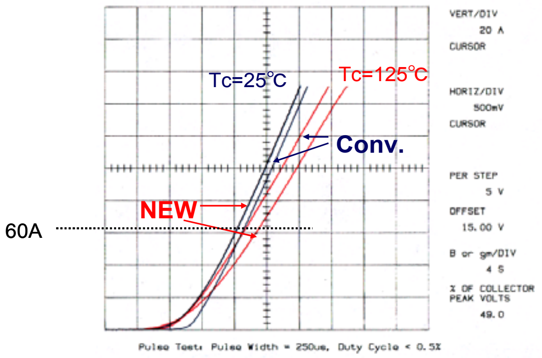

Fig.12 Current voltage curves of new 900V 60A MOSFET-mode IGBTs and conv. PTIGBTs.

It is another remarkable feature that the turn-off loss does not increase significantly even if the applied dV/dt increases as seen in Fig.15. The switching loss improvement becomes larger as the applied dV/dt increases.

We believe that MOSFET-mode operation is quite useful for over 100kHz high frequency soft switching applications, such as power supplies, where high switching capability is the main concern and the sustaining and short circuit capabilities are not required.

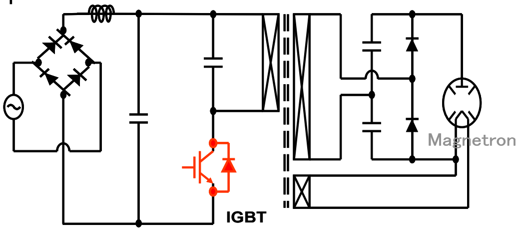

Fig.13 Evaluation circuit

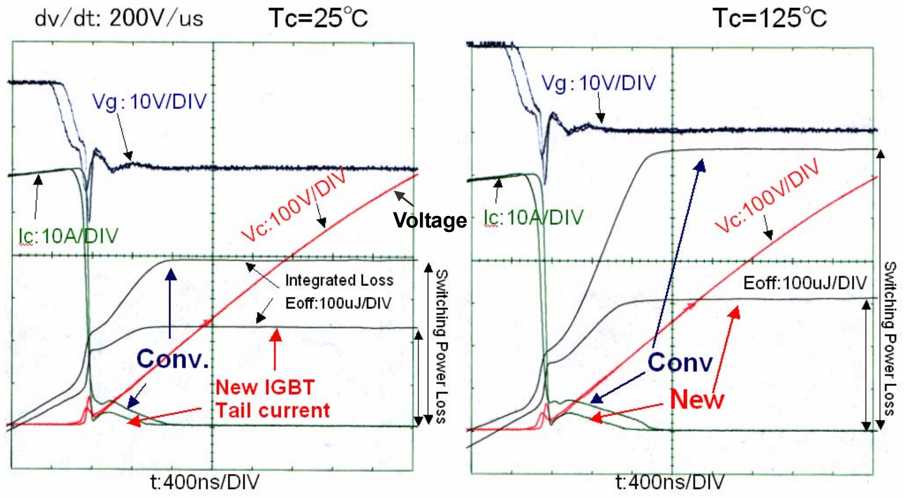

Fig.14 Switching-off waveforms are compared between conv. PTIGBT and new 900V MOSFET-mode thin wafer PTIGBTs. 55% power loss reduction is seen at 125°C temperature. (Voltage:100V/Div, Current:10A/Div)

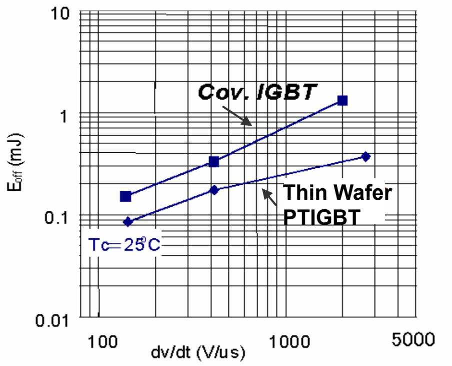

Fig.15 Turn-off loss as a function of applied dV/dt. Difference between conv. IGBTs and New IGBTs becomes larger for higher dV/dt.

References:

[1] T. Matsudai et. al., Proc. of ISPSD'02, p.258

[2] A. Nakagawa et al., IEEE Trans. ED-34, p.351(1987)

[3] M. Yamaguchi et al., Proc. of ISPSD'03, p.349