Ultra Low Cout×Ron Photo-relay using Depleted Drift Layer in Thin Film SOI

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Abstract

In this paper, we propose a new concept of a MOSFET switch for small-outline photo-relays. By applying the concept of depleted drift layer to the thin film SOI MOSFET, the developed photo-relay switch has achieved the lowest Cout×Ron (product of output capacitance and on-state resistance) of 1.87 pFΩ for 26.5V device and 4 pFΩ for 43V device, respectively. These values are the lowest ever reported. The packaged photo-relays achieved low off-state leakage current and low output pin capacitance, being sufficient to be used 2-3 MHz frequency range measuring instrument.

I. INTRODUCTION

The ATE (Auto Test Equipment) is indispensable to screening defect ICs and LSIs in mass-production. In one set of the ATE, 10,000 numbers of the relays are used for the probing interface of those equipments. The relay is the key device of the ATE. The characteristics that required for the relay used by such probing interface are small size and long lifetime. It is also required that it does not cause chattering noises. The photo-MOSFET switches (a photo-relay, see Fig. 3) have excellent characteristics for this kind of application, thus is replacing the conventional mechanical-relays. As the operation frequency of LSIs is steadily increasing, RF signal transmission characteristics of the photo-relay is increasingly important to examine LSI characteristics. The figure of merit, FOM, for higher frequency transmission characteristics of the photo-relays is expressed by Cout×Ron, where Cout is summation of source-drain (Csd) and gate-drain capacitance (Cgd), and Ron is on-state resistance of the photo-relay. The best FOM of currently available commercial products is 10 pFΩ (Vdss=40 V type). Less than 5pFΩ is desired for 2~5GHz testing ATE application. In this paper, we propose a new concept of a MOSFET switch that used in the small outline photo-relay.

II. ULTRA LOW $C_{OUT}\times R_{ON}$ MOSFET DESIGN

The proposed MOSFET designs are shown in Fig.1. The drift layer of the MOSFET in the thin film SOI is designed to be depleted when the gate and the drain voltage are zero. There are two method for the depletion the drift layer. One is to lowering the impurity concentration of the drift layer; the other is the super junction structure with a fine p-n pattern.

In the case of super junction structure, a very fine lateral super junction structure is formed between the gate and the drain. The big difference from the conventional super junction is that the n and p stripe layers are sufficiently narrow so that they are depleted by the built-in potential even when the drain bias is zero. This dramatically reduces drain-source (Csd1) and drain-gate (Cgd) capacitances. The stripe pattern width (W) and impurity concentration of the super junction (Np, Nn) are determined by the equation (1).

$$W < \{2\varepsilon_s \cdot Vbi \cdot (Np+Nn)/(qNpNn)\}^{0.5} \qquad (1)$$

where ε_s is silicon dielectric constant, Vbi is built-in potential of the super junction.

When the gate is positively biased (on state), the inversion layer is induced in the depleted super junction structure (or the depleted p- drift layer) that indicated by Loff in Fig.1. Consequently, the low on-resistance is realized. The resistance in the drift layer becomes significantly low if a positive gate bias is applied. The buried oxide layer is chosen to be thick enough to reduce the drain substrate (source) capacitance (Csd1)[4]. For example, 3μm-thick buried oxide layer is chosen for the experiment. The gate oxide thickness and the drift layer length between the gate to the drain layer were designed to obtain the blocking voltage (Vdss) of 20V and 40V.

The output capacitance (Cout) comes from the summation of the drain-source capacitance (Csd1), the drain-substrate capacitance (Csd2), the drain-gate capacitance (Cgd) and the package capacitance (Cpackage (~0.1pF)).

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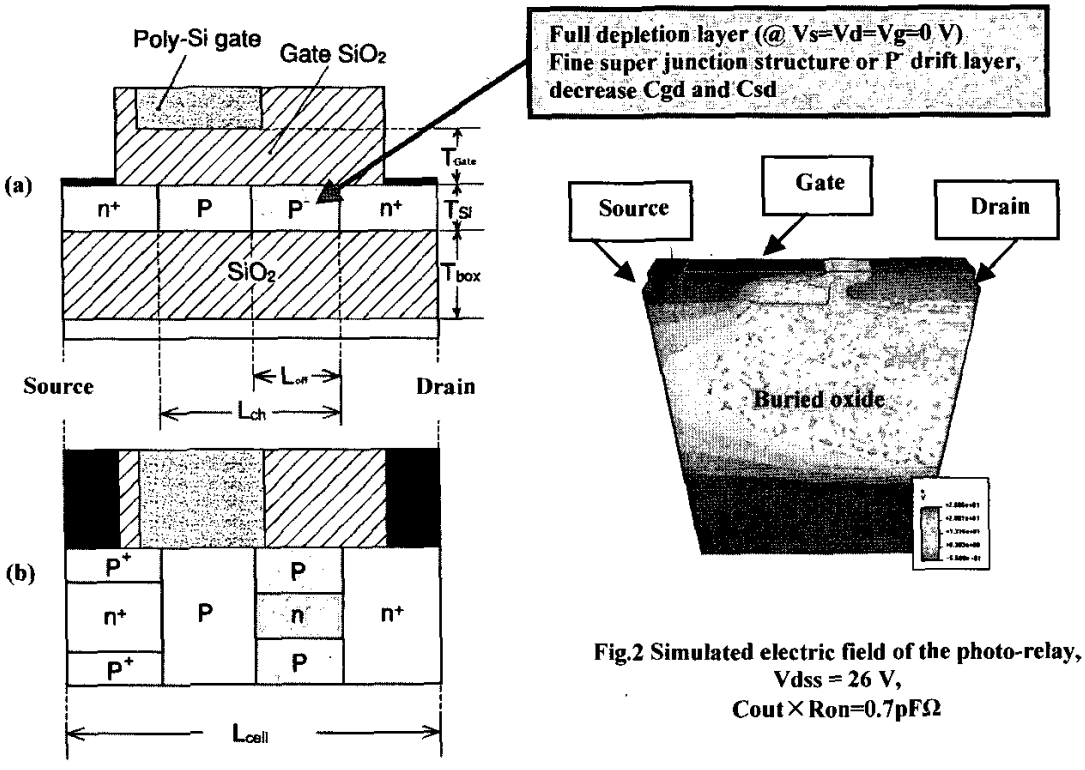

Fig.1 Cross sectional view of photo-relay; (a), pattern; (b)

$$Cout = Csd1 + Csd2 + Cgd + Cpackage \quad (2)$$

The characteristics of the MOSFETs were studied by using 3-D device simulator. The electric field of the MOSFET in the blocking state is shown in Fig.2. The device structural parameters are shown in Table 1. The best FOM is 0.7 pFΩ by the simulation with vdss of 23V.

Top silicon layer (Tsi)	0.1
Buried oxide (Tbox)	3.0
Gate oxide (Tgate)	0.14~0.21
Channel length (Lch-Loff)	1.1~1.3
Offset length P- (Loff)	0.6~2.5

Table 1 Main structural parameters (μm)

Fig.2 Simulated electric field of the photo-relay, Vdss = 26 V, Cout×Ron=0.7pFΩ

III. DEVICE FABRICATION

The proposed concept was experimentally verified by actually fabricating the devices. The fabricated photo-relay consists of a GaAs infrared-emitting diode, photocells and the MOSFET switches, which are housed in a 4-pin package (SOP). Figures 3-(a)(b) and (c) show a photo of the photo-relay SOP package, the photo-relay circuit, and a photo of the fabricated MOSFET switches. The chip size is 0.8mm×0.8mm, and the two MOSFET switches are connected in sires in a chip.

The cross sectional view of the MOSFET switch by SEM micrograph is shown in Fig.4. In the figure, the thickness of SOI and buried oxide is 0.1μm and 3μm. The thickness of the gate oxide is 0.21μm. The offset length between the gate to drain n+ layer is 0.6μm. Cout×Ron of the devices with Vdss of 26.5 V is 1.87 pFΩ and that of the devices of 43 V Vdss is 4 pFΩ. These values are the lowest ones ever reported. Figure 5 shows off-state leakage current of the MOSFET switch. The leakage current was less than 1pA at the rated drain voltage. This value is remarkably small comparing with the conventional MOSFETs for the photo-relay. The detailed experimental results are summarized in the table 2.

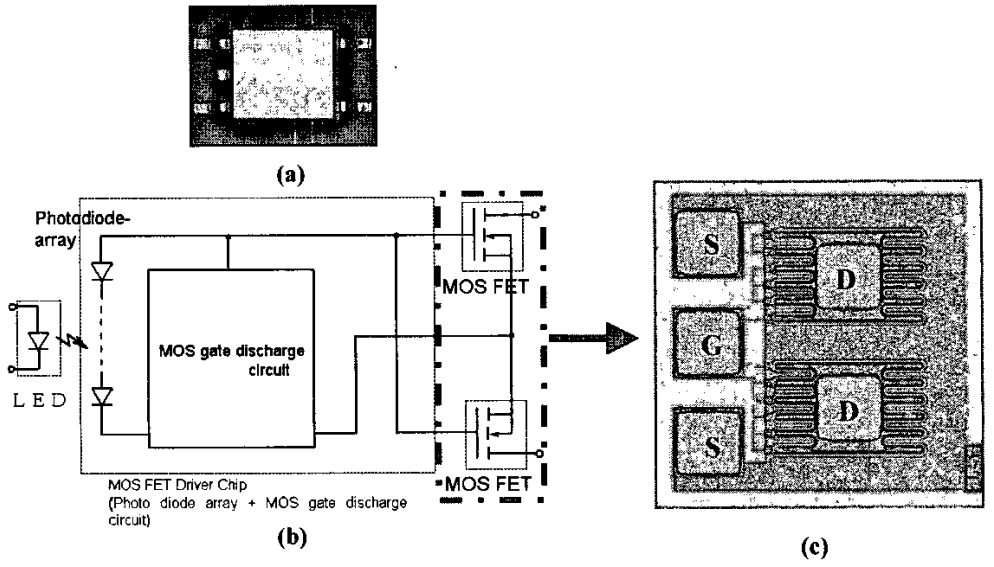

Fig. 3 (a) Photo of photo-relay SOP package, (b) Typical photo-relay circuit, (c) Photo of fabricated photo-relay chip (two MOSFETs are series connected)

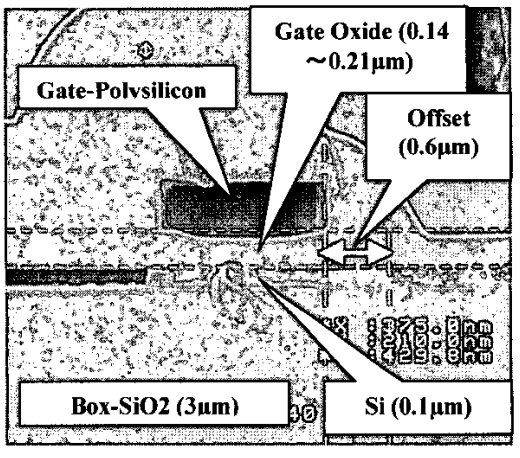

Fig.4 SEM Micrograph of the fabricated photo-relay

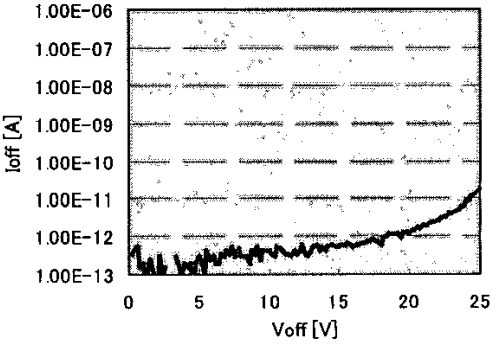

Fig.5 Leakage current flowing between the MOSFET's output pins in the OFF-state (Ioff ; pA)

SPL	Voff(V)	Ron(Ω) @Ion=100mA		Coff(pF)	Ioff(pA)		C×R(pFΩ)
	@Ioff=10nA	@Vg=30V	@Vg=60V		@Vds=20V	@Vds=40V	@Vg=60V
A(p-)	26.0	3.71	2.32	0.87	3.85	-	2.02
B(SJ)	26.5	3.65	2.28	0.82	3.75	-	1.87
C(p-)	43.0	7.50	5.04	0.81	-	6.20	4.08

Table 2 Experimental Results

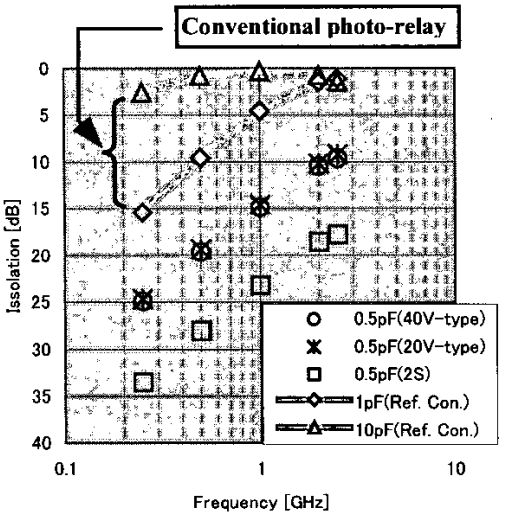

Fig.6 Isolation

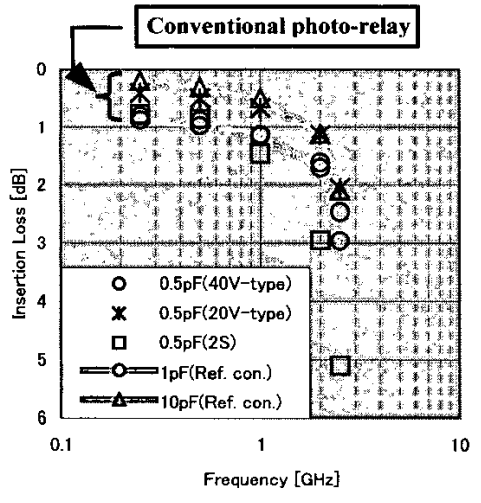

Fig.7 Insertion loss

In the table 2, the sample A and the sample C mean the MOSFET with the depleted p- type drift layer, the sample B means the MOSFET with the depleted super junction structure. A characteristic of a conventional small-output photo-relay is shown in the same table for the reference. [1]

The high-frequency characteristics of the photo-relays are measured by assembling in SOP package. The measured isolation characteristics of the photo-relays are shown in Fig.6. The isolation is 10dB at the signal frequency of 2.5GHz. The measured insertion losses of the photo-relays are shown in Fig.7. The insertion losses are 1dB at the signal frequency of 2GHz.

IV. CONCLUTION

We proposed a new design of the low Cout×Ron MOSFET switch using depleted drift layer in thin film SOI. The design was confirmed by device simulation and device fabrication.

The fabricated photo-relay with the MOSFET switches have the values of Cout×Ron of 1.87 pFΩ with Vdss of 26.5 V, and that of 4 pFΩ with Vdss of 43 V. These values are the lowest ones ever reported. The proposed concept is a promising candidate for future small-outline photo-relay.

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