30V New Fine Trench MOSFET with Ultra Low On-Resistance

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Abstract: **The present paper proposes a new ultra low on-resistance trench MOSFET. The proposed device is characterized by the narrow high resistance n-epi layer between the two trench gates and the thin n-drift layer, which lies between the trench bottom and the n+ substrate. The high resistance n-epi between the trenches is always depleted because of the built-in potential of the p+ gate poly, resulting in the normally-off characteristics without p-base. The thin n-drift layer enables the use of thin gate oxide. The optimum doping concentration and thickness of the n-drift is chosen so that the on-resistance is minimized.**

The proposed trench MOSFET experimentally achieved a 33(V) drain-source blocking voltage and a 10mΩmm^2 specific on-resistance at Vgs=10V. This is the lowest Ron value ever reported.

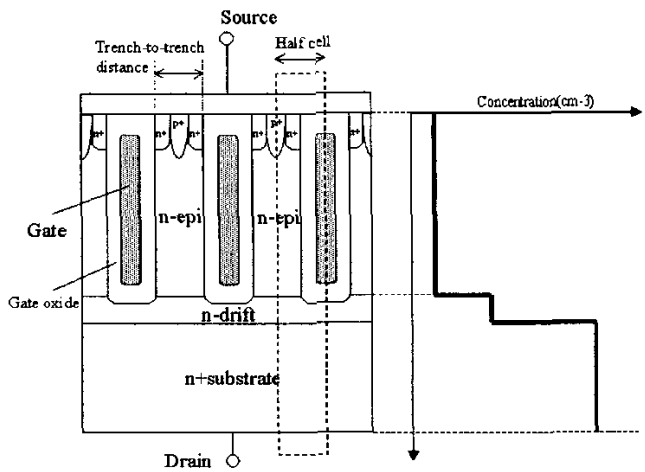

Fig.1 Cross section of the proposed fine trench MOSFET structure and impurity profile

I. Introduction

Many studies of the low on-resistance power MOSFETs have been presented. Especially, trench gate structures are the mainstream in low voltage class MOSFETs[1-2]. Reference [3] proposed an ultra low on-resistance trench MOSFET, which is characterized by deep trench gates penetrating the high resistance n-epi to reach the heavily doped n+ substrate. This trench MOSFET does not employ a p-base region. Low on-resistance is realized by an accumulation layer induced on the sidewall of the trench gate. However, it has a problem that all the drain voltage is applied across the gate oxide and the breakdown voltage was degraded by a high peak electric field induced around the n+ substrate/n-epi junction.

In this paper, we propose a new ultra low on-resistance trench MOSFET with a thin n-drift layer, which lies between the trench bottom and the n+ substrate in order to solve these problems.

II. Device Design and Simulation

The proposed ultra low on-resistance trench MOSFET is illustrated in Fig.1. The difference from Ref. [3] is that the trench gates do not reach the n+ substrate. Instead, an intermediately doped thin n-drift layer lies between the trench bottom and the substrate. The n-epi is always depleted because of the built-in potential of the gate poly. As a result, this fine trench MOSFET shows normally-off characteristics without p-base.

We carried out 2-D numerical simulation. Figures 2 and 3 show the dependence of the leakage current on the trench-to-trench distance and the impurity concentration of the n-epi, respectively. These figures indicate that less than 0.4um of trench-to-trench distance and less than 1e15cm^{-3} of the impurity concentration of the n-epi are required for normally-off operation. In order to relax the electric field at the bottom of trenches, the gate oxide thickness was chosen to be 100nm.

For example, our typical calculated structure was

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that the trench width and the trench-to-trench distance were both 0.4um, and that the impurity concentrations of the n-epi and the n-drift layer was 2e14cm^{-3} and 2.5e16cm^{-3}, respectively.

A positive gate voltage induces a low resistance accumulation layer on the trench sidewall. The drain current flows from the n-drift layer into the accumulation layer. A 8.9mΩmm^2 on-resistance at Vgs=10V and more than 35V source-drain blocking voltage (Vdss) were obtained by the 2-D numerical simulation, using an uniform gate oxide of 100nm and the n-drift layer thickness of 0.5um. It was found that 0.5um thick n-drift is sufficient to greatly reduce the electric field applied across the gate oxide film.

Figure.4 shows electron density distribution and equipotential contours at Vds=36V, Vgs=0V.In the figure, the white area indicates the depletion region.

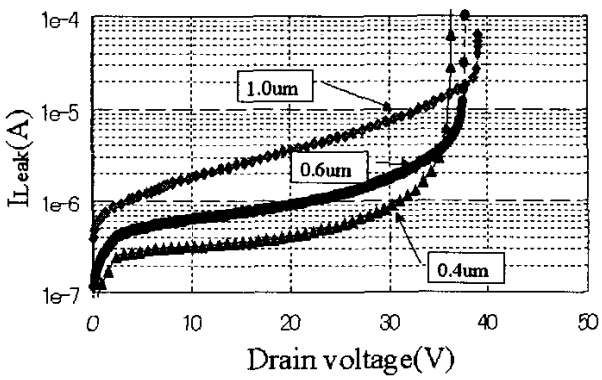

Fig.2 Leakage current vs. drain voltage with trench-to-trench distance as parameter (2-D simulation)

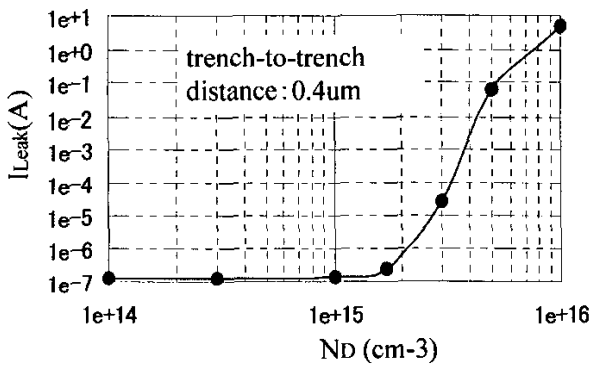

Fig.3 Leakage current vs. n-epi impurity concentration (2-D simulation)

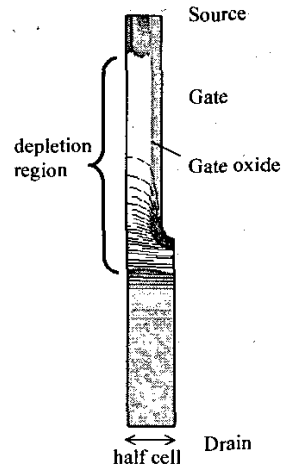

Fig.4 Electron density distribution and equipotential contours at Vds=36V,Vgs=0V by the 2-D simulation

III. Results and Discussion

Figure 5 shows the actually fabricated impurity profile of the epi-wafer. Since an abrupt change in the impurity profile was difficult to realize, the impurity concentration decayed gradually from the n-drift into the n-epi layer. There was a rather high impurity density portion in the n-epi, where trenches were to be fabricated. This would cause a large leakage current from Fig.3. Thus, in actual fabrication, we decided to execute very light implantation of boron to ensure complete normally-off operation. The boron dose was one order of magnitude lower than the conventional p-base as shown in Fig.6. The Active-Area was 1mm^2.

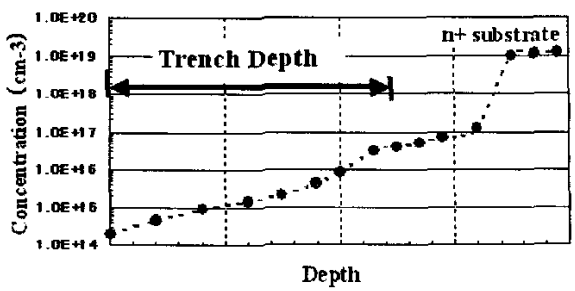

Fig.5 The impurity concentration profile of the wafer used for the experiment

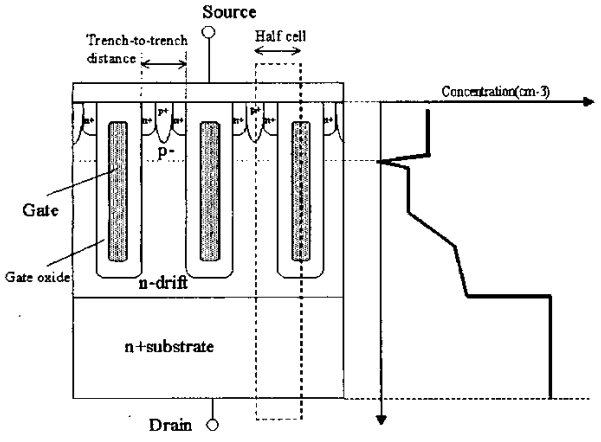

Fig.6 Cross section of experimentally fabricated fine trench MOSFET structure

Figure.7 shows the cross section of the fabricated trench MOSFET by the SEM observation. The fabricated device has a 0.4um of trench width and a 0.4um of trench-to-trench distance.

Figure.8 shows the measured static blocking voltage characteristics of the proposed trench MOSFET. The Vdss value is 33V. The measured Vdss value was lower than the predicted value by the 2-D simulation. We experimentally found that it was caused by the imperfect formation of the p+ region in the surface. Figure.9 shows the measured output characteristics of the proposed trench MOSFET. The numerically predicted values and the experimental results are compared in Table1. The proposed device exhibited a specific on-resistance of 10mΩmm^2 at the gate voltage of 10V.

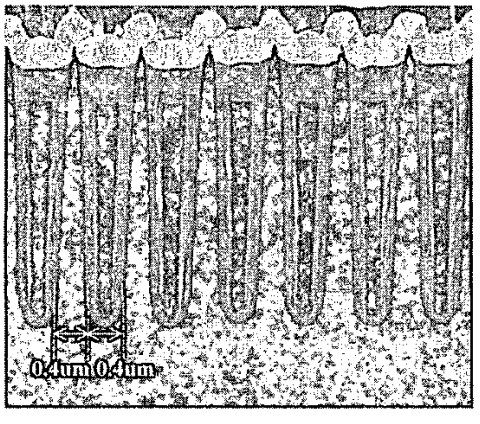

Fig.7 SEM photograph of cross sectional view

It was found that a large portion of the on-resistance comes from the resistance of the substrate wafer. If the thickness of the N+ substrate (0.03-Ωcm) is reduced to 50um, the on-resistance is expected to be 5.9mΩmm^2.

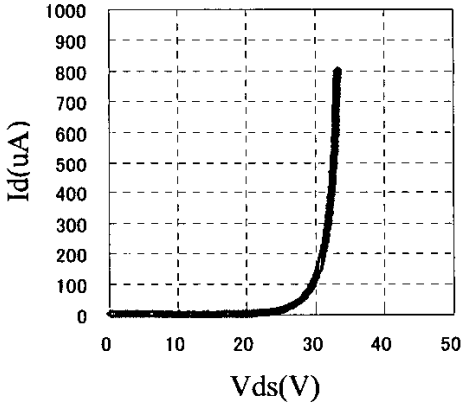

Fig.8 Measured static blocking voltage characteristics of the proposed trench MOSFET

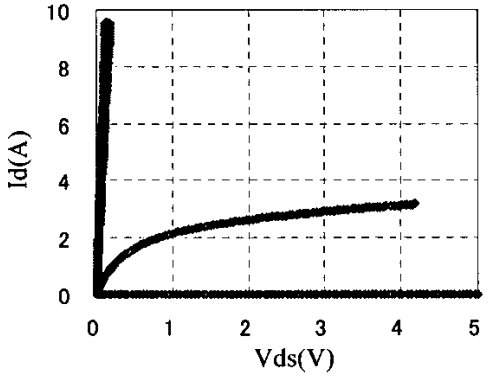

Fig.9 Measured output characteristics of the proposed trench MOSFET

Table 1

	Simulated	*Measured*
Blocking Voltage	36V	33V
Threshold Voltage	1.22V	0.36V
Ron(Vgs=10V)	8.9mΩmm^2	10.0mΩmm^2

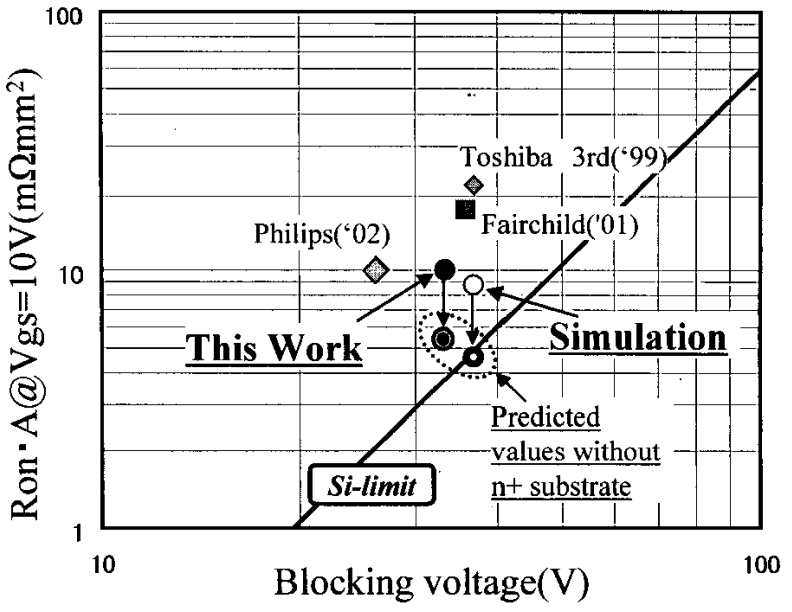

Fig.10 Comparison of state of art On-resistance vs. Blocking voltage. Black dot shows the present experimental result. Simulation shows the calculated on-resistance of the fabricated device. Circles (●,●) show the predicted on-resistances if n+ substrate is eliminated.

IV. Conclusion

An experimental data of the on-resistance vs. the blocking voltage for the proposed trench MOSFET and the conventional power MOSFETs are compared in Fig.10 [1-2,4]. The proposed trench MOSFET utilizing the accumulation effect achieved a low specific on-resistance $10m\Omega mm^2$ with 33V blocking voltage. This is the lowest Ron value ever reported. This figure also shows the predicted on-resistance (double circles) of the proposed device if n+ substrate is completely eliminated. It was found that a large part of the on-resistance is now attributed to the substrate resistance value of $4.6m\Omega mm^2$ (the resistivity of 0.03-Ωcm) and an improvement is no longer expected from the device structural optimization.

V. Acknowledgements

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