Low Gate Charge 30 V N-channel LDMOS for DC-DC Converters

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Abstract. We have developed low on-resistance and low feedback gate charge 30 V n-channel LDMOS for MHz switching DC-DC converter applications. The feature of the device is that it has achieved a high avalanche capability of more than 20 amperes together with Ron·Qgd value of 10 mΩnC, which is the lowest, ever reported for 30 V devices. A low gate resistance of 0.4 Ω was achieved by two layer metal electrodes. These features are desirable for MHz switching frequency DC-DC converters to obtain higher efficiency. Good avalanche capability of 20 amperes is achieved under unclamped inductive switching (UIS) condition.

INTRODUCTION

Next generation microprocessors will demand 1 V 100 A DC-DC power supplies. Higher power conversion efficiency at higher operating frequency is also required. Usually synchronous rectification is used to meet such requirement.

It is extremely important to reduce power loss of the MOSFETs used in synchronous buck converters. Particularly, control FETs are required to reduce both their conduction loss and switching loss.

Reducing the on-resistance (Ron) is necessary to reduce conduction loss. Reducing the gate drain feedback charge (Qgd) is effective to achieve high switching speed for the purpose of reducing switching loss[1]. To estimate the total loss of the control FET, the product of Ron and Qgd is conventionally used as the figure of merit (FOM). Reducing the gate resistance (Rg) is also an effective method to reduce switching loss because modern drivers for MOSFETs have low output resistance.

We have developed a new LDMOS with improved FOM for the control FET of DC-DC converter application. This device achieves not only low Ron·Qgd but also low gate resistance. Further more good avalanche capability is performed under UIS condition.

DEVICE STRUCTURE AND CHARACTERISTICS

The basic device structure is the same as conventional LDMOS, as shown in Fig. 1. The LDMOS is fabricated on a p-type epitaxial layer on a p+ substrate. Source regions are connected to the substrate by p+ sinker diffusion. Using two metal layers is a great help to achieve low gate resistance.

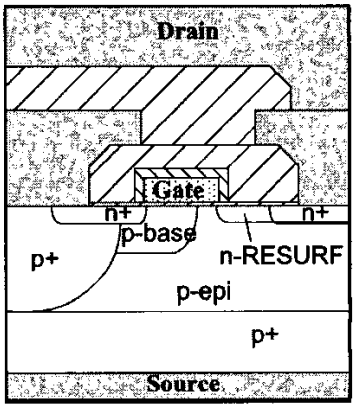

Figure 1. Cross-sectional view of the basic structure for the developed LDMOS

Figure 2 shows the photo of the fabricated chip. The active FET area is about 5.9 mm^2. The design optimizations of source, p-base, poly-silicon gate and the n-RESURF (off-set channel) structures are the key issue to reduce Ron·Qgd while keeping the high avalanche capability.

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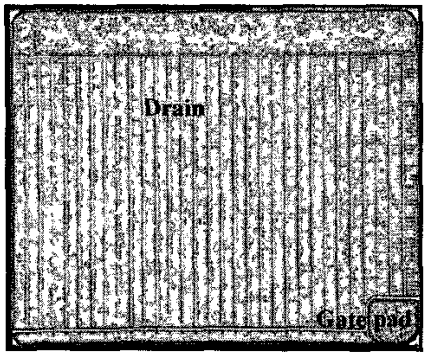


Figure 2. Chip photograph of a fabricated LDMOS

It is important to reduce the sheet resistance of the p-base region to suppress the action of the parasitic bipolar transistor and improve avalanche capability. The p+ sinker region was laterally diffused underneath the n+ source region. A high dose p-base region is also effective to increase avalanche capability (see Fig. 3). However, excessively higher dose of the p-base results in a higher gate threshold voltage, and accordingly degrades Ron·Qgd.

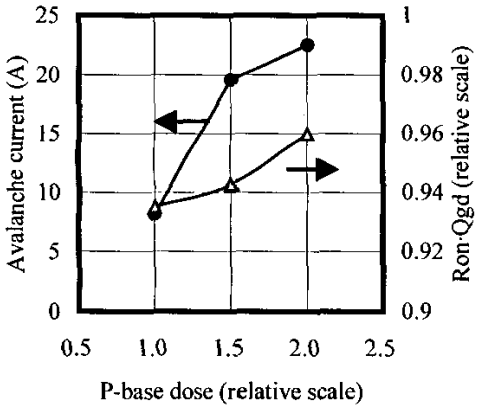


Figure 3. Influence of dose for the p-base region on avalanche current and R_{on}·Q_{gd}

Reducing the thickness of the gate oxide improves Ron·Qgd. However, excessively thinner gate oxide results in poor gate reliability. The thickness of the gate oxide layer was determined so that the high temperature bias reliability test for the gate voltage of 12.5 V was achieved.

The gate length has a great influence on both avalanche capability and Ron·Qgd. Figure 4 shows the relationship between the gate length and Ron·Qgd. The gate length is one of the key parameters for improving Ron·Qgd.

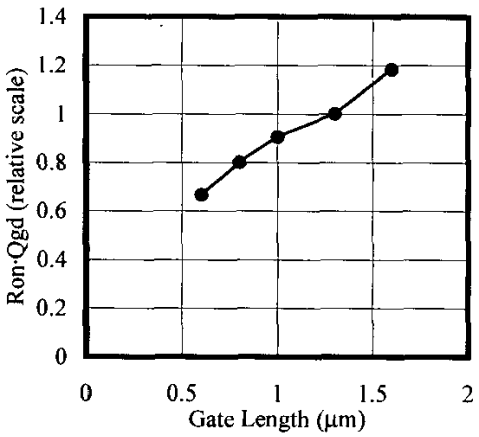


Figure 4. Influence of the gate length on R_{on}·Q_{gd}

However, shorter gate length degrades avalanche capability as seen in Fig. 5. We have successfully improved avalanche capability by optimizing the source, base and gate structures from the structures A, B to the final structure C. The source and p-base impurity dose and the thickness of the silicon dioxide layer around the poly-silicon gate electrode have been optimized so as to reduce the gain of the parasitic npn bipolar transistor, from the structure A, B to C.

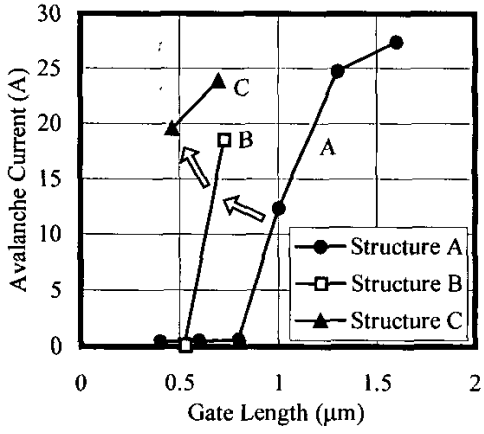
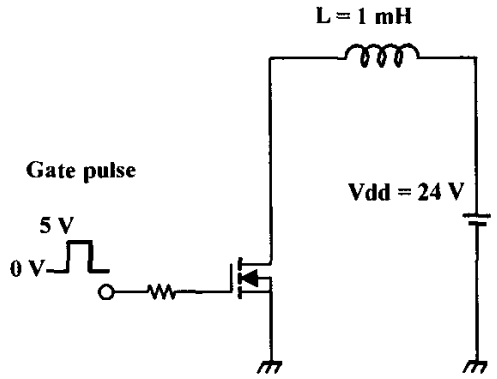
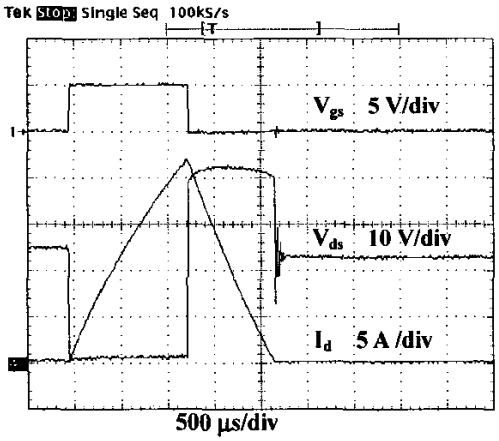


Figure 5. Influence of the gate length on avalanche current. Avalanche capability was improved by changing the structure from A, B, to C



(a) UIS condition for measurement of avalanche capability



(b) Measured turn-off waveforms for LDMOS with optimized structure

Figure 6. Measured 20 ampere turn-off waveforms under UIS condition

Figure 6 demonstrates unclamped inductive switching waveforms of 20 amperes.

Good avalanche capability was not able to be achieved for less than 0.45 µm gate length under the present our lithography rule. Thus, we have grown a thick silicon dioxide film around the poly-silicon gate, as seen in Fig. 7, in order to reduce the overlap between the gate and the self-aligned n-RESURF layer. This reduces the feedback capacitance.

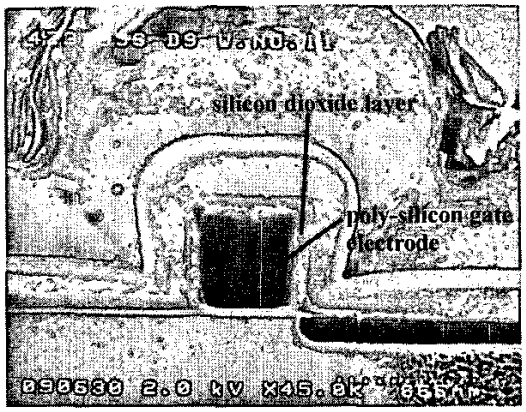


Figure 7. Cross section of the poly-silicon gate electrode

Active FET area	5.9 mm^2
Breakdown voltage	35 V
Gate Threshold voltage	1.5 V
Maximum gate voltage	12.5 V
Ron (Vgs=4.5V, Id=7.5A)	14.7 mΩ
Ron (Vgs=7V, Id=7.5A)	12.2 mΩ
Qgd (Vds=11V)	0.82 nC
Ron·Qgd	10.0 mΩnC
Gate resistance	0.4 Ω
Avalanche current (L=1mH, Vdd=24V)	20 A

R_{on} : on-resistance
Q_{gd} : gate-drain feedback charge

Table 1: Typical electric characteristics of the developed LDMOS

Typical electrical characteristics of the developed LDMOS are listed in Table 1.

Figure 8 shows a typical gate charge waveform. Measured Qgd depended significantly on the applied drain-source voltage (Vds) as shown in Figure 9. The same measurement condition as Ref.[2] was adopted for the value of Qgd, applying the drain-source voltage of 11 V. The measured Qgd is 0.82 nC for the drain-source voltage of 11 V. Ron without the package is 14.7 mΩ for the gate voltage of 4.5 V. Ron is reduced to 12.2 mΩ if the gate voltage of 7 V is used. The higher gate drive voltage of 7 V will be used in the next generation VRM[3]. Consequently, the Ron·Qgd value is 10 mΩnC, which is 25 % lower than the previously reported value[2] [4].

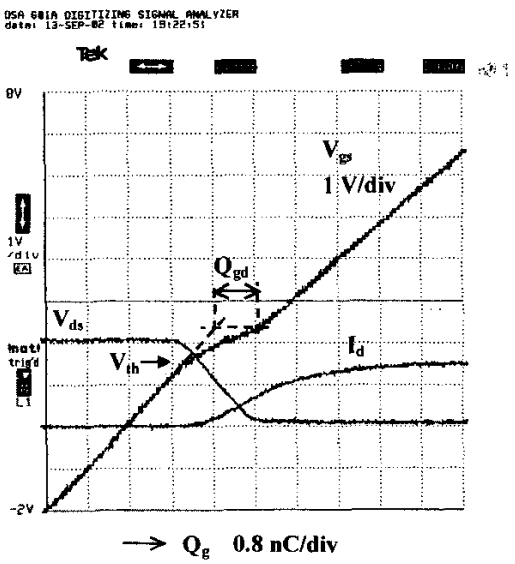


Figure 8. Measured typical gate charge waveform

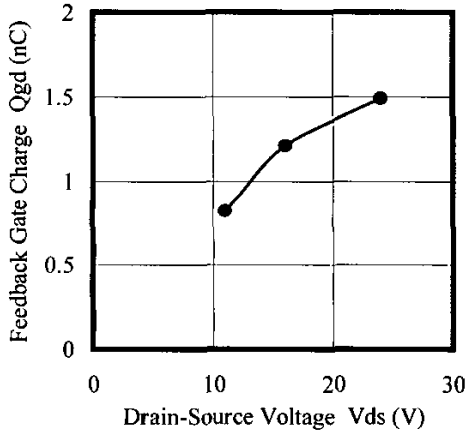


Figure 9. Influence of applied drain-source voltage on Q_{gd}

CONCLUSIONS

We have developed a new 30 V n-channel LDMOS, which has low on-resistance and low feedback gate charge. The figure of merit Ron·Qgd is 10 mΩnC. This device has also a low gate resistance of 0.4 Ω and achieved a high avalanche capability of more than 20 amps. These features are desirable for MHz switching frequency DC-DC converters to obtain higher efficiency.

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