New Anode Design Concept of 600V Thin Wafer PT-IGBT with Very Low Dose P-buffer and Transparent P-emitter

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ABSTRACT

We propose 600V new thin wafer PT (Punch Through) IGBT having a new concept of anode design. This proposed PT-IGBT has a very low dose p-type layer, called "p-buffer", between a transparent p-emitter (anode) and an n-buffer layer. This provide a practical design for easy fabrication without deteriorating the good feature of the thin wafer PT-IGBTs. The n-buffer dose and the p-emitter dose can be precisely controlled by the doses of the two ion implantations. This is a great merit in precise control of the p-emitter injection efficiency. An oscillation in the turn-off waveforms also disappears for the proposed PT-IGBT with p-buffer layer, because a smooth turn-off is achieved by a small tail current. The total power loss is not affected by the small tail loss.

Introduction

The device concept of thin wafer PT-IGBT with a low dose n-buffer and a transparent p-emitter (anode) is one of the main concerns for both the middle voltage IGBT and the high power IGBT. It has been verified that the device exhibits the excellent trade-off relation between the device on-state voltage and the switching speed [1-3]. However, the fabrication process includes many problems. 600V PT-IGBT requires about 60μm thin wafers. The process of thinning the wafer inevitably accompanies some variations in the resultant wafer thickness. The control of the total thickness and how to fabricate the anode side are the main issues for such thin wafer IGBTs. The variation in the total wafer thickness may cause the variation in the drift region thickness or in the n-buffer layer thickness. The change in the drift region thickness affects the on-state voltage and the turn-off losses. The change in the n-buffer thickness results in the difference in the total dose of the n-buffer and, thus, the p-emitter efficiency is not maintained in the same level.

In this paper, we propose a new anode design concept called lightly doped "p-buffer". The proposed thin wafer PT-IGBT has a low dose p-buffer layer between the transparent p-emitter and the n-buffer layer. The variation in the total thickness of the p-buffer in the fabrication process does not substantially influence the electrical characteristics. Taking advantage of this feature, practical fabrication process of the thin wafer IGBT is proposed. In addition, the turn-off characteristics are improved.

It should be noted that the p-buffer can be

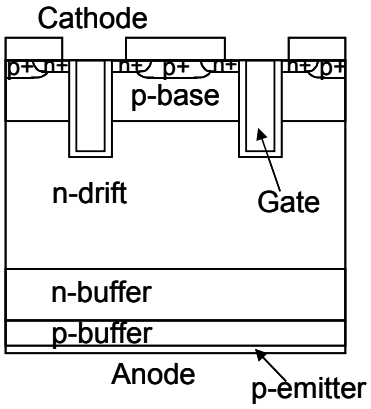


Fig. 1 Cross section of thin wafer PT-IGBT with transparent p-emitter and low dose p-buffer layer

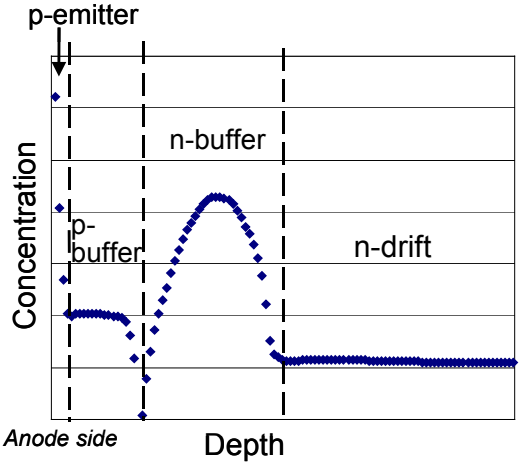


Fig. 2 Measured impurity distribution of cross section of anode region for proposed PT-IGBT, by SRA(Spreading Resistance Analysis) measurement

replaced by a lightly doped n type layer.

Device Structure and Fabrication

Figure 1 shows the schematic cross section of the proposed trench gate PT-IGBTs. This PT-IGBT has a low dose n-buffer layer and a low dose transparent p-emitter. Since the total dose of the p-buffer is small enough, the switching speed is substantially controlled by the dose of the transparent p-emitter. Then, the lifetime control is not necessary. The lifetime in the drift layer is kept high and the carrier densities in the drift layer were much higher than those of the conventional PT-IGBT. The design of the cathode side is almost the same as the conventional PT-IGBTs.

Figure 2 shows the measured impurity distribution of the anode region, by SRA (Spreading Resistance Analysis) measurement. The total dose of the p-buffer layer is extremely low in comparison with that of the transparent p-emitter. The p-buffer dose does not affect the total dose of the p-emitter. Thus, the emitter efficiency is substantially determined by the ratio of the dose of the n-buffer and the dose of the transparent p-emitter. It is expected that the thickness of the p-buffer doesn't affect the electrical characteristics. Furthermore, it is found that this p-buffer can replace by a lightly doped n type layer. In this case, the dose of a lightly doped n type layer does not affect the total dose of the p-emitter.

In Fig. 3, the fabrication process of the backside is outlined. First, we prepare the low concentration p-type raw wafer. The arsenic implantation for the n-buffer is carried out and annealed. A high resistivity n-type epitaxial layer is subsequently grown. This p-type raw wafer becomes the p-buffer layer and the implantation region becomes the n-buffer layer. The backside of p-type raw wafer is then removed by grinding so that a thin p-buffer layer remains. Finally, we fabricate the transparent p-emitter using the boron implantation and annealing. The n-buffer dose and the p-emitter dose can be precisely controlled by the dose of ion implantations. Thus, this method has a great merit in precise control of the p-emitter injection efficiency, which greatly affects the

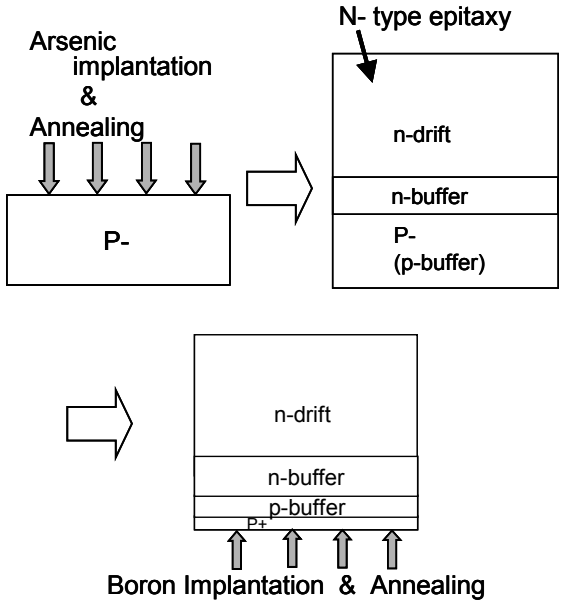


Fig. 3 Process steps of backside for proposed thin wafer PT-IGBT with low dose p-buffer layer

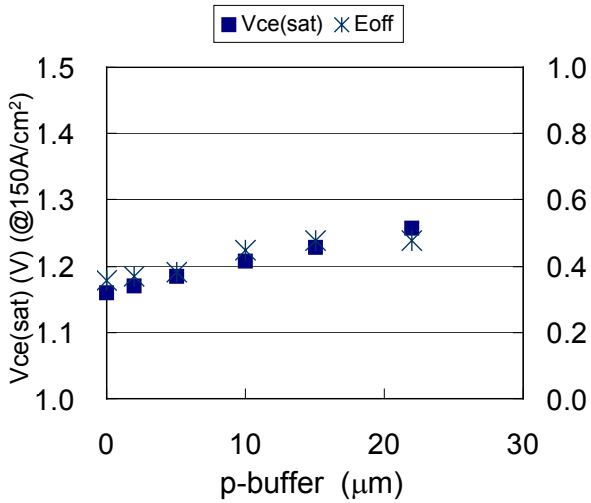


Fig. 4 Simulated on-state voltage drops(Vce(sat)) and turn-off losses(Eoff).
When thickness of p-buffer layer is practically changed, electrical characteristics is almost same.

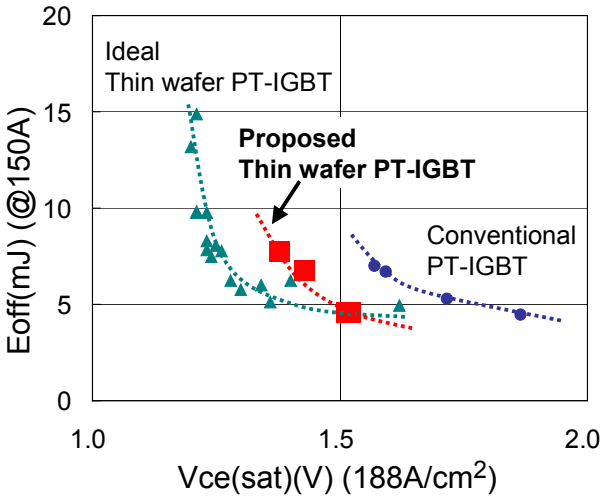


Fig. 5 Measured trade-off relations between on-state voltages and turn-off losses. Good trade-off relation was obtained for proposed PT-IGBT.

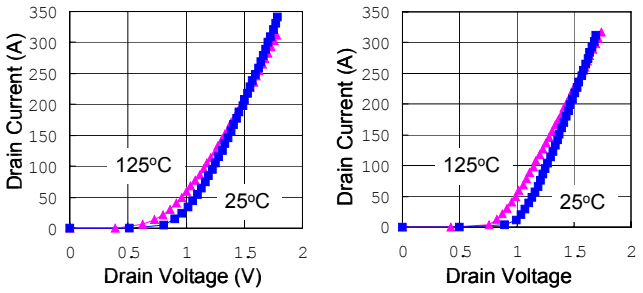


Fig. 6 Measured drain current-voltage curves for thin wafer PT-IGBTs
(a) Ideal thin wafer PT-IGBT
(b) Proposed thin wafer PT-IGBT with p-buffer

IGBT electrical characteristics.

Experimental Results and Device Simulations

In Fig. 4, we estimated the influence of the practical change of the p-buffer layer thickness upon the electrical characteristics, the on-state voltage and the turn-off losses, using the DESSIS device simulation. Even if the thickness of the p-buffer layer is practically changed, the electrical characteristics are almost same. When the p-buffer thickness changes to 15μm from 5μm, the on-state voltage changes only 0.044V. This value of the change is about 4% against the average on-state voltage. Usually the variation in the p-buffer layer thickness is less than 10μm in the fabrication process.

Figure 5 shows the measured trade-off relation between the on-state voltage and the turn-off losses at the room temperature. For the conventional/ideal thin wafer PT-IGBT and the proposed thin wafer PT-IGBT, we varied the p-emitter injection efficiency to obtain the relation. For the thick wafer conventional PT-IGBT, the lifetime in the drift layer was changed to obtain the trade-off relation.

The good trade-off relation (■) was obtained for the proposed PT-IGBT. The excellent data (▲) was attributed to the conventional/ideal thin wafer PT-IGBTs, reported in ISPSD 2001 [4]. We called this conventional/ideal PT-IGBT "ideal PT-IGBT" in this paper. The referenced ideal thin wafer PT-IGBT had a slightly thinner n-drift layer, and the breakdown voltage was just 620V. In this study, we redesigned the thickness of the n-drift layer to obtain more than 680V breakdown voltages, and the a little bit thicker n-drift layer was adopted. This is one of the reasons why the electrical characteristics of ISPSD 2001 were better than the proposed IGBTs.

The measured forward current-voltage

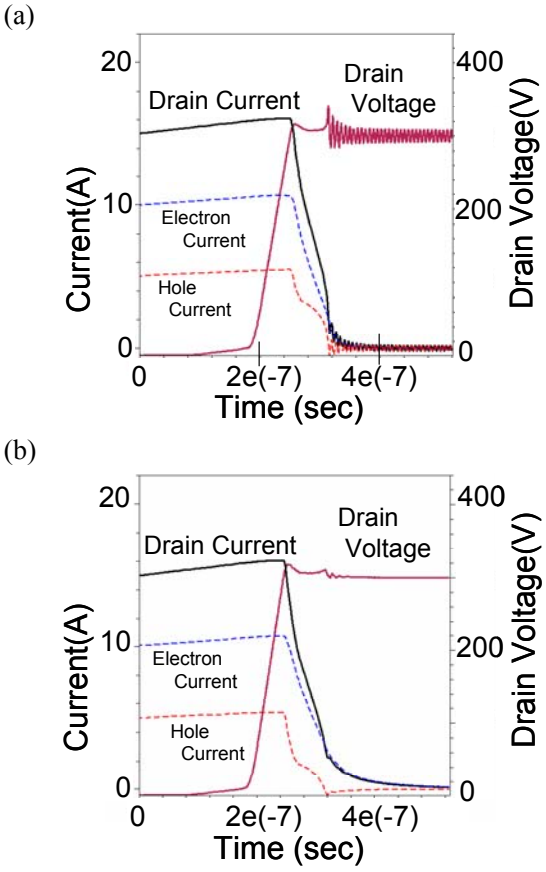


Fig. 7 Simulated turn-off curves for thin wafer PT-IGBT.
(a) Thin wafer PT-IGBT without p-buffer layer
(b) Thin wafer PT-IGBT with 5μm thick p-buffer layer. Oscillations in turn-off curves disappear.

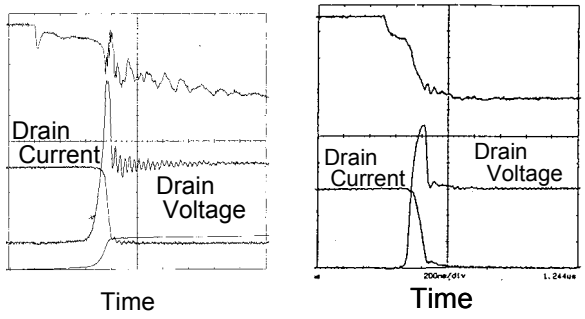
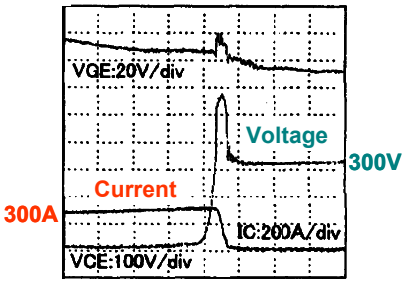


Fig. 8 Measured turn-off curves for thin wafer PT-IGBT.
(a) Ideal thin wafer PT-IGBT
(b) Proposed thin wafer PT-IGBT with p-buffer layer. Oscillations in turn-off curves disappear.

characteristics of the fabricated 600V/150A rated thin wafer PT-IGBTs are shown in Fig. 6, for the room temperature (25°C) and high temperature (125°C). The gate voltage is 15V, respectively. It was obtained the almost same characteristics for both the ideal thin wafer PT-IGBT and the proposed PT-IGBT in spite of having p-buffer

(a)



(b)

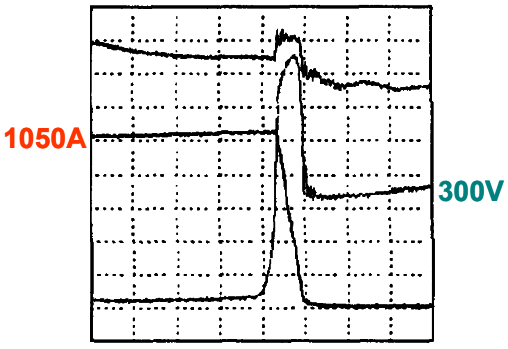


Fig. 9 Measured turn-off curves for proposed PT-IGBT.
Very large current, 1050A, which is seven times rated current, is cut off safely.
Turn-off failure dose not occur.

layer.

Another remarkable feature of the proposed PT-IGBT is that the oscillations in the turn-off waveforms disappear. One of the main challenges for the ideal thin wafer PT-IGBT is to eliminate the oscillation in the turn-off period.

Figure 7(a) shows the simulated turn-off curves for the ideal thin wafer PT-IGBT. The applied voltage is 300V for 150A current turn-off under an inductive load. On the other hands, the proposed PT-IGBT has a very small tail electron current in the same condition due to the stored carriers in the p-buffer layer in Fig. 7(b). The small tail current prevents oscillations effectively. It should be mentioned that the total power loss is not affected by the very small tail loss.

Figure 8 shows the measured turn-off curves for the room temperature. The turn-off loss is 6mJ for the ideal thin wafer PT-IGBT. For the proposed PT-IGBT, the oscillation disappears and the loss is 5.7mJ in Fig.8(b).

We also demonstrated the large current turn-off capability of the proposed devices in Fig.9. It is found that the proposed 600V 150A IGBT has a very large current turn-off capability. The very large current of 1050A, which is seven times rated current, was turned off safely in Fig.9(b). The short circuit withstand capability is also confirmed.

Conclusion

We have proposed and fabricated the 600V new thin wafer PT-IGBT having a new concept of the anode design. The proposed PT-IGBT has a very low dose p-type (or n-type) layer between a transparent p-emitter and an n-buffer layer.

The proposed thin wafer PT-IGBT provides a practical design for easy fabrication without deteriorating the good feature of the thin wafer IGBTs. The total dose of the p-buffer layer is extremely low in comparison with that of the transparent p-emitter. The p-buffer dose does not affect the total dose of the p-emitter. Then the proposed PT-IGBT maintains the excellent trade-off relation between the on-state voltage and the turn-off losses in spite of the variation in the p-buffer layer thickness.

The oscillation phenomena in the turn-off waveforms can also be eliminated. The small tail current prevents oscillations effectively.

Acknowledgement

The author would like to thank Senior Manager Kouhei Morizuka and Group Manager Tsuneo Ogura for their support and advice during the course of this study.

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