Cost-Effective Approach in LDMOS with Partial 0.35μm Design into Conventional 0.6μm Process

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Abstract. We propose a practical solution, which can provide the same high performance LDMOS as that of the more advanced CMOS design rule with retaining still the low cost of the old technology. More specifically, we have introduced a limited number of 0.35μm equivalent mask alignment steps into 0.6μm based BCD processes. We have successfully developed 0.6μm design based 40V and 50V LDMOS, whose on-resistances are superior to those of 0.35μm based LDMOS. The on-resistance of the developed 40V and 50V LDMOS are 54.3 and 69.7 mΩ mm^2, respectively. These values are superior to the reported values of the 0.35μm design LDMOS.

INTRODUCTION

Smart Power technologies [1,2] have been widely expanding their application fields since LDMOS has a lot of attractive features; low on-resistance, low power dissipation, and high speed switching capability. Especially, the greatest merit of LDMOS is that the specific on-resistance and the performance can be simply improved by scaling its design according to CMOS lithography rule [2,3,4,5,6]. The finer design rule also facilitates the integration of more functions in a single chip[2,3]. However, the advanced CMOS process still requires cost higher.

In view of these situations, we propose a practical solution, which can provide the same high performance LDMOS as that of the more advanced CMOS design rule with retaining still the low cost of the old technology. More specifically, we have introduced a limited number of 0.35μm equivalent mask alignment steps into 0.6μm based BCD processes. Based on the concept, we have successfully developed 0.6μm design based 40V and 50V LDMOS, whose on-resistances are superior to those of 0.35μm based LDMOS. The on-resistance of the developed 40V and 50V LDMOS are 54.3 and 69.7 mΩ mm^2, respectively. These values are superior to the reported values of the 0.35μm design LDMOS [3,4,5].

PROCESS CONCEPT/ DEVICE DESIGN

Concept. Most of the applications of Smart Power do not need to integrate such a large scale of logic circuits that requires the finer design rule of, for example, 0.25μm CMOS. The advanced CMOS process still requires cost higher than the conventional technology. We estimated the relative cost of logic part as a function of logic scale in each design rule generation. The results are shown in Fig.1. It seems that 0.6μm is a practical choice in case of under 10k gates scale. It is true that LDMOS can be improved and can be shrinkable according to CMOS design rule. However, the ratio of reduction in LDMOS area is smaller than that of the logic part. If a chip consists of a small area of logic and a large area of LDMOS, finer design is not needed. Thus, our goal is a practical solution that maximizes LDMOS performance in conventional 0.6μm CMOS fab.

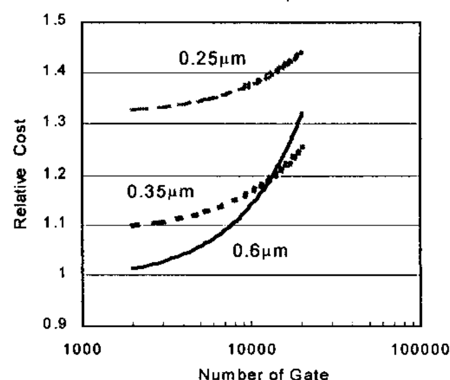

Fig.1 Relative chip cost on logic scale in various design rule

In our LDMOS design, not only minimum dimensions, but also alignment margins are important. Then, we re-designed our LDMOS processes,

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introducing a limited number of 0.35μm mask steps into 0.6μm BCD, so that LDMOS performances could be improved meaningfully as compared to the simple 0.6μm BCD. We examined each mask step adapted to 0.35μm design rule carefully. We finally concluded that the critical steps are only 5 mask alignment steps, which are some ion-implant steps, isolation (field formation) step and gate formation step. This design scheme is shown in Fig.2.

Also the Adaptive Resurf [6,7] techniques were introduced for improving snapback voltage. The process flow of the present work is shown in Fig. 3. The conventional 0.6 μm BCD consists of LDMOS drift layer steps, bipolar steps, polycrystalline-silicon resistor, capacitor steps and the third thick aluminum metal layer, in addition to 0.6 μm original CMOS processes. The process flow modification from the original 0.6μm BCD is minimal and only 5 photo steps modified, especially Step & Repeater.

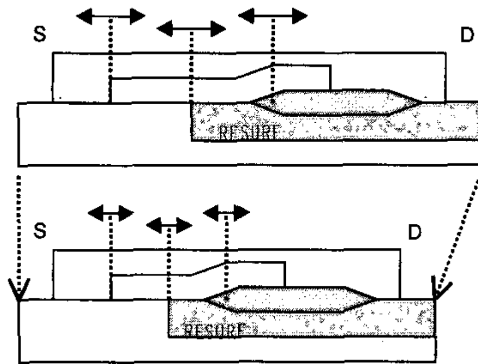

Fig.2 The scheme of LDMOS design by improving mask alignment margins

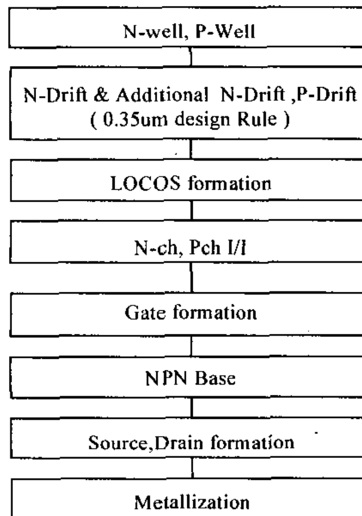

Fig.3 Process Flow in the present work

Design for ESD in LDMOS. Our another aim is to improve the ESD capability of LDMOS. T-CAD analysis of ESD phenomena in LDMOS indicated remarkable temperature rise in silicon lattice in the neighborhood of the drain n+. By introducing sinker n+ diffusion in the drain, such temperature rise could be reduced and the position of temperature rise could be shifted to a deeper region. T-CAD results are shown in Fig.4. The LDMOS with the sinker n+ is shown in Fig.5, compared to the normal LDMOS.

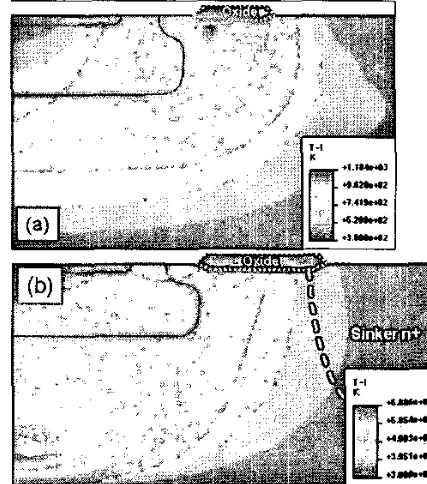

Fig.4 Simulated lattice temperature in ESD Phenomena for (a) the normal LDMOS structure and (b) the LDMOS with sinker n+

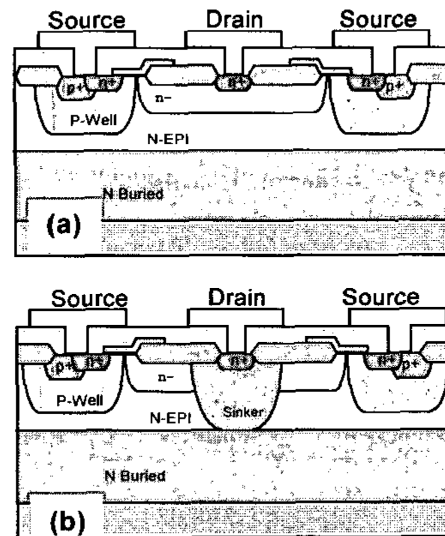

Fig.5 The LDMOS cross-sectional images of (a) a conventional type and (b) a type with sinker n+ in drain

RESULTS

We fabricated 40V LDMOS, 50V LDMOS, and 30V npn/pnp, 5V CMOS, diode, resister and capacitor using the proposed process. The gate oxide is 14nm, the same as 5V CMOS. Each Ion implantations for 40V and 50V LDMOS were optimized independently. Measured characteristics of major devices are summarized in Table 1.

Table1 The summary of measured characteristics of major devices compared with conventional 0.6μm devices

Devices	Items	unit	Conventional 0.6μm Design	This Work 0.6μm with 0.35μm
NPN	hFE		100	120
	BVceo	V	40	37.8
LPNP	hFE		76	79.7
	BVceo	V	38	37.4
CMOS	Lg	μm	0.6	0.6
(NMOS/PMOS)	Vth	V	0.85/-0.85	0.85/-0.85
	BVds(op.)	V	5	5
40V Nch-LDMOS	BVdss	V	48	48.8
	Ron*A	mΩYmm2	115	54.3
50V Nch-LDMOS	BVdss	V	-	58.6
	Ron*A	mΩYmm2	-	69.7
40V Pch-LDMOS	BVdss	V	49	45.8
	Ron*A	mΩYmm2	228	131
# of Metal layers			3	3

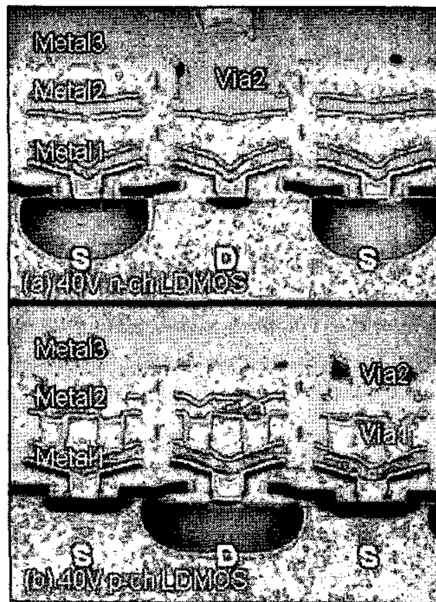

Fig.6 Cross-sectional SEM photographs of 40V LDMOS for (a) n-ch and (b) p-ch

LDMOS. Cross sectional SEM photos of fabricated 40V n-ch and p-ch LDMOSs are shown in Fig.6.

Measured device characteristics are compared with those of conventional 0.6μm BCD, and are shown in Table 1. There is a significant improvement in the on-resistance from conventional 0.6μm BCD. The on-resistance of the developed 40V and 50V n-ch LDMOS are 54.3 and 69.7 mΩmm^2, respectively. These values are superior to the reported values of the 0.35μm design LDMOS [3,4,5]. The comparison of the results with those of the state of the art LDMOS is plotted in Fig.7. It should be noted that we adopted none of the processes which are unique to 0.35μm-generation CMOS, resulting in no special increase in cost. Similarly, the on-resistance of 40V and 50V p-ch LDMOS are 131 and 230 mΩmm^2, respectively.

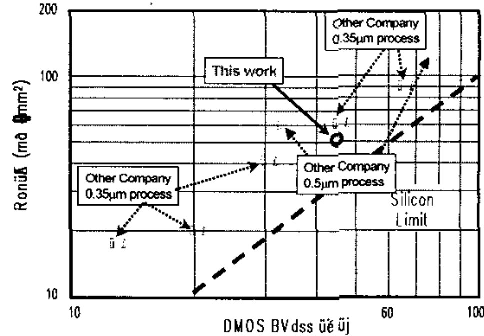

Fig.7 The comparison of the results with those of the state of the art LDMOS in RonA plot

Vd-Id characteristics are shown in Fig.8 and Fig.9, in which we notice that the device achieved the high on-state breakdown voltage similar to the static breakdown voltage.

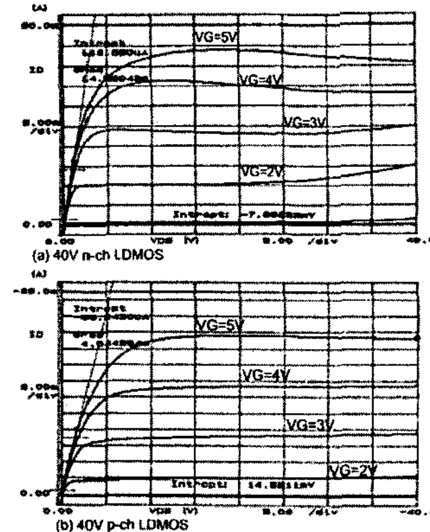

Fig.8 *ID-VD* characteristics of (a) 40V n-ch LDMOS and (b) 40V p-ch LDMOS

ESD Evaluation. Also ESD capability was evaluated for each devices with/without sinker n+ in drain. We obtained significant improvement not only in normal HBM ESD stress test but also so-called air-gap discharge ESD. The developed LDMOS with sinker n+ achieved the ESD level of over 15kV in the air-gap discharge ESD test.

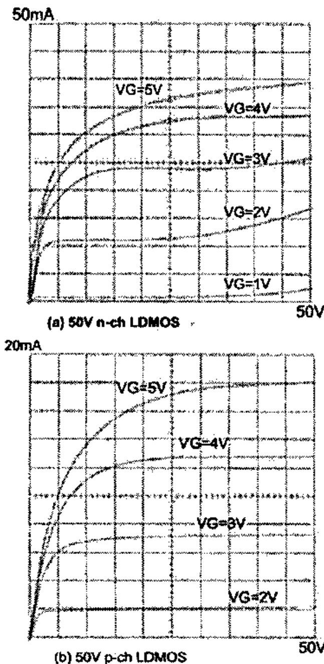

Fig.9 *ID-VD* characteristics of (a) 50V n-ch LDMOS and (b) 50V p-ch LDMOS

Other Devices and IC Application. Measured characteristics of other devices are shown in Table 1. Since the analog performances are the same as the conventional 0.6 μm BCD, it is easy and smooth for IC designer to adopt the developed process. This is very efficient to evolve generations of IC.

We report an application example of motor-driver ICs developed with the present 40V BCD, as seen in Fig.10. It is easily noticed that the present our approach is strongly effective, since LDMOS occupies the majority area of the chip in the most of the applications.

CONCLUSION

Combining a limited number of 0.35μm equivalent mask steps into 0.6μm BCD process, we have successfully developed 0.6μm design based 40V and 50V LDMOS, whose on-resistances are superior to those of 0.35μm BCD. The on-resistances of the developed 40V and 50V LDMOS are 54.3 and 69.7mWmm2, respectively. It should be noted that we adopted none of the processes which are unique to 0.35μm-generation CMOS, resulting in no special increase in cost. We notice that the present our approach is strongly effective, since LDMOS occupies the majority area of the chip in the most of applications.

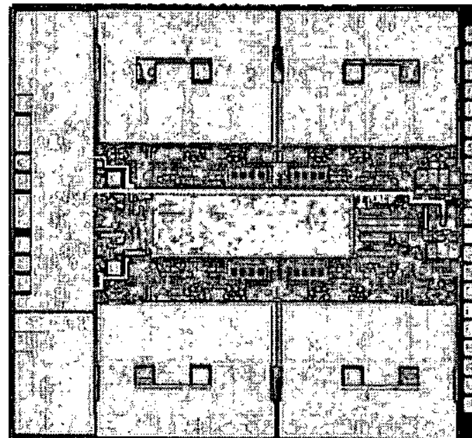

Fig.10 A photograph of motor drive IC by using this technology.

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