Advanced 60μm Thin 600V Punch-Through IGBT Concept for Extremely Low Forward Voltage and Low Turn-off Loss

Tomoko Matsudai, Hideki Nozaki, Shinichi Umekawa, Masahiro Tanaka, Motoshige Kobayashi, Hidetaka Hattori and *Akio Nakagawa

Discrete Semiconductor Div., Semiconductor Company, Toshiba Corporation
*Advanced Discrete Semiconductor Technology Laboratory, Toshiba Corporation
1 Komukai Toshiba-cho Saiwai-ku, Kawasaki 210-8583, Japan
Tel: +81-44-549-2602 Fax: +81-44-549-2883 E-mail: tomoko.matsudai@toshiba.co.jp

ABSTRACT : A vertical trench gate 600 V PT (Punch Through) IGBT structure with a new concept of thin substrate wafer with a low dose n-buffer and a transparent p-emitter is proposed to realize an excellent trade-off relation between the device on-state voltage and the switching speed. In this paper, we have fabricated and evaluated 600 V/150 A rated thin wafer PT IGBT in a 60 μm thin silicon substrate. It was experimentally confirmed that 60 μm PT IGBTs with a transparent p-emitter have an excellent trade-off relation for room temperature and 125 °C. Especially the fabricated 60 μm thin 600 V PT IGBTs have realized an on-state voltage as low as 1.23 V at 150 A/cm^2 current density with an extremely short fall-time of 60 ns for 25 °C.

INTRODUCTION

In the course of IGBT development, two typical design concepts of PT (Punch Through) IGBTs and NPT (Non Punch Through) IGBTs have been proposed and widely studied. Recently, NPT trench gate IGBT has been attracting more interest [1,2,3], because it has been believed that a lower on-state voltage and a higher switching speed can be achieved by the transparent p-emitter and the NPT structure. The typical on-state voltage drop of the conventional 600 V NPT trench gate IGBTs is 1.6 V at 180 A/cm^2 [4]. However, the ultimate limit design has not been discussed sufficiently.

In IPEC'2000, we, for the first time, proposed the device concept of 60 μm thin wafer PT IGBT with a low dose n-buffer and the transparent p-emitter by numerical simulations [5,6]. Then, the similar concept of IGBT structure, the Field Stop IGBT, was proposed [7].

In the present paper, we have experimentally verified, for the first time, that thin wafer PT IGBT with a transparent p-emitter is better than the counterpart 600 V NPT IGBTs. We fabricated and evaluated 600 V/150 A rated thin wafer PT IGBT in a 60 μm thin silicon substrate. The fabricated thin wafer PT IGBTs have exhibited an on-state voltage as low as 1.23 V at 150 A/cm^2 current density with an extremely short fall-time of 60 ns.

DEVICE STRUCTURE

The schematic cross section of proposed trench gate 600 V PT IGBTs is shown in Fig.1. The feature of the proposed structure is that the wafer thickness is very thin. The total wafer thickness is only 60 μm. The thin n-buffer layer is adopted to maintain the high breakdown voltage of more than 600 V.

In NPT IGBT, the n-drift layer is relatively thick in comparison with conventional PT IGBT. The depletion layer dose not reach the p-emitter (anode) layer, even when a high voltage is applied to the anode

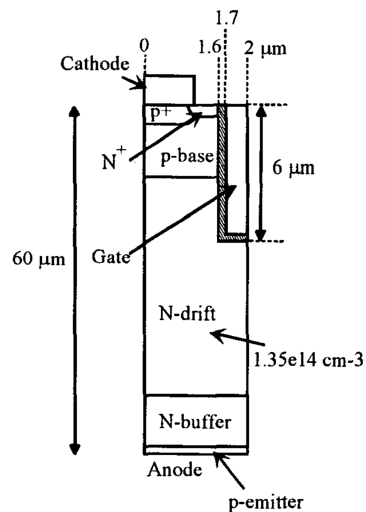

Fig.1 Cross-sectional view of the proposed PT trench gate IGBT

layer.

In the present structure, the n-drift layer is reduced to achieve a low forward voltage with retaining all the good features of NPT IGBTs. Namely, the switching speed is controlled by a low dose anode emitter with an optimally doped n-buffer layer. The lifetime in the drift layer is kept high, preventing the degradation of switching speed in an elevated temperature.

The trench width is 0.8 μm. The trench depth is 6 μm. The trench-to-trench distance is 3.2 μm. The gate oxide thickness is 120 nm. The adopted design of the cathode side is almost the same as the conventional PT IGBTs.

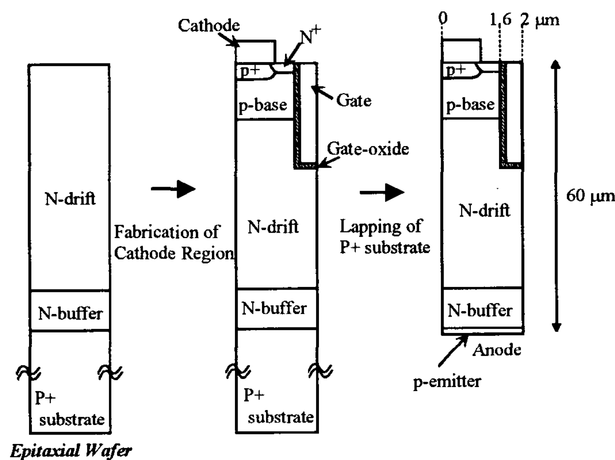

Fig. 2 Process steps of the proposed 60 μm thick PT IGBT

DEVICE FABRICATION

In Fig. 2, the fabrication process flow is outlined. First, we fabricated the whole IGBT structure in a conventional thick epitaxial wafer with an n-buffer. The doping concentration of the n-buffer was relatively low compared with conventional PT IGBT. Then, we removed the most of the p+ substrate region by grounding and a careful wet etching process so that only a very thin p-type layer (p+ substrate) remains. The remaining p-type layer served as a low efficiency p-emitter (anode). The anode metal was, then, deposited. The carrier lifetime control was not executed.

The SEM photograph of the anode region for the fabricated IGBT is shown in Fig. 3(a). The photograph shows the very thin p-type layer (p-emitter) and the pn-junction between the p-emitter and the n-buffer layer. Figure 3(b) shows the impurity distribution by SIMS

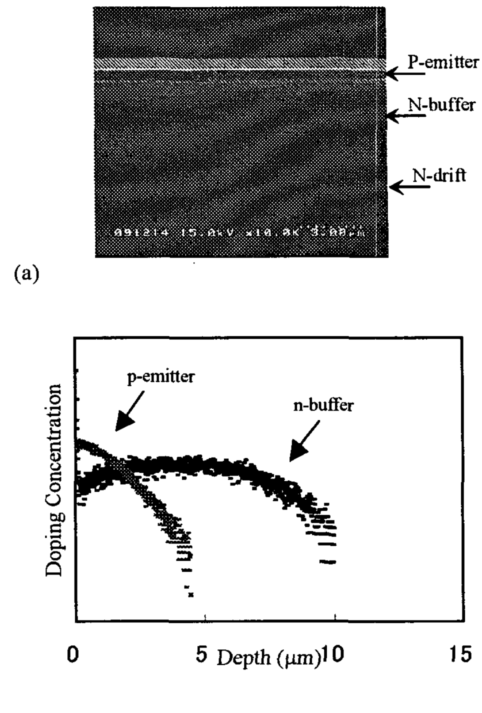

Fig. 3 SEM photograph and impurity distribution of cross section of anode region for the proposed 60 μm thick PT IGBTs

measurement. This low dose n-buffer acts to stop the electrical field and the very low dose p-type layer functions as a transparent p-emitter.

RESULTS AND DISCUSSION

The measured current-voltage characteristics of the fabricated 600 V/150 A rated IGBTs are shown in Fig. 4, for room temperature (25 °C) and 125 °C. The

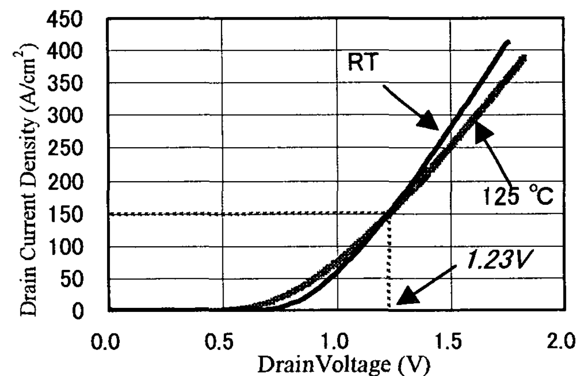

Fig. 4 Measured forward current-voltage characteristics for 60 μm thick trench gate PT-IGBTs at room temperature and 125 °C. Gate voltage is 15 V respectively.

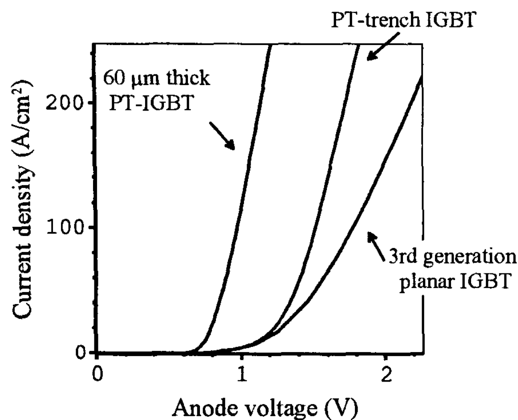

Fig. 5 Simulated forward current-voltage characteristics for conventional IGBTs and 60 μm thick trench gate IGBTs

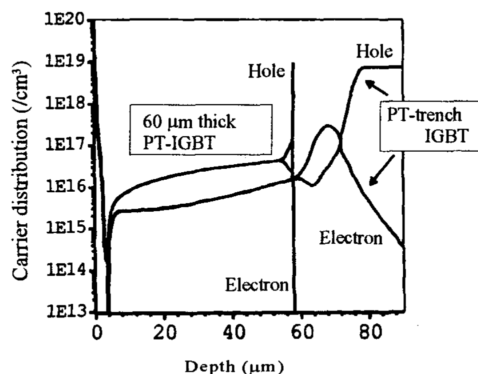

Fig. 6 Simulated carrier distribution for PT trench gate IGBTs and the proposed PT-IGBTs. Current density is 150 A/cm^2

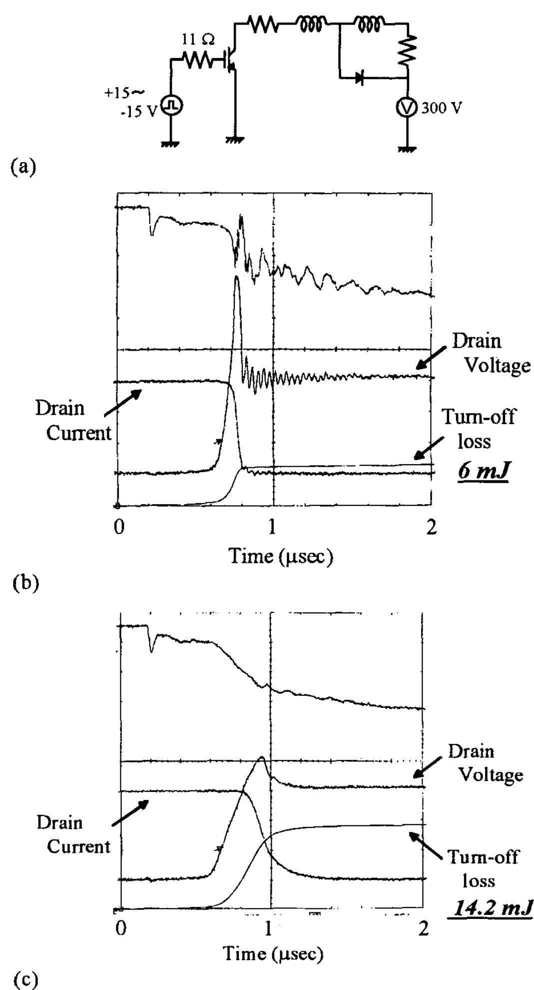

Fig. 7 Measured turn-off waveforms for 60 μm thick PT-IGBT with transparent p-emitter and circuit for turn-off measurement.

on-state voltage is 1.23 V for 120 A (150 A/cm^2) and 1.31 V for 150 A (188 A/cm^2) at room temperature.

We have simulated forward current-voltage characteristics of the proposed 60 μm thick IGBT. Figure 5 compares the simulated forward current-voltage characteristics of conventional 3rd generation planar IGBTs, PT trench gate IGBTs and the proposed 60 μm PT IGBTs. The simulated on-state voltage of the proposed IGBT is 1.04 V for 150 A/cm^2 at 300 K [5]. We assume that this measured value includes the resistance of the metal contact and other resistance component, so the measured value is a little higher than the simulated value.

Figure 6 shows the simulated carrier distribution of the conventional PT trench gate IGBTs and the proposed IGBTs when the current density is 150 A/cm^2. The left side of the graph shows the surface of the cathode region. In the proposed 60 μm thick IGBTs, the carrier densities in the n-drift layer are much higher than those of the conventional PT IGBT. This is why the proposed thin wafer PT IGBT achieves lower on-state voltage. The higher carrier density distribution mostly comes from the high carrier lifetime in the n-drift region. On the other hand, in the conventional PT IGBT, shorter carrier lifetime is necessary for improving the switching fall time.

Figure 7 shows the experimental circuit and the obtained turn-off waveforms. The applied voltage is 300 V. In Fig. 7(b), the proposed IGBT achieved a fast switching speed of 60 ns without lifetime control. The tail current rapidly decays as in PT IGBTs. The total turn-off loss was 6 mJ for 150 A current turn-off under an inductive load. The value of 6 mJ is the same as

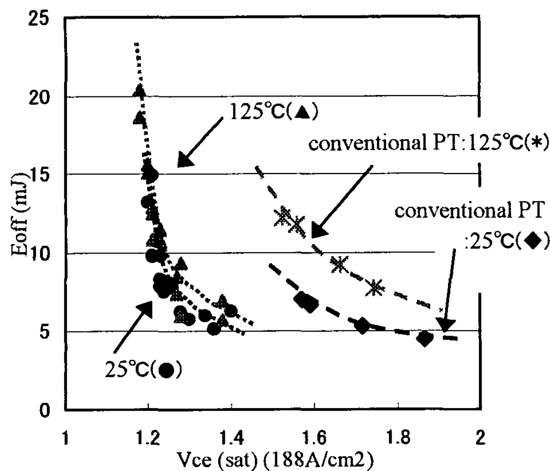

Fig. 8 Measured trade off relation between on-state voltage drops and turn-off losses for different generation IGBTs.

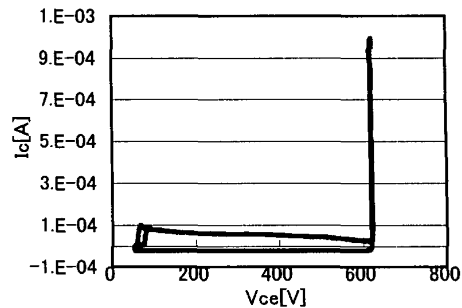

Fig. 9 Measured breakdown characteristic for 60 μm thick PT-IGBT with the trench depth of 6 μm.

conventional 600 V/150 A IGBT.

The doses of both the n-buffer and the p-emitter strongly affect the switching speed. In Fig.7(c), the turn-off loss was 14.2 mJ when the dose of p-emitter was high and the dose of n-buffer was same.

Figure 8 shows the measured trade-off relation between the device on-state voltages and the turn-off losses, when the dose of p-emitter changes. The typical characteristics of conventional PT IGBT are plotted in this figure as a comparison. The excellent trade-off relation for 600 V IGBT can be confirmed both for 25 °C and 125 °C. Especially the on-state voltages are extremely low, compared with conventional IGBTs.

In Fig. 9, it is seen that the breakdown voltage is more than 600 V for the fabricated 60 μm thin IGBT with low dose n-buffer.

CONCLUSION

We have proposed and fabricated the new concept 600 V/150 A rated PT trench-gate IGBT in 60 μm thin wafer. An extremely low on-state voltage of 1.23 V was realized, for the first time, for 600 V IGBTs with retaining the fast switching speed. Important point is to adopt the very thin substrate wafer with a low dose n-buffer layer and transparent p-emitter. The merit of fabricated design is that the lifetime control is not necessary. Furthermore, the new concept of thin substrate wafer is proposed to realize an excellent trade-off relation between the device on-state voltage and the switching speed.

Acknowledgment

The author would like to thank Senior Manager Yasuo Ashizawa and Group Manager Tsuneo Ogura for their support and advice during the course of this study.

References

[1] D.Burns, I.Deram, J.Mello, J.Morgan, I.Wan and F.Robb, "NPT-IGBT-Optimizing for manufacturability," Proc. of ISPSD'96, pp 331-334, 1996

[2] T.Laska, J.Fugger, F.Hirler and W.Scholz, "Optimizing the vertical IGBT structure - The NPT Concept as the most economic and electrically ideal solution for a 1200V IGBT", Proc. of ISPSD'96, pp 169-172, 1996

[3] T.Laska, M.Matschitsch and W.Scholz, "Ultrathin-Wafer Technology for a New 600V-NPT-IGBT," Proc. of ISPSD'97, pp 361-364, 1997

[4] M.Tanaka, S.Teramae, Y.Takahashi, T.Takeda, M.Yamaguchi, T.Ogura, T.Tsunoda and S.Nakao, "600 V Trench-gate NPT-IGBT with Excellent Low On-State Voltage," Proc. of ISPSD'2000, pp 279-282, 2000

[5] T.Matsudai, K.Kinoshita and A. Nakagawa, "New 600 V Trench Gate Punch-Through IGBT Concept with Very Thin Wafer and Low Efficiency p-emitter, having an On-state Voltage Drop lower than Diodes," Proc. of IPEC 2000, pp 292-296, 2000

[6] Japanese Patent Laid Open (Kokai) No.11-274484, 1999

[7] T.Laska, M.Munzer, F.Pfirsch, C.Schaeffer and T.Schmidt, "The Field Stop IGBT (FS IGBT) – A New Power Device Concept with a Great Improvement Potential," Proc. of ISPSD'2000, pp 355-358, 2000