0.6 \mu m BiCMOS Based 15 and 25V LDMOS for Analog Applications

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Abstract

In the present paper, we report the development of complementarily 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS. The developed LDMOS achieved high on-state breakdown voltages for the gate voltage of 5.0V. The on-resistance values of the developed 15V and 25V n-ch LDMOS achieves 22.7 and 27.5 $\text{m}\Omega \cdot \text{mm}^2$, respectively. The characteristics of bipolar transistors and CMOS are also sufficiently good.

Device Structure

Figure 1 shows cross-sectional views of an Adaptive Resurf (2-step n-offset structure) LDMOS. Considering compatibility with BiCMOS process, we chose the n-epi/n+/p- substrate. The epitaxial layer resistivity and thickness is chosen so that the optimized 18 V npn and pnp transistors, shown in fig. 3 and 4, were realized. The difference between a conventional LDMOS and an Adaptive Resurf LDMOS is whether it has a second n-Resurf layer of an optimally high ion implantation dose or not.

Experimental Results

We fabricated 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS, using 0.6 \mu m BiCMOS process with an additional ion implantation process as shown in fig. 5. The ion implantation of the first and the second n-offset layers for n-ch LDMOS and p-offset layer for p-ch LDMOS are carried out before LOCOS oxidation. The thickness of the LDMOS gate oxide is 14 nm, which is the same as 5V CMOS.
A. LDMOS

Figure 6 (a) and (b) show the dependence of static and on-state breakdown voltages and on-resistance on the first and second n-offset layer dose (normalized value), respectively. It is effective to optimize first n-offset layer dose in order to minimize on-resistance. As the first n-offset layer dose increases, the breakdown voltage reduces and the on-resistance decreases. The impurity dose of the second n-offset layer was chosen to be less than 1×10^{13}cm^{-2}.

The optimized on-state breakdown voltage exceeded 30V for 25V LDMOS when the second n-offset layer dose is optimized both for on-resistance and static breakdown voltage. Since the device dimensions of 15V LDMOS are the same as those of 25 V LDMOS, the second n-offset layer dose of 15V LDMOS was chosen to be greater than that of 25V LDMOS so that the on-resistance is minimized.

Figures 7 (a), (b) and (c) show the measured I-V characteristics for the fabricated 15V LDMOS, 25V n-ch and p-ch LDMOS. The measured values of the device characteristics are listed in Table I. The developed LDMOS achieve high on-state breakdown voltages for the gate voltage of 5.0 V. The values of specific on-resistance are 22.7 and 27.5 mΩ·mm² for 15 and 25V n-ch LDMOS respectively. The on-resistance value of 25V p-ch LDMOS was 111 mΩ·mm².

B. Bipolar transistors and CMOS

Measured characteristics for the fabricated 18V bipolar transistors and CMOS are shown in Table II. These characteristics of these devices are sufficiently good for analog circuits. This result shows that the developed LDMOS structure is suitable for fabrication with bipolar transistors and CMOS.

Summary

We presented the development of complementally 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS. The developed LDMOS achieved high on-state breakdown voltages for the gate voltage of 5.0V. The on-resistance values of the developed 15V and 25V n-ch LDMOS achieved 22.7 and 27.5 mΩ·mm², respectively. The characteristics of bipolar and CMOS were also sufficiently good.

Acknowledgment

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References


Table I Measured Values for the developed LDMOS

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<tr>
<th>Voltage (V)</th>
<th>15V nch LDMOS</th>
<th>25V nch LDMOS</th>
<th>25V pch LDMOS</th>
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<tr>
<td>Static Breakdown Voltage</td>
<td>21.9</td>
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<td>34.0</td>
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<td>On-state Breakdown Voltage</td>
<td>24.5</td>
<td>33.0</td>
<td>50.0</td>
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<tr>
<td>On-resistance (mΩ·mm²)</td>
<td>22.7</td>
<td>27.5</td>
<td>111.3</td>
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Table II Measured values for the bipolar transistors and CMOS

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<tr>
<th>Transistor</th>
<th>Vceo (V)</th>
<th>hFE</th>
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<td>npn transistor</td>
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<td></td>
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<tr>
<td>VA</td>
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<tr>
<td>hFE</td>
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<tr>
<td>pnp transistor</td>
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<td>NMOS</td>
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<tr>
<td>Vth</td>
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<tr>
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Fig. 1 Cross-sectional view of an Adaptive Resurf (2-step n-implant structure) LDMOS. 2nd n-offset layer improves on-state breakdown voltage.

Fig. 2 Cross-sectional view of a p-channel LDMOS. Because of lower carrier mobility, compared with n-channel LDMOS, the current density of a p-channel LDMOS is not so high as that of n-channel LDMOS. Conventional Resurf p-channel LDMOS can achieve a high on-state breakdown voltage.

Fig. 3 Cross-sectional view of an npn transistor. The epitaxial layer resistivity and thickness is chosen so that the optimized 18 V npn and pnp transistors were realized.

Fig. 4 Cross-sectional view of a pnp transistor

Fig. 5 Process flow of the developed LDMOS, bipolar transistors and CMOS. Additional ion implantation of the first and the second n-offset layers for n-ch LDMOS and p-offset layer for p-ch LDMOS are carried out before LOCOS oxidation.
Fig. 6 (a) Dependence of measured breakdown voltage and on-resistance on the first n-offset layer dose. The 2nd offset dose value is fixed at 3.0. It is effective to optimize first n-offset layer dose in order to minimize on-resistance. As the first n-offset layer dose increases, the breakdown voltage reduces and the on-resistance decreases.

Fig. 6 (b) Dependence of measured breakdown voltage and on-resistance on the 2nd n-offset layer dose. The 1st offset dose value is fixed at 2.0.

Fig. 7 (a) The measured I-V characteristics of developed 15V nch LDMOS.

Fig. 7 (b) Measured I-V characteristics of developed 25V nch LDMOS.

Fig. 7 (c) Measured I-V characteristics of 25V pch LDMOS. Developed LDMOS achieve high on-state breakdown voltages for the gate voltage of 5.0V.