0.6 μm BiCMOS Based 15 and 25V LDMOS for Analog Applications

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Abstract

In the present paper, we report the development of complementally 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS. The developed LDMOS achieved high on-state breakdown voltages for the gate voltage of 5.0V. The on-resistance values of the developed 15V and 25V n-ch LDMOS achieves 22.7 and 27.5 mΩ·mm^2, respectively. The characteristics of bipolar transistors and CMOS are also sufficiently good.

Introduction

Many studies on low on-resistance power MOSFETs in the 20-30V range have been conducted, reflecting the fact that these devices have various applications such as computer peripheral. It was recently reported that a 25 V LDMOS achieved a specific on-resistance as low as 18 mΩ·mm^2 [1].

If LDMOS can be used in place of bipolar transistors in analog ICs, the device area will be reduced because of lower specific on-resistance of LDMOS. One drawback of conventional LDMOS is that the breakdown voltage degrades as the drain current increases, and the I-V curves show snapback characteristics. The snapback characteristics prevent LDMOS from being applied in analog ICs. The mechanism of snapback characteristics was discussed in Refs. [2-5]. We proposed Adaptive Resurf concept[2] (a 2-step Resurf structure on p-epi or a 2-step shallow n-offset structure on n-epi) in order to solve this problem[2,3] and experimentally verified the effectiveness of the Adaptive Resurf[6]. Low voltage LDMOS of a low on-resistance is required for the application of battery powered mobile equipments. In addition, these LDMOS are required to be fabricated using conventional BiCMOS process, because bipolar transistors are still important precision component for analog circuits.

In the present paper, we report the development of complementally 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS. The developed LDMOS achieved high on-state breakdown voltages for the gate voltage of 5.0V. The on-resistance values of the developed 15V and 25V n-ch LDMOS achieves 22.7 and 27.5 mΩ·mm^2, respectively.

Device Structure

Figure 1 shows cross-sectional views of an Adaptive Resurf (2-step n-offset structure) LDMOS. Considering compatibility with BiCMOS process, we chose the n-epi/n+/p- substrate. The epitaxial layer resistivity and thickness is chosen so that the optimized 18 V npn and pnp transistors, shown in fig. 3 and 4, were realized. The difference between a conventional LDMOS and an Adaptive Resurf LDMOS is whether it has a second n-Resurf layer of an optimally high ion implantation dose or not.

The reason why the on-state breakdown voltage is degraded is described in Ref. [2,3,6]. The first n-offset layer is completely compensated in a highly biased on-state by the negative charge of the high density electron current. The more heavily and optimally doped second n-offset layer remains uncompensated and adaptively provides optimum positive space charges. This results in a high on-state breakdown voltage by the reduced surface field. Figure 2 shows a cross-sectional view of a p-channel LDMOS. Because of lower carrier mobility, compared with n-channel LDMOS, the current density of a p-channel LDMOS is not so high as that of n-channel LDMOS. Conventional Resurf p-channel LDMOS can achieve a high on-state breakdown voltage.

Experimental Results

We fabricated 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS, using 0.6 μm BiCMOS process with an additional ion implantation process as shown in fig. 5. The ion implantation of the first and the second n-offset layers for n-ch LDMOS and p-offset layer for p-ch LDMOS are carried out before LOCOS oxidation. The thickness of the LDMOS gate oxide is 14 nm, which is the same as 5V CMOS.

A. LDMOS

Figure 6 (a) and (b) show the dependence of static and on-state breakdown voltages and on-resistance on the first and second n-offset layer dose (normalized value), respectively. It is effective to optimize first n-offset layer dose in order to minimize on-resistance. As the first n-offset layer dose increases, the breakdown voltage reduces and the on-resistance decreases. The impurity dose of the second n-offset layer was chosen to be less than 1e13cm^{-2}.

The optimized on-state breakdown voltage exceeded 30V for 25V LDMOS when the second n-offset layer dose is optimized both for on-resistance and static breakdown voltage. Since the device dimensions of 15V LDMOS are the same as those of 25 V LDMOS, the second n-offset layer dose of 15V LDMOS was chosen to be greater than that of 25V LDMOS so that the on-resistance is minimized.

Figures 7 (a), (b) and (c) show the measured I-V characteristics for the fabricated 15V LDMOS, 25V n-ch and p-ch LDMOS. The measured values of the device characteristics are listed in Table I. The developed LDMOS achieve high on-state breakdown voltages for the gate voltage of 5.0V. The values of specific on-resistance are 22.7 and 27.5 $m\Omega\cdot mm^2$ for 15 and 25V n-ch LDMOS respectively. The on-resistance value of 25V p-ch LDMOS was 111 $m\Omega\cdot mm^2$.

B. Bipolar transistors and CMOS

Measured characteristics for the fabricated 18 V bipolar transistors and CMOS are shown in Table II. These characteristics of these devices are sufficiently good for analog circuits. This result shows that the developed LDMOS structure is suitable for fabrication with bipolar transistors and CMOS.

Summary

We presented the development of complementally 25V LDMOS, 15V n-ch LDMOS, 18V npn/pnp and 5V CMOS. The developed LDMOS achieved high on-state breakdown voltages for the gate voltage of 5.0V. The on-resistance values of the developed 15V and 25V n-ch LDMOS achieved 22.7 and 27.5 $m\Omega\cdot mm^2$, respectively. The characteristics of bipolar and CMOS were also sufficiently good.

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Table I Measured Values for the developed LDMOS

	15V nch LDMOS	25V nch LDMOS	25V pch LDMOS
Static Breakdown Voltage (V)	21.9	30.0	34.0
On-state Breakdown Voltage (V)	24.5	33.0	50.0
On-resistance ($m\Omega\cdot mm^2$)	22.7	27.5	111.3

Table II Measured values for the bipolar transistors and CMOS.

npn transistor	Vceo	>25 V
	VA	100
	hFE	100
pnp transistor	Vceo	>25 V
	hFE	90
NMOS	BV	>8 V
	Vth	0.8 V
PMOS	BV	>8 V
	Vth	0.8 V

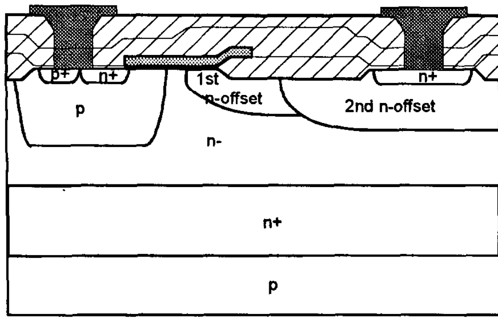


Fig. 1 Cross-sectional view of an Adaptive Resurf (2-step n-implant structure) LDMOS. 2nd n-offset layer improves on-state breakdown voltage.

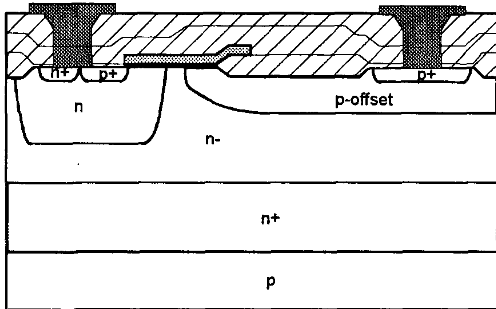


Fig. 2 Cross-sectional view of a p-channel LDMOS. Because of lower carrier mobility, compared with n-channel LDMOS, the current density of a p-channel LDMOS is not so high as that of n-channel LDMOS. Conventional Resurf p-channel LDMOS can achieve a high on-state breakdown voltage.

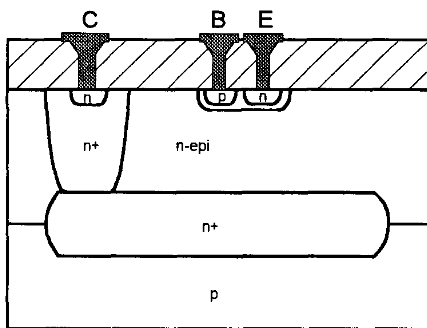


Fig. 3 Cross-sectional view of an npn transistor. The epitaxial layer resistivity and thickness is chosen so that the optimized 18 V npn and pnp transistors were realized.

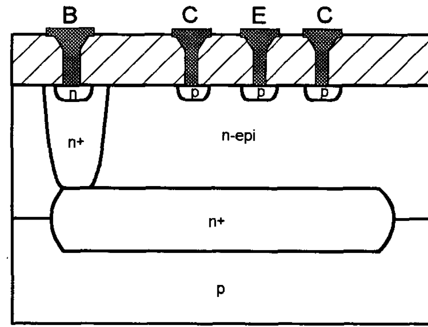


Fig. 4 Cross-sectional view of a pnp transistor

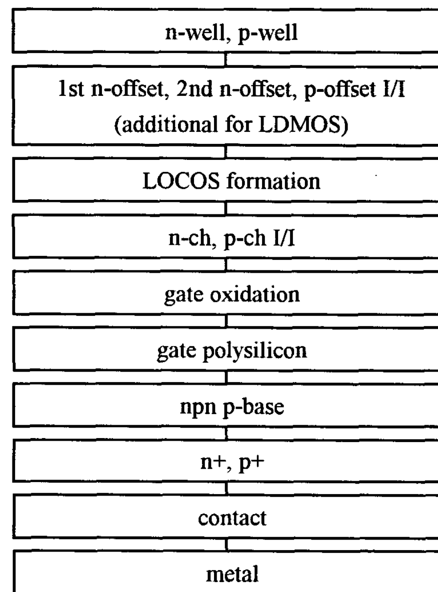


Fig. 5 Process flow of the developed LDMOS, bipolar transistors and CMOS. Additional ion implantation of the first and the second n-offset layers for n-ch LDMOS and p-offset layer for p-ch LDMOS are carried out before LOCOS oxidation.

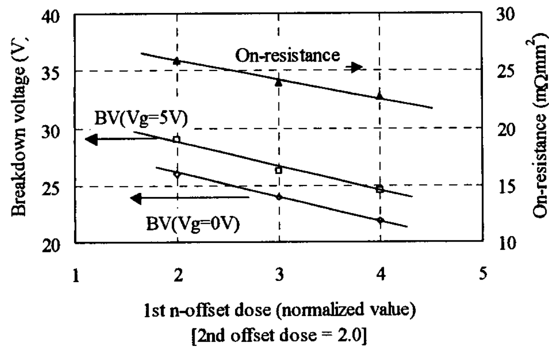


Fig. 6 (a) Dependence of measured breakdown voltage and on-resistance on the first n-offset layer dose. The 2nd offset dose value is fixed at 3.0. It is effective to optimize first n-offset layer dose in order to minimize on-resistance. As the first n-offset layer dose increases, the breakdown voltage reduces and the on-resistance decreases.

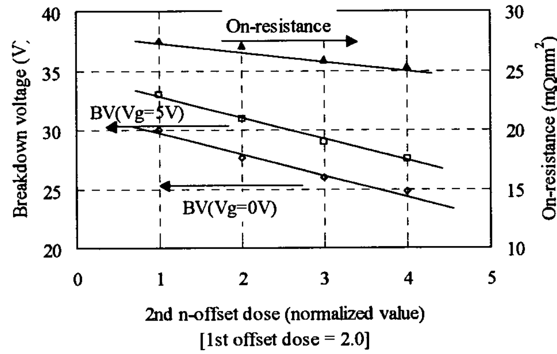


Fig.6 (b) Dependence of measured breakdown voltage and on-resistance on the 2nd n-offset layer dose. The 1st offset dose value is fixed at 2.0.

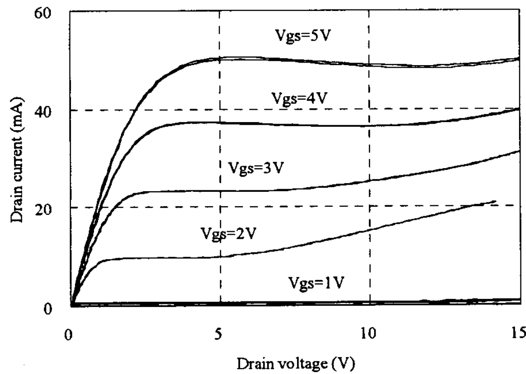


Fig.7 (a) The measured I-V characteristics of developed 15V nch LDMOS.

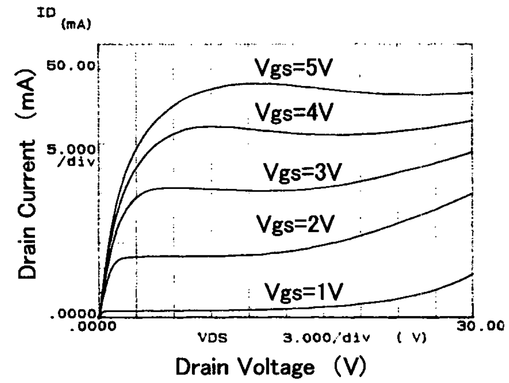
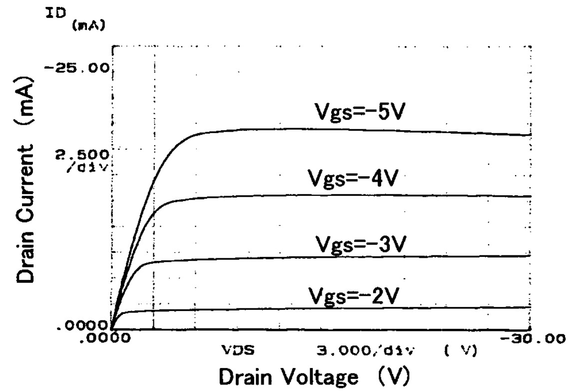


Fig.7 (b) Measured I-V characteristics of developed 25V nch LDMOS.



(c)

Fig.7 (c) Measured I-V characteristics of 25V pch LDMOS. Developed LDMOS achieve high on-state breakdown voltages for the gate voltage of 5.0V.