Improved 20V Lateral Trench Gate Power MOSFETs with Very Low On-resistance of 7.8 mΩ·mm^2

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Abstract--**We propose an improved lateral trench gate MOSFET with a new trench drain contact. The device is predicted to achieve 25V breakdown voltage and a very low on-resistance of 7.8 mΩ·mm^2, which is by 20% lower than that of previously proposed standard lateral trench gate MOSFETs. The proposed trench contact uniformly distributes the electron current in the drift layer, and effectively reduces the device on-resistance.**

In the present paper, we also show the detailed electrical characteristics of the fabricated standard trench gate LDMOS. The large current turn-off capability of 1.1×10^4 A/cm^2 was achieved by the fabricated device.

I. Introduction

Many studies of low on-resistance 20 V range lateral power MOSFETs have been conducted because these devices have a variety of applications in computer peripherals. In 1999, we proposed 20V lateral trench gate MOSFETs, shown in Figs.1 & 2, which have successfully achieved a record low specific on-resistance 13 mΩ·mm^2[1, 2]. Conventionally, trench gate structures have been used for vertical trench MOSFETs, where channel current flows vertically on the trench sidewalls. The unique feature of the lateral trench gate MOSFETs is that the electrons spread from the source layer into the channel regions, induced both on the trench terraces and on the trench sidewalls, and that the electrons flow laterally on the trench sidewalls from the source to the drain. The lateral trench gate MOSFETs were fabricated, using the standard 0.6μm CMOS process with an additional trench gate formation process. The fabricated device achieved 13 mΩ·mm^2 of on-resistance with the breakdown voltage of 25V, which is the lowest on-resistance ever reported, and is even lower than that of the vertical trench MOSFETs. The previously reported lowest specific on-resistance of 25 V lateral DMOS was 18 mΩ·mm^2 [3].

In the present paper, we propose an improved lateral trench gate MOSFET with a trench drain contact, which is effective to achieve a further lower on-resistance of 7.8 mΩ ·mm^2 with 25V breakdown voltage.

II. Improved Trench Gate LDMOS

Figure 1 shows a top view of the proposed new trench gate LDMOS. The top view of the proposed trench LDMOS is the same as that of the previously proposed standard trench gate LDMOS.

Figures 2 (a) and (b) show cross-sectional views of the standard lateral trench gate MOSFETs along the line A-A' and B-B' in Fig. 1. Figures 2 (c) show the cross-sectional views of the proposed lateral trench LDMOS along the line A-A' in Fig. 1. A number of fine trenches were formed, running from the source to the drain n-layer.

The trench width, the trench-to-trench space and the depth are 0.4 μm, 0.4μm and 1.0μm, respectively. Since the terraces and the side walls of the trenches work as channels, the effective gate width is 3.5 times as wide as that of the conventional planer LDMOS.

Figure 3 shows the SEM photograph of the fabricated trench gates, which corresponds to the cross-section of Fig. 2 (b). The photograph shows that the fine trenches are formed and filled up with the gate poly-silicon.

It is important to reduce the spreading resistance from the channel to the shallow source layer to achieve a low on-resistance. The trench gate must overlap sufficiently with the source n+ diffusion layer. The overlapped length of the trench and the source n+ layer were optimized in order to reduce the spreading resistance and to realize uniform electron current flow in the trench sidewall.

In the new trench LDMOS, the drain metal contact is performed by trenches as seen in Fig.2(c). The trench contact is found to be effective to reduce the n-drift layer resistance. In the n-drift, the electrons flow uniformly, being widely spread in the depth direction. The trench drain contact reduces the spreading resistance from the drain contact.

Calculations were carried out using 3D device simulator dessis-3D in order to confirm the effect of the drain trench contact. Figure 4 shows the dependence of the on-resistance on the drain trench depth. It was found that the on-resistance reduces as the drain trench becomes deeper. If 1μm deep trench contact is adopted, 20% on-resistance

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improvement is expected.

Figure 5 (a) and (b) compares the current density distributions between the standard trench gate LDMOS and the proposed trench gate LDMOS. It is seen that the trench contact realizes more uniformly distributed electron current flow in the n-drift layer, eliminating the spreading resistance from the drain metal contact.

Figure 6 shows the calculated current voltage curves of the proposed trench LDMOS with 14nm thick gate oxide for the gate voltages of 0V and 5V. The static breakdown voltage is 25V. The on-resistance is 7.8 $m\Omega \cdot mm^2$, which is the lowest value ever reported.

Figure 7 compares the measured and calculated specific on-resistances of the proposed trench LDMOS and the fabricated standard trench LDMOS. The calculated on-resistance for the standard trench LDMOS is $10m\Omega \cdot mm^2$, whereas the fabricated device on-resistance was $13m\Omega \cdot mm^2$. The difference between simulated and measured on-resistances is assumed to be attributed to the degraded channel mobility due to the surface roughness [4].

III. Switching Characteristics Of Lateral Trench Gate Mosfets

In this section, we report the details on the electrical characteristics of the fabricated standard lateral trench MOSFETs.

Figures 8 and 9 show the static breakdown characteristics and the measured current voltage curves. The measured on-resistance was $13m\Omega \cdot mm^2$.

Figure 10 shows a resistive load switching waveforms for the standard trench gate LDMOS. The switching frequency is 1MHz. Typical turn-on and turn-off times are 15ns and 40ns, respectively.

Short-circuit withstanding capability for standard trench gate LDMOSFETs is shown in Fig. 11. The applied DC drain bias is 12 V and the gate voltage is 5 V. The device withstood 1.1 x $10^4 A/cm^2$ of current density for 100 μsec under the short circuit condition.

IV. Conclusion

In the present paper, we proposed an improved lateral trench gate MOSFET with a trench drain contact. It was predicted that the trench contact uniformly distributes the electron current flowing in the drift layer and effectively reduce its on-resistance to 7.8 $m\Omega \cdot mm^2$ with 25V breakdown voltage. We also showed the measured electrical characteristics of standard trench gate LDMOS. The large current turn-off capability of 1.1×10^4 A/cm^2 and the sufficient ruggedness in short-circuit withstanding capability of 100 μsec was achieved by the fabricated device.

Acknowledgement

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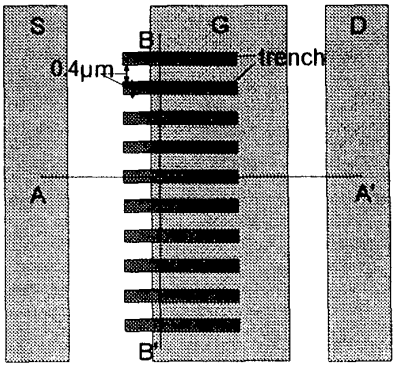

Fig. 1 Top view of the proposed trench gate 20 V LDMOS

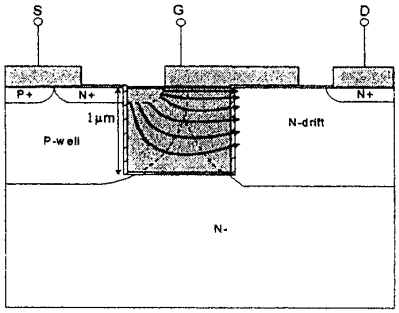

Fig.2(a) Cross-sectional view of stnadard trench gate LDMOS of line A-A' in Fig. 1

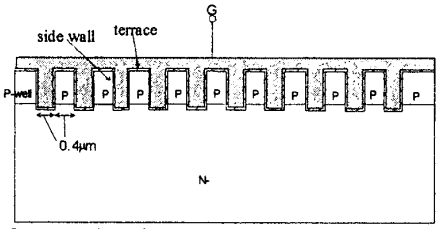

Fig.2(b) Cross-section of line B-B' in Fig. 1

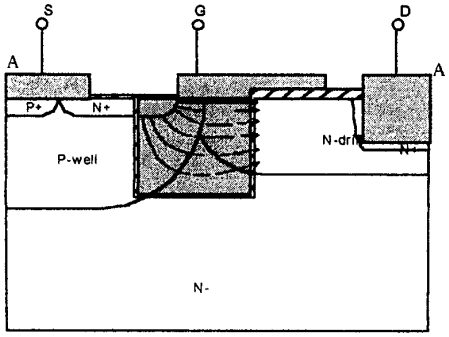

Fig.2(c) Cross-sectional view of improved trench gate LDMOS of line A-A' in Fig. 1

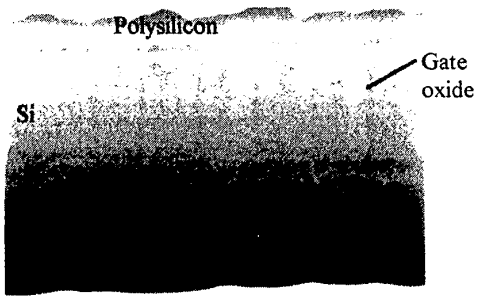

Fig. 3 SEM photograph for the cross-section correspond to Fig.2 (b)

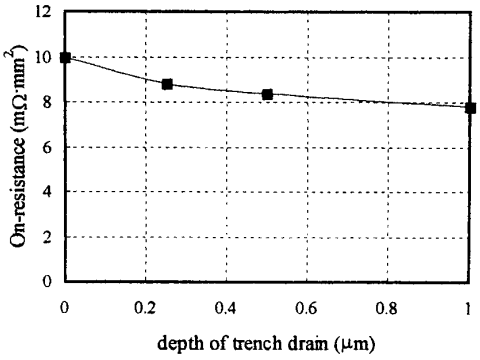

Fig. 4 Dependence of on-resistance on the depth of trench drain contact

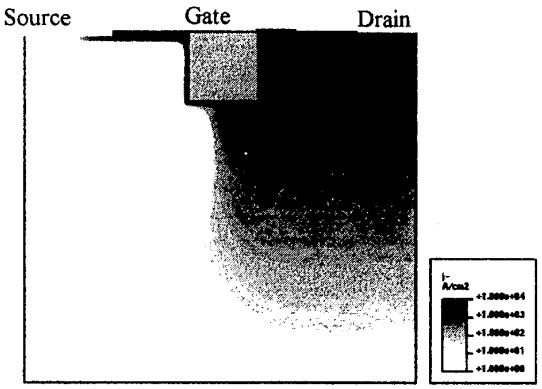

Fig. 5 (a) Electron current density distribution for Standard trench gate LDMOS

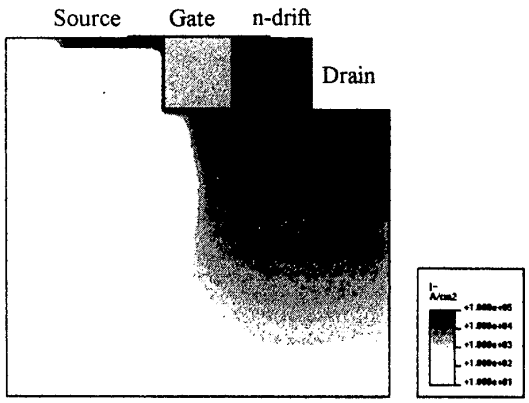

Fig. 5 (b) Electron current density distribution for Improved trench gate LDMOS

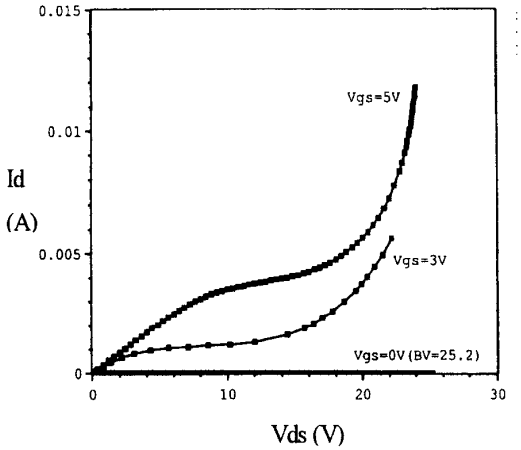

Fig. 6 Calculated I-V characteristics of new lateral trench MOSFETs. Breakdown voltage is 25V. (Device Area = 3.6 μm^2)

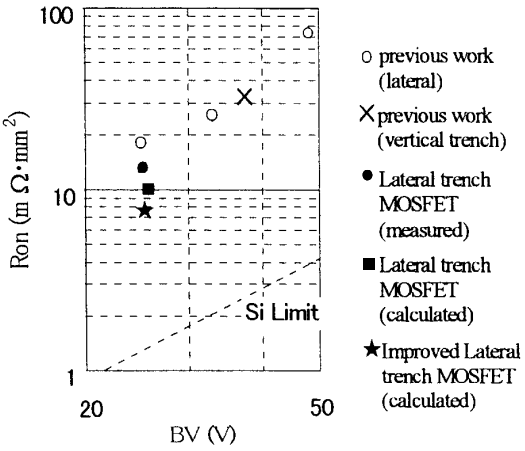

Fig. 7 Comparison of state of the art on-resistance vs. Breakdown voltage.

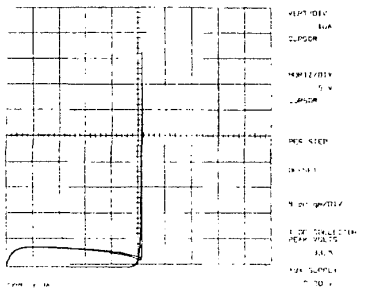

Fig.8 Typical static breakdown characteristics of a standard lateral trench MOSFET.

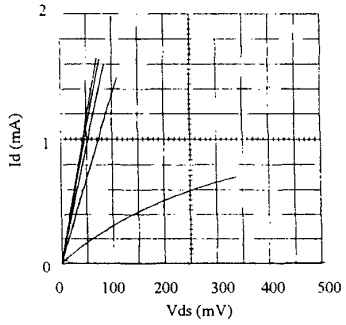

Fig.9 Typical I-V curves of standard lateral trench MOSFETs.

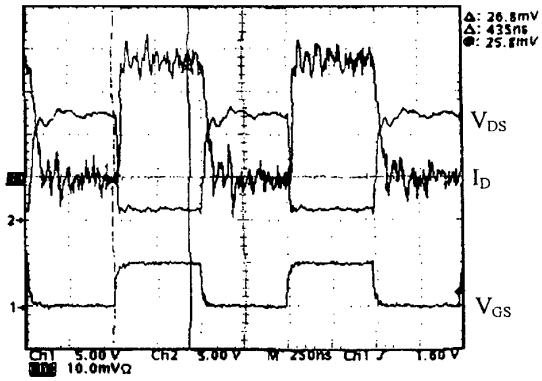

Fig. 10 Resistive load 1MHz switching waveforms for trench gate LDMOS. (Drain current: 10mA/Div., Drain voltage: 5V/Div., Gate voltage: 5V/Div., Time:250ns/Div.)

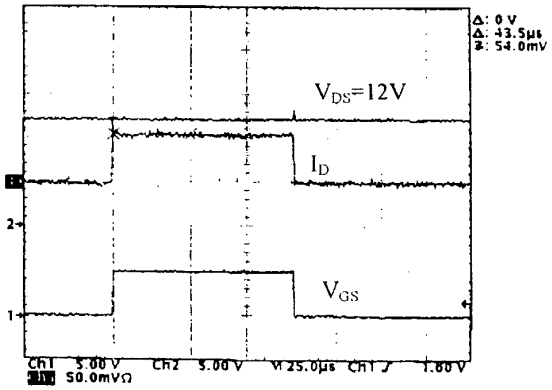

Fig. 11 Short circuit waveform for trench gate LDMOS. (Drain voltage: 5V/Div., Drain current: 50mA/Div., Gate voltage:5V/Div., Time: 25μs/div.)