New 600 V Trench Gate Punch-Through IGBT Concept with Very Thin Wafer and Low Efficiency p-emitter, having an On-state Voltage Drop lower than Diodes

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Abstract : A vertical trench gate 600 V punch through IGBT(Insulated Gate Bipolar Transistor) structure with a new concept of thin substrate wafer with a low dose n-buffer is proposed, for the first time, to realize an excellent trade-off relation between the device on-state voltage and the switching speed. This paper outlines the ultimate limit design and characteristics, using a very thin wafer in trench gate IGBTs with the transparent p+ emitter and the n-buffer layer. The realized forward voltage drop is predicted to be even lower than that of 600 V diodes with retaining a fast switching speed.

INTRODUCTION

In the vertical devices, the trench gate structure has been widely introduced both for low voltage 600 V IGBTs and high voltage 4.5 kV IGBTs[1,2,3]. The reason is because of the significant improvement that has been achieved in the trade-off relation between a device on-state voltage and a switching speed. It has been widely believed that a lower on-state voltage can be attained by electron injection enhancement from the MOS channel into the drift layer. This leads to an idea to make trench gate deeper and deeper. The current 4^{th} generation trench IGBTs adopts 6 μm deep trench gates.

On the other hand, recently, NPT (Non-Punch-Through) trench gate IGBT is attracting considerable interest, since NPT-IGBT has the good trade-off relation[4,5,6]. NPT-IGBT has relatively thicker n-drift layer compared with conventional PT (Punch-Through)-IGBT. In NPT-IGBT, the n-drift layer is sufficiently thick so that the depletion layer should not reach the p+ emitter (anode) layer. It is known that a thinner wafer improves the Vce(sat) and the fall time, although it affects the forward blocking voltage. No papers have discussed the ultimate limit design, using a very thin wafer, especially in trench gate IGBTs. It has been widely known that a low on-state voltage and a high switching speed can be achievable using NPT type IGBT design, adopting the transparent p+ emitter. However, the typical on-state voltage drop of NPT trench gate IGBTs is 1.65 V at 150 A/cm^2.

In the present paper, we successfully introduce the idea of very thin wafer punch-through IGBTs, for the first time, and numerically study the potential of 600 V IGBTs, having an on-state voltage drop lower than diodes. We propose very thin substrate wafer with a low dose n-buffer and the transparent p+ emitter. The proposed IGBT will realize a on-state voltage drop that is even lower than that of 600 V diodes with retaining fast switching speed! The merits of proposed design are that the lifetime control is not necessary and the shallow trench gate is sufficient. This is very important feature to successfully realize low on-state voltage and to reduce the total power loss.

DEVICE STRUCTURE

The schematic cross section of proposed 600 V trench-gate IGBTs is shown in Fig. 1. The first feature of this structure is that the total wafer thickness is only 58 μm! This substrate wafer has a n-buffer layer to maintain the high breakdown voltage, because the depletion layer spreads throughout the n-drift layer. A low dose shallow boron diffusion layer is adopted as a low efficiency p+ emitter (IGBT collector) to attain high speed switching. The trench width is 0.6 μm, and the thickness of the gate oxide in the trench was 120 nm. The trench to trench distance is about 3.2 μm and the trench depth is 6 μm. The half cell size is 2 μm. In this structure, we assumed that the lifetime control is

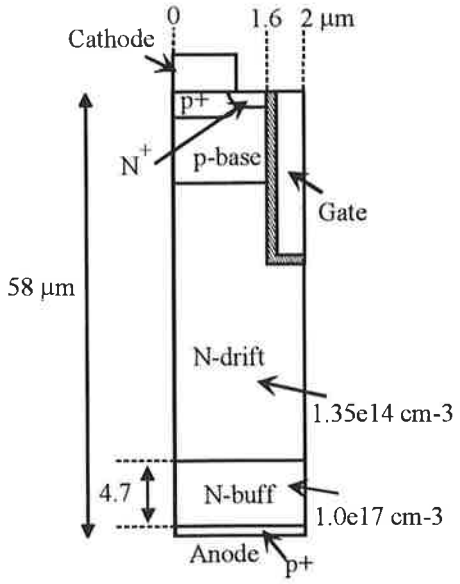
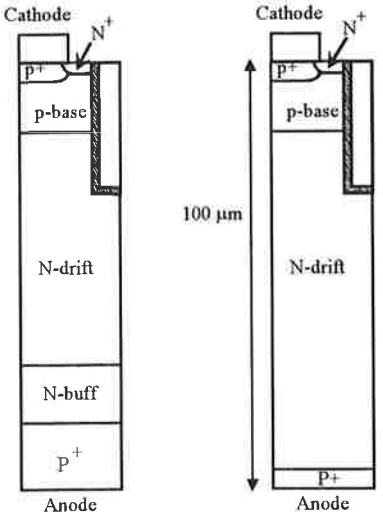


Fig. 1 Cross-sectional view of the simulated trench gate IGBT



(a) PT-IGBT (b) NPT-IGBT

Fig. 2 Cross-sectional view of the conventional trench gate IGBT

not necessary. Thus, the lifetime is 10 μsec in the simulation. The design of cathode side is almost the same as the conventional PT-IGBTs. Only the peak concentration of p-base is slightly little because of the condition without lifetime control.

Figure 2 shows the conventional 600 V trench gate IGBT using PT type substrate wafer and NPT type substrate wafer with the transparent p+ emitter. This PT-IGBT adopts epitaxial wafers with n-buffer layer and electron irradiation method for lifetime

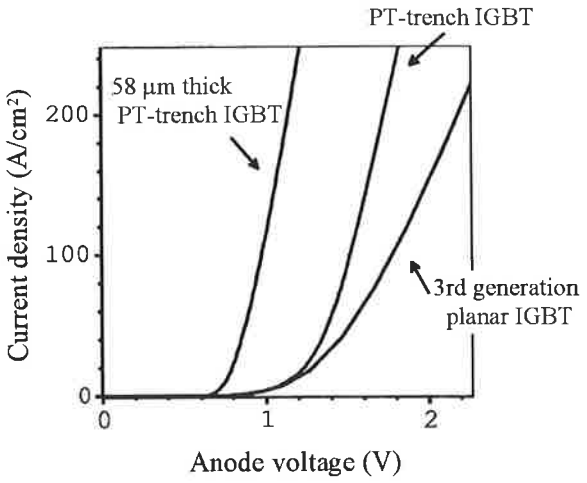


Fig. 3 Simulated forward current-voltage characteristics for conventional IGBTs and 58 μm thick trench gate IGBTs

control. The demerit of epitaxial wafers is high cost. On the other hand, the on-state voltage drop of NPT-IGBT isn't sufficiently low, because the n-drift layer is relatively thick.

RESULTS AND DISCUSSION

Current-voltage characteristic

Figure 3 compares the calculated forward current-voltage characteristics of conventional 3rd generation planar IGBTs, PT trench gate IGBTs and the proposed 58 μm thick PT trench gate IGBTs. The gate voltage is 15 V respectively. Even if the planar DMOS IGBT cell is reduced, it is experimentally confirmed that the on-state voltage drops cannot be lower than 1.6 V at 100 A/cm^2 because of the JFET effects. If the trench gate is adopted to eliminate JFET resistance, forward voltage can be reduced. However, the typical on-state voltage drop of the conventional PT trench gate IGBTs is 1.5 V at 150 A/cm^2.

On the other hand, the simulated on-state voltage drop of the proposed 58 μm thick IGBT is only 1.04 V for 150 A/cm^2 at 300 K! This is even lower than a voltage drop of 600 V diodes. It is verified that the very thin substrate wafer with a low dose n-buffer and transparent p+ emitter is effective in reducing the on-state voltage of trench gate IGBTs.

Figure 4 shows the simulated carrier distribution of the conventional PT trench gate IGBTs and the proposed IGBTs when the current density is 150 A/cm^2. The left side of the graph shows the surface of the devices with the trench gate regions. In conventional

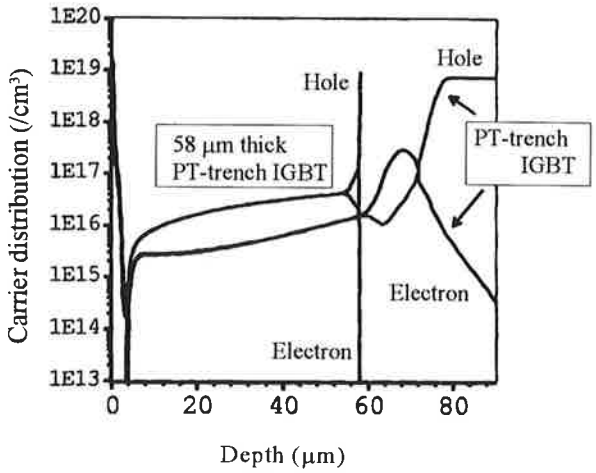


Fig. 4 Simulated carrier distribution for PT trench gate IGBTs and 58 μm thick trench gate IGBTs. Current density is 150 A/cm^2.

PT IGBT, it is found that the stored carrier in the n-drift layer near the surface of the device appeared with the IE-effect. In the proposed 58 μm thick IGBTs without lifetime control, the carrier densities in the n-drift layer were much higher than those of the conventional PT IGBT. This is why the proposed thin wafer PT IGBT achieves lower on-state voltage. The higher carrier density distribution mostly comes from the high carrier lifetime in the n-drift region. On the other hand, in the conventional PT IGBT, shorter carrier lifetime is necessary for improving the switching fall time.

Forward current-voltage characteristics were also calculated for the proposed thin wafer PT IGBT with further finer trench gate design rule. The obtained on-state voltage drop of finer trench cell IGBTs was only 0.97 V for 200 A/cm^2.

Turn-off characteristic

Figure 5 shows the external circuit for the turn-off simulation and the parameters in the simulated system. These parameters are same as the experimental condition. The proposed IGBT shown in Fig.1 achieved 170 ns fall-time without lifetime control at a 150 A/cm^2 current density as shown in Fig.6. Figure 7 shows the trade off relation between on-state voltage drop and fall time. PT-IGBTs have comparatively good trade off relation using trench gate structure. It was found that the proposed 58 μm thick IGBTs with the low efficiency p+ emitter had excellent trade off relation and exhibited the fast switching speed and the low on-state voltage drop.

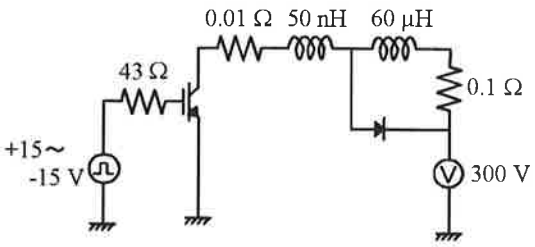


Fig. 5 Circuit for turn-off simulation and all the parameters in the simulated system

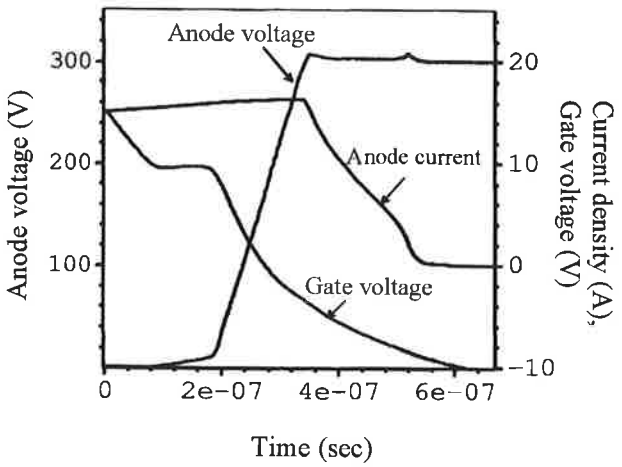


Fig. 6 Simulated 58 μm thick trench gate IGBT turn-off waveforms

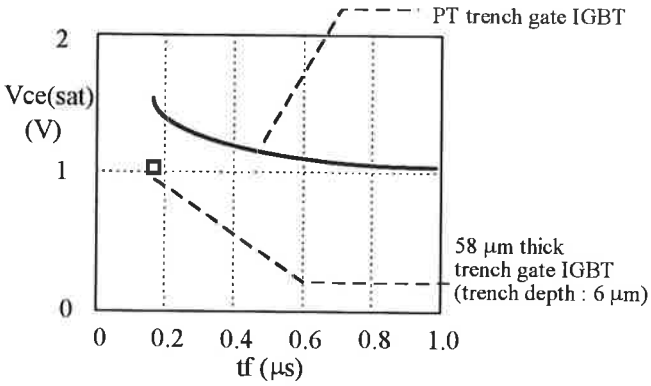


Fig. 7 Trade off between on-state voltage drops and fall time for conventional trench gate IGBTs and 58 μm thick trench gate IGBTs

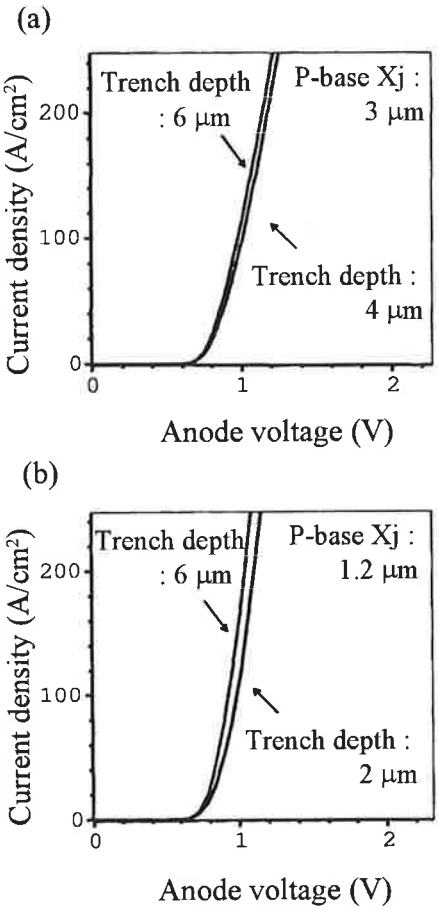


Fig. 8 Simulated current-voltage characteristics for the 58 μm thick substrate with the trench depth of 2 μm and 6 μm

It was found in Fig.8(a) that the current-voltage characteristics of the proposed IGBTs do not depend on the trench gate depth from 4 μm to 6 μm. Figure 8(b) shows also the characteristics of the proposed IGBTs with shallow p-base layer. These results show that simple shallow trench gate structure is sufficient for a lower on-state voltage, resulting in a high fabrication yield. On the other hands, if epitaxial wafers and electron irradiation are adopted, the on-state voltage drop strongly depends on the trench gate depth. This is because stored carrier density under the gate is not sufficient for shallow trench gate to inject sufficient electrons.

The forward blocking voltage of 600 V was numerically confirmed, as seen in Fig.9. The thickness of the n-drift layer is 50 μm. When the 600 V positive voltage is applied to the cathode layer, the depletion layer reaches to the n-buffer layer. It is effective that the proposed IGBT with 58 μm thick substrate wafer has the n-buffer layer to obtain the high breakdown voltage more than 600 V.

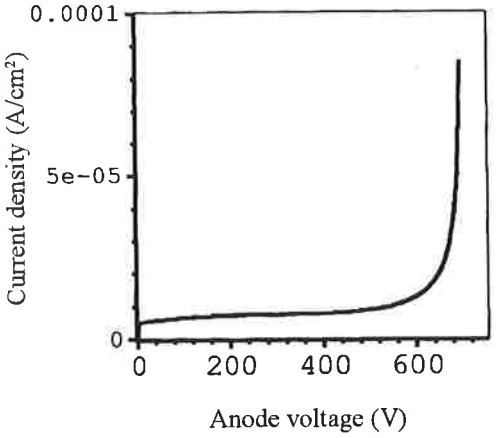


Fig. 9 Simulated breakdown characteristic with the trench depth of 6 μm combined with low efficiency p+ emitter

CONCLUSION

The present paper has analyzed the capability of trench gate IGBT. It should be noted that the completely scaled down IGBT cells are not necessarily required to achieve low on-state voltage. Namely, in practical design, high density trench gates are not the requisite. Furthermore, the deep trench gates are not necessary. Important point is to adopt the very thin substrate wafer with a low dose n-buffer layer and transparent p+ emitter. It was found that the proposed 58 μm thick IGBTs with the low efficiency p+ emitter had excellent trade off relation and exhibited the fast switching speed and the low on-state voltage drop.

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