Improvement in Lateral IGBT Design for 500V 3A One Chip Inverter ICs

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Abstract- **This paper reports, for the first time, the development of 500V 3A one chip inverter ICs. The chip size of the IC is 7.1 x 5.2 mm^2, which is only 30% larger than that of 500A 1 A inverter ICs. The chip size reduction has been realized by 35% improvement in lateral IGBT on-resistance and an optimized layout of LIGBT unit cells and bonding pads.**

1. Introduction

Large capacity one chip inverter ICs are demanded for home use appliances, because inverter systems have already been widely accepted and the inverter ICs can reduce the system size and increase its reliability. 250V or 500V blocking voltage is required to directly control DC motors by 100V or 200V AC line source. 250V 1A and 500V 1A three phase one chip inverter ICs were already developed [1,2]. Although their capacity is sufficient for fan motors, larger current capacity is required for compressor motors.

This paper reports, for the first time, the development of 500V 3A one chip inverter ICs for compressor motor control.

2. 500V 3A Lateral IGBT and Diodes

As the cost is the first priority for consumer application, great efforts were made to reduce the chip size of the developed inverter IC chip. The chip size of the IC is 7.1 x 5.2 mm^2, which is only 30% larger than that of 500A 1A inverter ICs. The chip size reduction has been realized by 35% improvement in lateral IGBT on-resistance and an optimized layout of lateral IGBT unit cells and bonding pads.

The lateral IGBT on-resistance has been improved by adopting (1) finer multi-channel design using i-line stepper, (2) reduced JFET effects by phosphorous implant under the poly-silicon gate and (3) thicker aluminum interconnection layers.

Figure 1 shows the cross section of the improved multi-channel LIGBTs. Shallow n-type implant layers are formed under the poly-silicon gate to reduce JFET resistance without introducing any additional process step by using the same channel implant as that used for PMOS threshold voltage control. Thus, the formed n-type layer under the gate actually consists of a buried n-layer with a very thin boron surface layer.

The p-well size is reduced from 8μm down to 5μm by adopting 0.5μm fine alignment tolerance as shown in Fig.2. The drain (collector) p+ emitter size was also reduced to 16μm. This resulted in very small curvature of n-buffer at its end, as seen in Fig.3. Special care was taken to achieve 520V breakdown voltage with the small n-buffer curvature. The final unit LIGBT cell size was reduced to 140μm, which is 87% of the conventional multi-channel LIGBTs[3], as shown in Fig.3.

Figure 4 compares I-V curves of new multi-channel LIGBT and conventional multi-channel LIGBTs. A large current capability of 175A/cm^2 current density was realized in the new LIGBTs for 3.0V forward voltage and 300nsec fall-time, which is 35% improvement, compared with that of conventional multi-channel LIGBTs, as illustrated in Fig.5. Forward voltage drop is 3.2V for 3.0 amperes of the drain current.

Figure 6 shows switching waveforms of 3.0A drain current. The switching-off time is 300nsec., which enables 20kHz operation.

Shortcircuit withstanding capability of the developed LIGBTs was maintained although its on-resistance was decreased. Figure 7 shows that the new

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LIGBT withstands load short-circuit current of 8A for 8μsec at room temperature. Shortcircuit capability was increased by optimizing the shallow p^+/p^- anode emitter structure and their boron doses as well as the fine source layer structure.

The diode electrical characteristics are also important to reduce chip size. Reverse recovery switching loss and maximum current capability determines the size of the diodes. Figure 8 shows the reverse recovery waveforms of the diodes, turning off 5A of current with di/dt of 30A/μsec at 100°C. The reverse recovery time was 300nsec.

3. 500V 3A Inverter IC Chip

Two metal interconnection layers were adopted. The thickness of the second aluminum layer was 4μm. Figure 9 shows top view of a 500V 3A inverter IC and six lateral IGBTs and diodes. It is clearly noticed that bonding pads are placed in the widest portion of the metal interconnection layers, which changes its width as it goes apart from the bonding pads. The locations of bonding pads and the layout of LIGBT unit cells are optimized so that total LIGBT area consumption and its on-resistance are minimized.

The forward voltage of the final LIGBTs is 3.0V for 3.0A drain current since the final channel design was further improved, compared with the LIGBT TEG design, described in Section 2.

4. Circuits and dV/dt malfunction

A protection circuit called RTC (Real Time Control) was installed to further increase the reliability. The gate voltage was successfully controlled below a low value and the drain current was suppressed when the RTC protection circuit detected a large current exceeding 5A. Figure 10 shows short-circuit waverforms. The drain current was suppressed below 5A at 125°C

It was found that the dV/dt current, caused by the low side IGBT turn-off, flows through the buried oxide and may cause malfunction of the high side driver circuits. Figures 11(a) and (b) shows how the dV/dt current flows, for example, in trench isolated islands with a p-well. If the n-type island layer is floating, an inversion layer is immediately created on the buried oxide by injected holes from the p-well. If the n-type island is electrically connected to the high voltage line, a depletion layer is initially created. After the depletion layer reaches the p-well, holes are injected and an inversion layer is created.

The management of the dV/dt current is an important issue in high voltage SOI circuits.

5. Conclusion

This paper reports the development of 500V 3A one chip inverter ICs. Current capacity of 500V inverter IC chip was successfully increased by the improvement in multi-channel LIGBT characteristics with increased cost performance.

References

[1]N.Sakurai et al., Proc. of ISPSD'90, p.66
[2]A.Nakagawa et al., Proc. of ISPSD'92,p.328
[3]H. Funaki et al.,Proc. of ISPSD'97, p.33

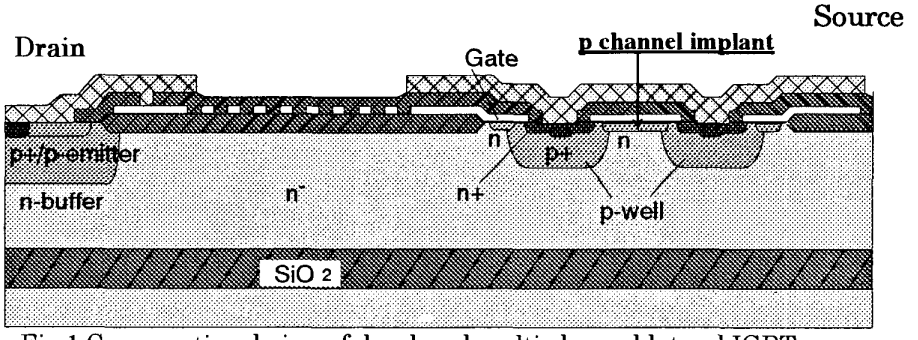


Fig.1 Cross sectional view of developed multi-channel lateral IGBT p-channel implant layer is introduced under the gate oxide.

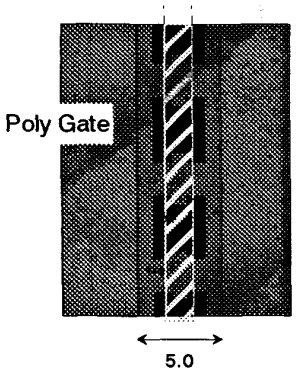


Fig.2 Fine p-well and source structure

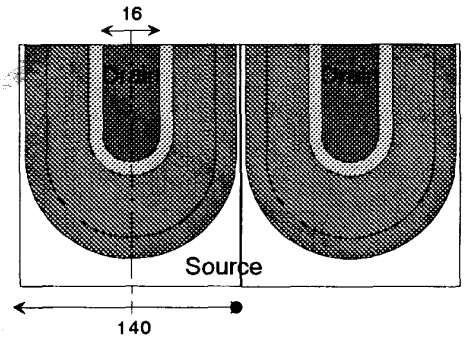
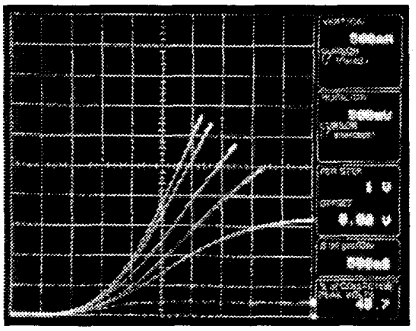
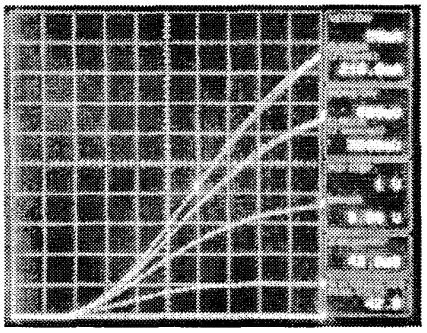


Fig.3 Top view of two unit LIGBT cells



(a) New Multi-chanel IGBT
Vf=3.0V for Drain current of 2.6A
(Vg=5.0V) Device area:1.48mm^2
Vertical axis: 0.5A/Div Horizontal axis: 0.5V/Div



(b) Conventional Multi-chanel IGBT
Vf=3V for Drain current of 215mA
(Vg=5.0V) Device area: 0.165mm^2
Vertical axis: 50mA/Div Horizontal axis: 0.5V/Div

Fig.4 Comparison of new and conventional LIGBT I-V curves. Note that two device areas are different from each other.

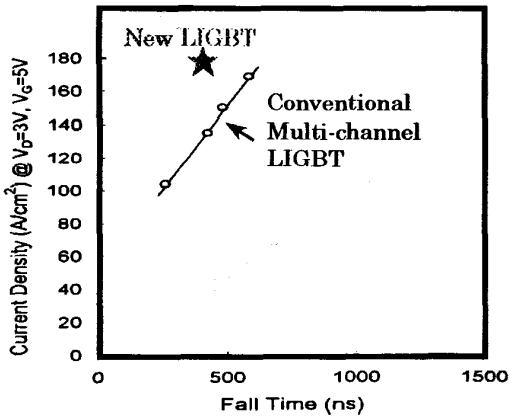
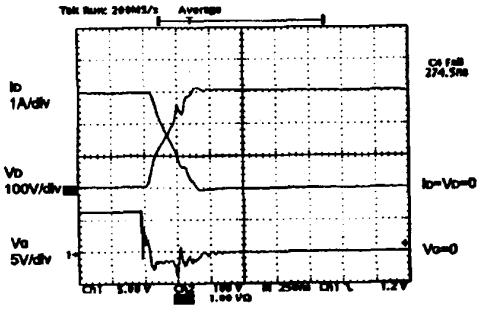
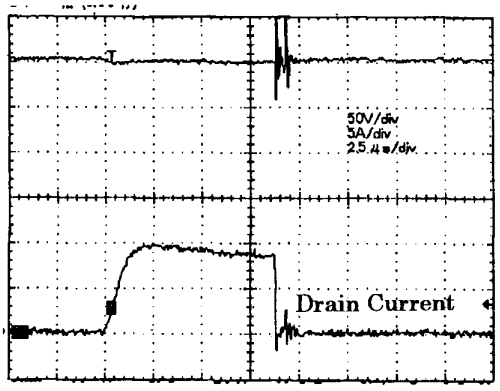


Fig.5 Comparison in trade-off relation between new LIGBTs and conventional multi-channel LIGBTs.



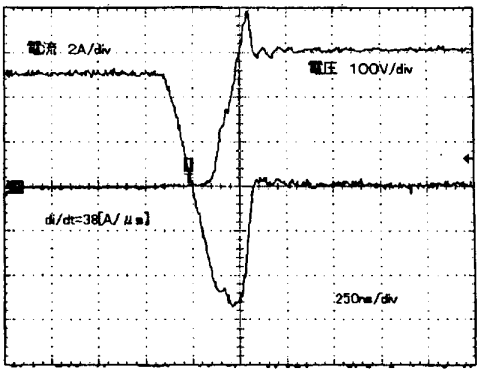
Time: 200nsec/Div
Drain current: 1A/Div

Fig.6 Three ampere switching waveforms of 500V 3A LIGBTs



Drain current: 5A/Div, Time:2.5μsec/Div

Fig.7 Shortcircuit withtanding waveforms of LIGBT TEG at 25°C. Applied drain voltage is 300V.



Drain current: 2A/Div, Voltage:100V/Div
Time:250nsec/Div

Fig.8 Diode reverse recovery waveformes at 100°C.

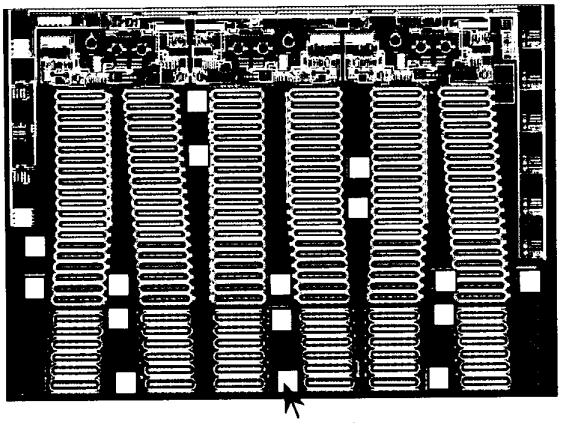
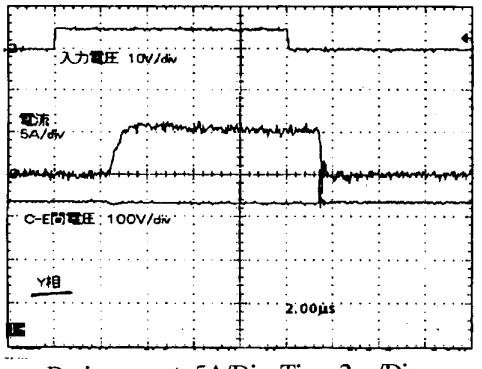


Fig.9 Top view of 500V 3A inverter IC Chip



Drain current: 5A/Div, Time:2μs/Div

Fig.10 Short circuit waveforms at 125°C with RTC circuit

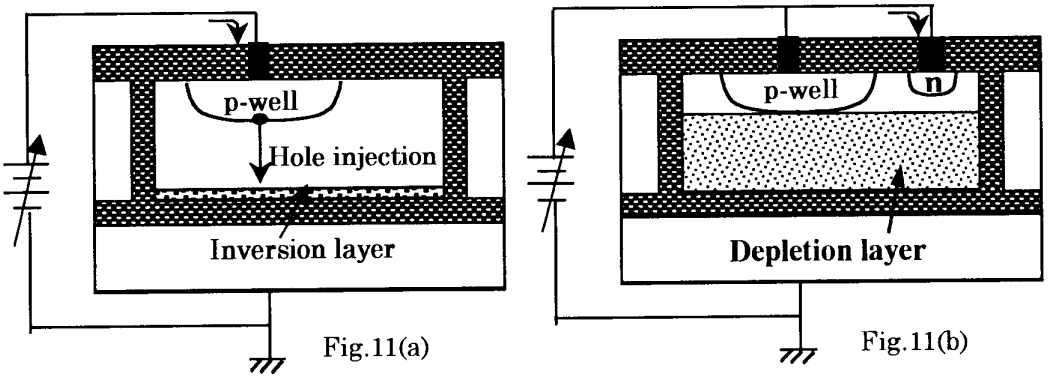


Fig.11 dV/dt current flowing mechanism in a trench isolated island.