20 V LDMOS Optimized for High Drain Current Condition Which is better, n-epi or p-epi?

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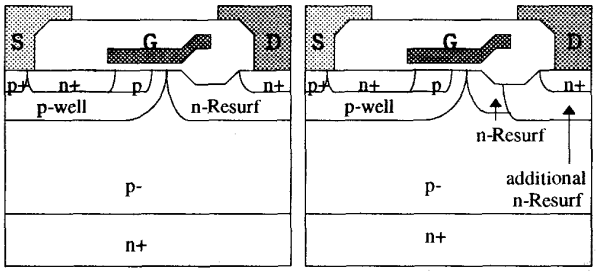
***Abstract*–This paper discusses which is better for 20 V range LDMOS, n-epi or p-epi substrate. We present four optimized 20 V LDMOSFETs and compare them. The best compromise is the LDMOS on n-epi with a high dose n-implant layer which achieves a sufficiently low on-resistance of 17.2 mΩ·mm^2 and a high static breakdown voltage of 24.0 V without breakdown voltage degradation under large drain current flow conditions. The device on-state breakdown voltage for a 5 V gate voltage is 24.5 V.**

I. INTRODUCTION

Many studies on low on-resistance 20 V range power MOSFETs have been conducted, reflecting the fact that these devices have various applications in computer peripherals. It was recently reported that a 25 V LDMOS achieved a specific on-resistance as low as 28 mΩ·mm^2 [1]. However, one drawback of conventional Resurf LDMOS, shown in Fig. 1(a), is that the breakdown voltage degrades as the drain current increases, and the I-V curves show snapback characteristics (Fig. 2(a)). The snapback characteristics in bipolar transistors are well observed as "second breakdown" [2].

The authors have proposed the mechanism of the breakdown voltage degradation and have proposed a new 20 V Resurf MOSFET on p-epi/n+ substrate, named "adaptive Resurf LDMOS", which uses 2-step Resurf layers (Fig. 1(b)) [3].

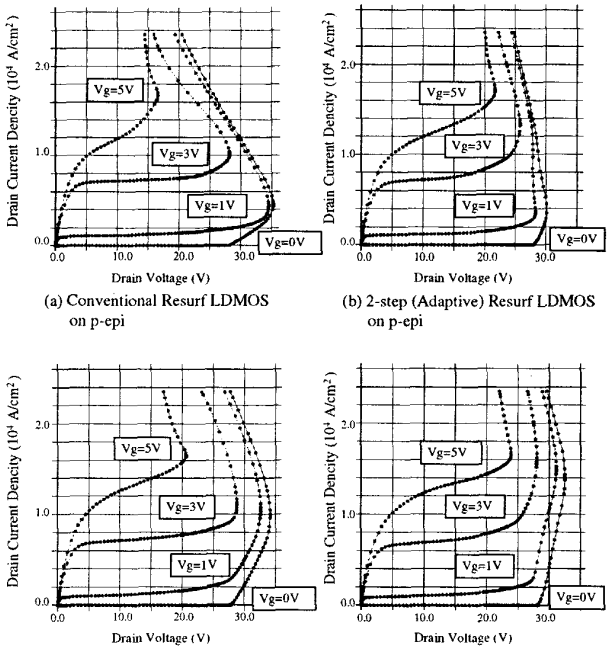
However, there still remain controversial issues: whether p-type or n-type epi/substrate should be chosen and/or whether 2-step Resurf/n-implant layers or more heavily doped single Resurf/n-implant layer should be used to improve on-state (Vg = 5 V) breakdown voltage. In the present paper, we present and compare four optimized 20 V power MOSFETs, based on four different design principles and show how the issues can be resolved.



(a) Conventional Resurf LDMOS on p-epi (b) 2-step (Adaptive) Resurf LDMOS on p-epi

(c) Conventional shallow n-implant LDMOS on n-epi (d) 2-step shallow n-implant LDMOS on n-epi

Fig. 1 Cross-sectional view of (a) conventional Resurf LDMOS on p-epi, (b) 2-step (adaptive) Resurf LDMOS on p-epi [2], (c) conventional shallow n-implant LDMOS on n-epi, and (d) 2-step shallow n-implant LDMOS on n-epi.



(a) Conventional Resurf LDMOS on p-epi (b) 2-step (Adaptive) Resurf LDMOS on p-epi

(c) Conventional shallow n-implant LDMOS on n-epi (d) 2-step shallow n-implant LDMOS on n-epi

Fig. 2 The I-V characteristics of (a) conventional Resurf LDMOS on p-epi, (b) 2-step (adaptive) Resurf LDMOS on p-epi [2], (c) conventional shallow n-implant LDMOS on n-epi, and (d) 2-step shallow n-implant LDMOS on n-epi.

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II. Device Structures

We carried out a thorough series of design optimization works, using a device simulator DESSIS-ISE. Calculations were carried out for the following boundaries. The thickness of the p-epi or n-epi layers is 5 μm. The gate oxide thickness is 15 nm. The physical cell pitch is 4.25 μm. All the other device dimensions were kept the same.

III. Device Simulations

A. *Adaptive Resurf/n-implant LDMOS*

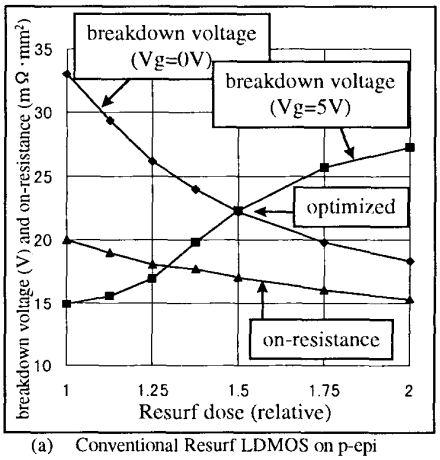
First, two optimized lateral power MOSFETs are shown; 2-step adaptive Resurf layers are adopted for one (Fig. 1(b)), and 2-step shallow n-implant layers for the other (Fig. 1(d)). Figure 2 shows the calculated I-V curves for the two devices, both of which have static breakdown voltage of around 28 V. Conventional two devices on p-epi and n-epi are also shown. The adaptive Resurf LDMOS on p-epi achieved a specific on-resistance as low as 17.7 $m\Omega \cdot mm^2$ and a high on-state breakdown voltage of 21.8 V [3]. The concept of "two step n-implant layers" is the same as "adaptive Resurf" in LDMOS on p-epi, and effectively increases on-state breakdown voltage in LDMOS on n-epi without decreasing static breakdown voltage and increasing on-resistance. The device on-state breakdown voltage of "2-step n-implant" LDMOS on n-epi is 23.8 V and the on-resistance is 18.7 $m\Omega \cdot mm^2$.

Although these two devices have good characteristics, the number of process steps is increased due to the additional Resurf/n-implant layer.

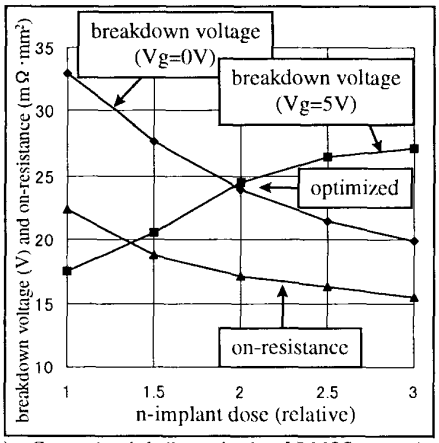
B. *High dose Resurf/n-implant LDMOS*

Next, we adopted a different design principle, namely the impurity dose in the Resurf or shallow n-implant layer is simply increased in order to increase on-state breakdown voltage. It is possible to increase on-state breakdown voltage by this method. However, the static breakdown voltage simply degrades as the impurity dose in the Resurf/n-implant layer increases [3]. Figure 3 shows how static and on-state breakdown voltages change as the implant dose increases for each MOSFET on p-epi and n-epi. Comparing the two figures, there is a tendency that, for Resurf LDMOS on p-epi, it is more difficult to realize a higher on-state breakdown voltage for 5V gate voltage without sacrificing static breakdown voltage as compared with LDMOS on n-epi.

Figure 4 shows the dependence of on-state breakdown voltage and on-resistance on static breakdown voltage, where the Resurf/n-implant layer dose is the parameter. In these figures, A and B denotes the impurity concentrations of p-epi or n-epi substrate, where A is higher than B. In Resurf LDMOS on p-epi, the characteristics are not so depending on the impurity concentrations of p-epi substrate. On the other hand, in n-implant LDMOS on n-epi, the impurity concentrations of n-epi substrate have a great influence on the on-state breakdown voltage. As the impurity concentrations of n-epi substrate is lower, the characteristics of the n-implant LDMOS on n-epi are close to those of the Resurf LDMOS on p-epi. Conversely, as the impurity concentrations of the n-epi substrate is higher, the on-state breakdown voltage is increased, but the static breakdown voltage is decreased. There exists a trade-off relationship between the static breakdown voltage and the on-state breakdown voltage about the impurity concentrations of n-epi substrate. The LDMOS on n-epi with single high dose n-type implant layer is superior to the counterpart Resurf devices on p-epi, because it achieves higher



(a) Conventional Resurf LDMOS on p-epi



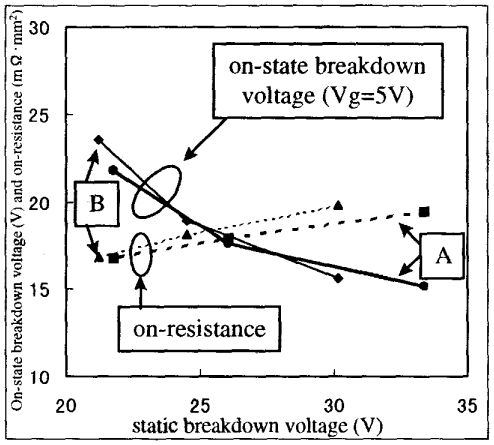
(b) Conventional shallow n-implant LDMOS on n-epi

Fig. 3 Static and on-state breakdown voltages and on-resistance versus n-type implant layer dose of (a) Resurf LDMOS on p-epi, (b) shallow n-implant LDMOS on n-epi.

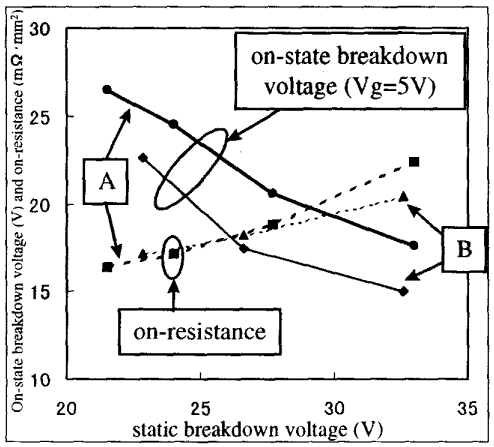
on-state breakdown voltages and a low on-resistance with static breakdown voltage equivalent to the counterpart device. Figure 5 shows the calculated I-V curves for an optimized LDMOS on n-epi adopting the single n-type high dose implant layer. The static and on-state breakdown voltage are both the same as 24.0 V and the on-resistance is 17.2 $m\Omega \cdot mm^2$.

Ⅳ. Analysis

In conventional Resurf devices in p-epi, the Resurf layer is designed so that the static breakdown voltage take the maximum value. The breakdown voltage simply decreases as the drain current density increases because electrons flowing in the Resurf layer neutralize the ionized impurities. In contrast, the n-implant LDMOS in n-epi is not designed to have a maximum breakdown voltage. The device breakdown voltage decreases as the n-implant layer dose increases.



(a) Resurf LDMOS on p-epi



(b) n-implant LDMOS on n-epi

Fig. 4 On-state breakdown voltage and on-resistance versus static breakdown voltage of (a) Resurf LDMOS on p-epi, and (b) shallow n-implant LDMOS on n-epi. A and B denote the impurity concentrations of p-epi or n-epi substrate, where A is higher than B.

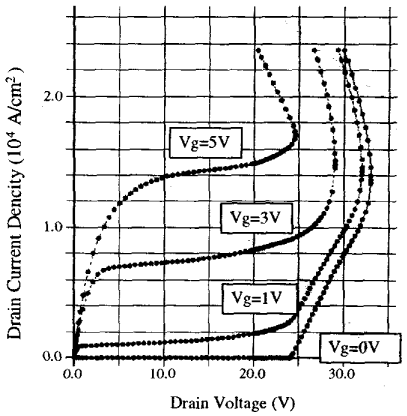


Fig. 5 Calculated I-V characteristics for the shallow n-implant LDMOS on n-epi adopting the high dose single n-implant layer.

As the drain current increases, n-implant layer positive charge is partially compensated by the flowing electron charges as seen in Fig. 6. In Resurf LDMOS on p-epi, the electron current path is restricted by the Resurf layer. On the other hand, in n-implant LDMOS on n-epi, the electron current path is not restricted by the n-implant layer and the negative space charge region reaches the n-epi substrate.

Figure 7 shows the doping concentration and electron density distribution of Resurf/n-implant LDMOS on p-epi/n-epi under the center of the LOCOS. The electron density under a large drain current flow condition has a peak value near the surface. The maximum electron density of Resurf LDMOS on p-epi is far greater than the doping concentration because of the restriction of current path. This is why on-state breakdown voltage of LDMOS in p-epi is lower than in case of the counterpart devices.

Ⅴ. Discussions & Conclusion

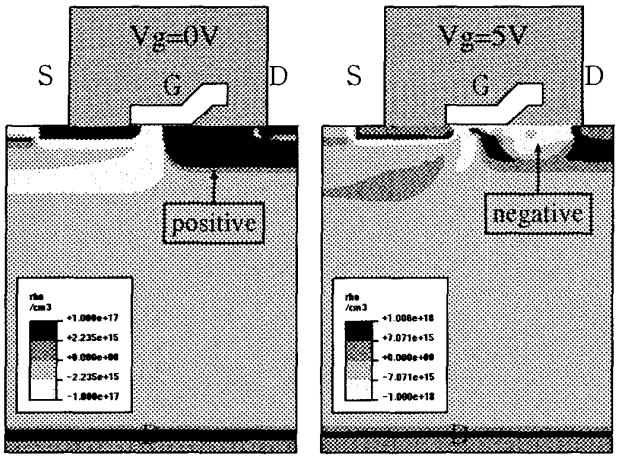
We have presented four optimized 20 V range LDMOSFETs, all of which achieve a sufficiently low on-resistance and a high static breakdown voltage without breakdown voltage degradation under large drain current flow conditions. Table I compares the two conventional devices and the four optimized LDMOSFETs. In terms of the static and on-state breakdown voltages, two step n-implant layer LDMOS on n-epi is the best, but the on-resistance is higher than for the two step Resurf LDMOS on p-epi. On the other hand, the optimized LDMOS on n-epi with single high dose n-type implant layer is superior to the counterpart Resurf devices on p-epi, because it achieves higher static and on-state breakdown voltages with a low on-resistance equivalent to those of the counterpart device. Regarding the process step, the best compromise is the LDMOS with high dose n-implant layer in n-epi.

Table I

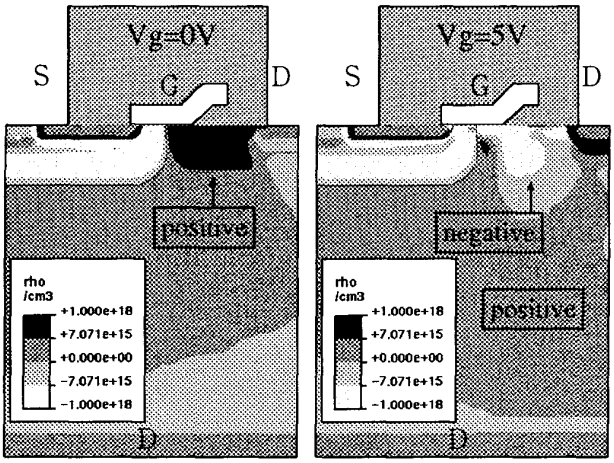
BREAKDOWN VOLTAGE AND ON-RESISTANCE OF THE DEVICES

The LDMOS on p-epi achieves low on-resistance, but low on-state breakdown voltage. The LDMOS on n-epi achieves high on-state breakdown voltage, but high on-resistance. The high dose shallow n-implant LDMOS on n-epi achieves low on-resistance without breakdown voltage degradation due to large current flow.

Optimization	Device Type	Substrate Type	Breakdown Voltage (V)		On-resistance ($m\Omega \cdot mm^2$)
			$V_g = 0$ V	$V_g = 5$ V	
Conventional	Conventional Resurf LDMOS	p-epi	28.1	16.6	18.9
Conventional	Conventional shallow n-implant LDMOS	n-epi	27.7	20.6	18.8
Optimized	2-step (Adaptive) Resurf LDMOS	p-epi	28.0	21.8	17.7
Optimized	2-step shallow n-implant LDMOS	n-epi	28.0	23.5	18.7
Optimized	High dose Resurf LDMOS	p-epi	22.2	22.3	17.1
Optimized	High dose shallow n-implant LDMOS	n-epi	24.0	24.5	17.2



(a) Resurf LDMOS on p-epi



(b) n-implant LDMOS on n-epi

Fig. 6 Space charge distribution of (a) Resurf LDMOS on p-epi, (b) shallow n-implant LDMOS on n-epi when the breakdown occurs at Vg = 0 V, 5 V. In these figures, the black region means that net charge is positive and the white region means that net charge is negative. The positive space charge in the Resurf/n-implant layer is compensated by the negative charge of the drain current. This initially increases on-state breakdown voltage in LDMOS.

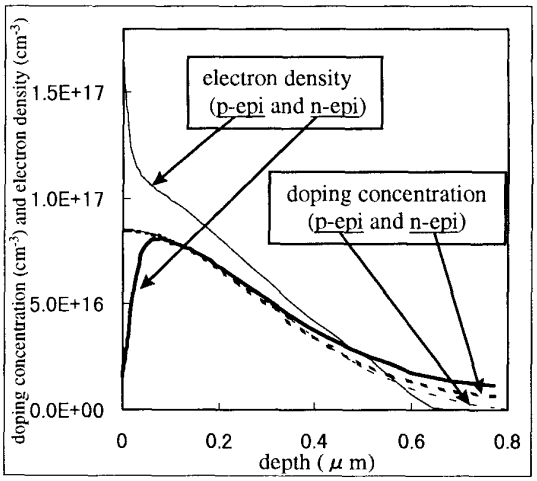


Fig. 7 Doping concentration and electron density of Resurf/n-implant LDMOS on p-epi/n-epi at Vg = 5 V, Vd = 15 V. The doping profile of Resurf and n-implant layers are almost the same.

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