Predicted Electrical Characteristics of 4500 V Super Multi-Resurf MOSFETs

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Abstract-**In this paper, We show the optimized device parameters for various voltage multi-resurf device based on exact simulation. In addition, we also present, for the first time, the exact static and transient simulation of a 4500 V multi-resurf device. The distinguished feature for the multi-resurf MOSFET is that there exist a storage time and that the fall time is extremely small. Multi-resurf MOSFET was found to be ideal device for high voltage applications, superior to IGBT.**

I. Introduction

Recently, novel devices called as "Cool MOS"[1, 2] and "Superjunction" devices[3, 4] have been presented. These devices are characterized by stripe p and n column layers (shown in fig. 1), which are designed under the "multi-resurf" concept or "extended resurf principle"[5]. Previous studies experimentally and analytically showed that these devices can significantly reduce their on-resistance by paralleling a number of low resistance thin column layers in a unit device area. However, there has been no report which discuss the dynamic phenomena inside the multi-resurf device. In this paper, we present, for the first time, the exact static and transient simulation of a 4500V multi-resurf device. It was found that the simulated characteristics of multi-resurf MOSFET are superior to that of IGBT. The distinguished feature for the multi-resurf MOSFET is that there exists a storage time and the fall time is extremely small. This is because all of the carriers are removed in the storage time period and the multi-resurf device turns into insulator. We show the optimized device parameters for various voltage multi-resurf device based on exact simulations. We further show that stripe column layers thinner than 0.05μm don't significantly contribute to the reduction in device on-resistance, anymore, which contradicts the results of Ref.[3].

II. Device Structures and Calculation Results

A. Breakdown Voltage and On-Resistance

Figure 1 shows schematic view of multi-resurf diode which is used for calculation of breakdown voltage and on-resistance. Optimization parameters are the device length (L), the p and n layer thickness (W), and the p and n layer impurity concentration (C_p and C_n). Figure 2 shows the dependence of breakdown voltage on p and n column layer impurity concentration for the case of L = 15 μm, W = 0.5 μm and $C_p = C_n$. It was found that breakdown voltage decreased abruptly when the impurity dose was more than 1.0e17 cm^{-2}. This is because the breakdown occurred before the p and n layer was completely depleted. These calculations were carried out for each device length and p and n column layer thickness. On-resistance was calculated for the p and n layer impurity dose just before breakdown voltage began to decrease.

Figure 3 shows calculated on-resistance vs. breakdown voltage as a function of p and n column layer thickness. The device on-resistance reduces significantly as the p and n column layers become thinner. However, contrast to the results of Ref.[3], the on-resistance for W = 0.05 μm is almost the same as the value for W = 0.5 μm. This is because the p and n layers of the devices for W = 0.05 μm are already depleted by the junction built-in potential as shown in Fig. 4. It is shown that the amount of the carrier (electron) is only about one fifth of that of the impurity. If the impurity concentration is increased in order to compensate the depleted carriers, leakage current caused by band to band tunneling abruptly increases.

B. 4500 V Multi-Resurf MOSFET

Figure 5 shows the cross-section of calculated 4500 V multi-resurf MOSFET. The p and n column thicknesses are chosen as 7 μm, which is practical from fabrication viewpoint. The breakdown voltage is 4950V. Calculated turn-off waveforms are shown in Fig. 6 and 7. The most notable feature of the waveforms is that there exists a storage time of 1.5 μsec, and voltage recovering process is extremely short. During the storage time, carriers in the p

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and n column layers are being depleted. Figure 8 shows the carrier density distributions at the time steps of 0, 1.05e–6 and 1.5e–6 sec, which describe the carrier removing process in n and p column layers. Applied drain (or collector) voltage is only 30 V when the p and n layers is completely depleted and the storage time finishes. After the storage time, the drain current decreases abruptly in 10 nsec. Figure 7 shows the magnified turn-off waveforms. It was found that the fall time is extremely small because all of the carriers have already been removed and the whole multi-resurf columns are completely depleted in the storage time. This is quite distinguished feature for the super multi-resurf devices. For all of the conventional devices, depletion layer develops in the high resistance drift layer as the applied voltage increases.

Calculated V-I characteristics are shown in Fig. 9. The calculated on-resistance value is 132 $m\Omega \cdot cm^2$, and the forward voltage drop at 30 A/cm^2 is 3.9 V.

Figure 10 shows the dependence of breakdown voltage on p column layer concentration (C_p) for the same structure shown in fig. 5 while C_p is kept constant. The breakdown voltage strongly depends on p column layer concentration, and acceptable error range is about ± 3e13 cm^{-3}. This acceptable concentration error corresponds to the concentration of n-drift layer of conventional 4500V devices.. This result indicates that precise column layer concentration control within an error of 1% is required for fabrication of 4500 V range multi-resurf MOSFET.

Table I shows the comparison of multi-resurf MOSFET and IGBT. Although the forward voltage drop value at 30A/cm^2 is comparable, the fall time of multi-resurf MOSFET is about one hundredth of that of IGBTs. According to Fig. 3, on-resistance value will be further lowered when the p and n layer thicknesses is thinner. When both of the p and n layer thicknesses are 0.5 μm, the forward voltage drop will be 0.4V for 30A/cm^2 current density. In addition, for multi-resurf MOSFET, there is no threshold drain voltage like IGBT, and free wheel diode (FWD) is included as body diode. Multi-resurf MOSFET was found to be ideal device for high voltage applications, superior to IGBT.

III. Summary

We presented the optimized device parameters for various voltage multi-resurf device based on exact simulation. We showed that stripe column layer thinner than 0.05 μm does not significantly contribute to the reduction in device on-resistance because the p and n layers of the devices for W = 0.05 μm are already depleted by the junction built-in potential. In addition, we also presented, for the first time, the exact static and transient simulation of a 4500V multi-resurf device. The distinguished feature for the multi-resurf MOSFET is that there exist a storage time and the fall time is extremely small. In 4500 V devices, precise column layer concentration control within an error of 1% is required for fabrication. Multi-resurf MOSFET was found to be ideal device for high voltage applications, superior to IGBT.

Acknowledgement

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TABLE I Comparison of Multi-Resurf Mosfet and Igbt.

The values of multi-resurf MOSFET with 0.5 μm p and n column layer is predicted value from fig. 3. Multi-resurf MOSFET was found to be ideal device for high voltage device, superior to IGBT.

	Multi-resurf MOSFET (W=7μm) Calculated	Multi-resurf MOSFET (W=0.5μm) Predicted	IGBT
Fall time	10nsec	10nsec	~1μsec
Forward voltage drop @30A/cm²	3.9 V	0.4V	~4.5V
Drain voltage threshold	none	none	~0.8V
Free wheel diode	included	included	none

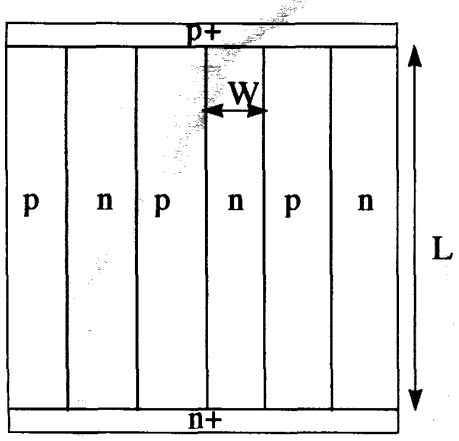


Fig. 1 Schematic view of multi-resurf diode which is used for calculation of Breakdown voltage and On-resistance.

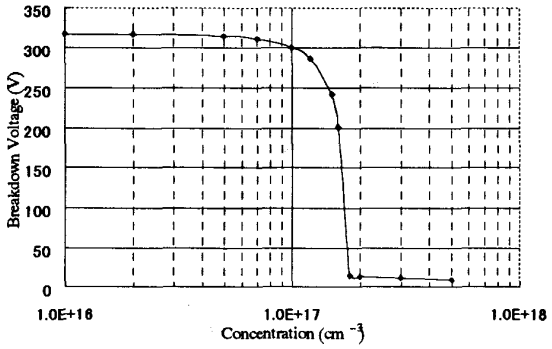


Fig. 2 Dependence of breakdown voltage on p and n layer impurity dose for L = 15 μm, W = 0.5 μm. It was found that breakdown voltage decreased abruptly when the impurity dose was more than 1.0e17 cm^{-2}.

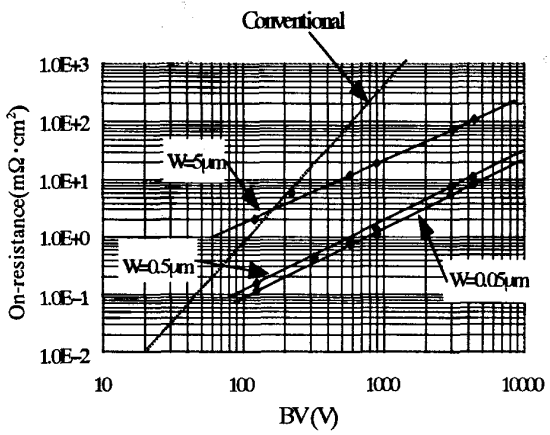
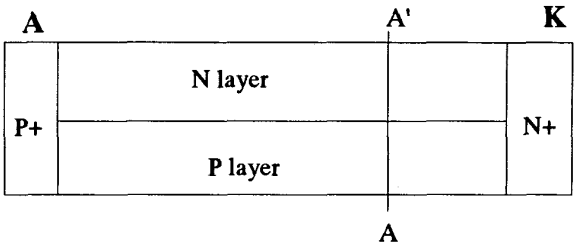
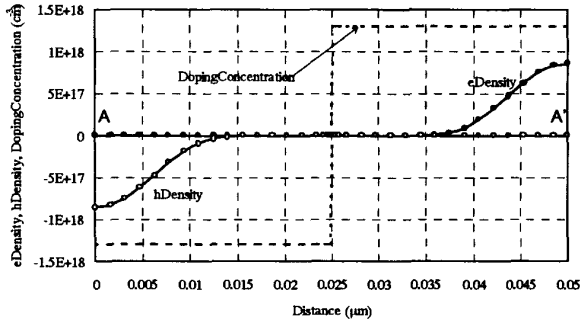


Fig. 3 Dependence of on-resistance on breakdown voltage for each p and n layer thicknesses. Compared with the conventional device, multi-resurf device have the advantage for higher voltage devices.



(a)



(b)

Fig. 4 Relationship of carrier density and doping concentration for the multi-resurf device of W = 0.05 μm. (b) shows the electron and hole density and doping concentration for the cross-section of line A – A' in (a). The n layer near the junction of this device is depleted by the junction built-in potential. This is the reason why the stripe column layer thinner than 0.05μm don't significantly contribute to the reduction in device on-resistance, anymore.

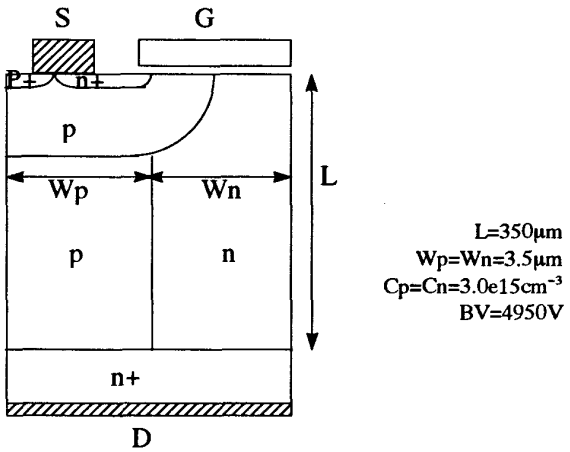


Fig. 5 Cross-sectional view of 4500 V multi-resurf MOSFET.

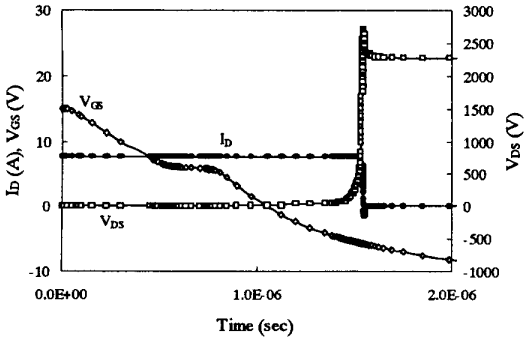


Fig. 6 Calculated turn-off wave forms. After the storage time for 1.5 μsec, the drain current value decreased abruptly.

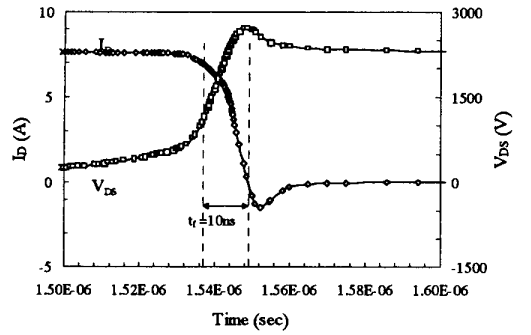
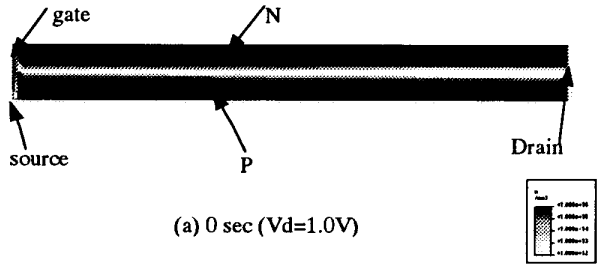


Fig. 7 Magnified turn-off wave forms. It was found that the fall time of this device was only 10 nsec.



(a) 0 sec (Vd=1.0V)

(b) 1.05e-6 sec (Vd=19.2V)

(c) 1.5e-6 sec (Vd=30.1V)

Fig. 8 Carrier density distribution of the time of (a) 0, (b) 1.05e-6 and (c) 1.5e-6 sec in fig. 7, which describe the carrier removing process in n layer.(The white region shows the depletion layer and the shadow portion shows the area where the carrier density is more than 1e15 cm^{-3}) When the drain voltage is only 30V, the p and n layer is completely depleted.

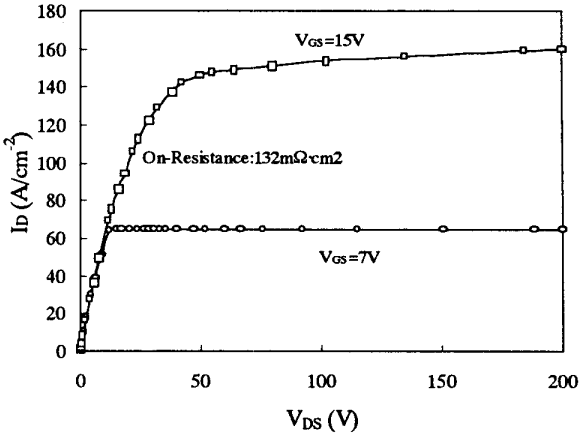


Fig. 9 Calculated V-I characteristics. The calculated on-resistance value was 132 $m\Omega \cdot mm^2$.

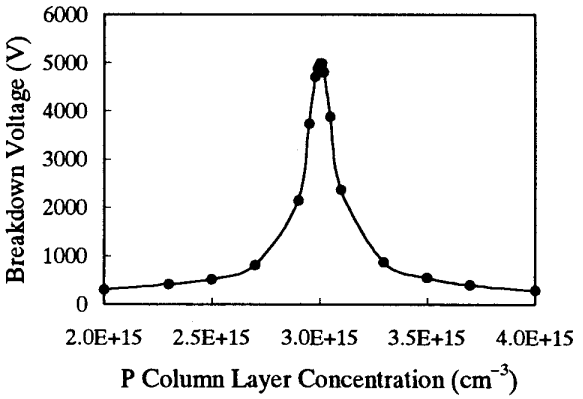


Fig. 10 Dependence of breakdown voltage on p column layer concentration (C_p) for the same structure shown in fig. 5. The breakdown voltage strongly depend on p column layer concentration, and acceptable error range is about ± 3e13 cm^{-3}.