A New Adaptive Resurf Concept for 20 V LDMOS Without Breakdown Voltage Degradation at High Current

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Abstract

This paper presents a new adaptive Resurf concept for 20 V LDMOS which introduces an additional Resurf layer to the conventional Resurf layer. The new Resurf LDMOS achieves a sufficiently low on-resistance of 17.7 $m\Omega \cdot mm^2$ and a high static breakdown voltage of 28.0 V without significant breakdown voltage degradation under large drain current flow conditions. The device on-state breakdown voltage for a 5 V gate voltage is 21.8 V.

Introduction

Many studies of low on-resistance 20 V range MOSFETs have been conducted because these devices have a variety of applications in automotive systems and computer peripherals. It was recently reported that a 25 V Resurf LDMOS achieved a specific on-resistance as low as 30 $m\Omega \cdot mm^2$ [1,2]. However, one drawback of conventional Resurf LDMOS, shown in Fig. 1(a), is that the breakdown voltage is degraded as the drain current increases, and the I-V curves show snapback characteristics which cause destruction of the device. Fig. 2(a) shows a typical I-V curve of a conventional Resurf LDMOS. The device on-state breakdown voltage is degraded.

In the present paper, we propose a new adaptive Resurf concept for 20 V LDMOS, shown in Fig. 1(b), which achieves a sufficiently low on-resistance and a high static breakdown voltage without significant breakdown voltage degradation under large drain current flow conditions.

Device structures and analysis

A. *Conventional structure*

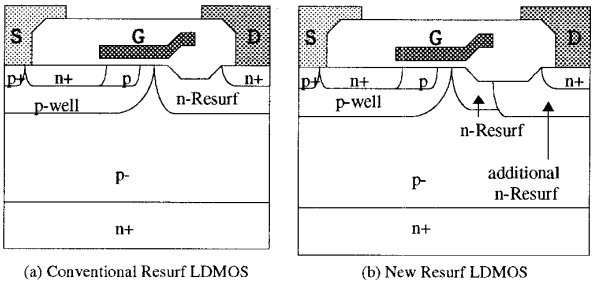
Fig. 1(a) shows a cross-sectional view of a conventional Resurf LDMOS on a p-epi wafer with an n+ buried layer, which is electrically connected to the drain. The Resurf structure is effective in increasing the static breakdown voltage and in reducing the on-resistance. Calculations were carried out for the following conditions : the thickness of the p-epi layer is 5 μm, the impurity concentration of the p-epi layer is 2×10^{15} cm^{-3} and the gate oxide thickness is 15 nm. The physical cell pitch in Fig. 1(a) is 4.0 μm. The optimization parameters for a conventional Resurf LDMOS are the n-Resurf layer impurity dose, length, and depth. Fig. 2(a) shows a typical I-V curve of a conventional Resurf LDMOS with an on-resistance of 15.7 $m\Omega \cdot mm^2$ @ Vg = 5 V and a static breakdown voltage of 30.2 V. The device on-state breakdown voltage for a 5 V gate voltage is only 13.9 V.

The reason why the on-state breakdown voltage is degraded is that the net effective positive charge is reduced by the existence of a large amount of negative electron charges in the Resurf layer due to a large drain current flow. Fig. 3 shows the drain current flow density when the junction breakdown occurs in the optimized conventional Resurf LDMOS for 5 V gate voltage and Fig. 5(a) shows the space charge distribution when the junction breakdown occurs for 0 V and 5 V gate voltages. These figures indicate that the positive space charge of the n-Resurf region is compensated by the negative charge of current flow when the gate voltage is 5 V. Thus, the net positive charge in the depleted Resurf layer of the on-state deviates markedly from the optimized value. The net positive Resurf charge ρ_{net} under a drain current of I_D is expressed by

$$\rho_{net} = \rho_{Resurf\ dose} - I_D / q v_s$$

where $\rho_{Resurf\ dose}$ denotes the original Resurf dose, q the elementary electric charge, and v_s the electron saturation velocity.

Although an LDMOS with an excessively doped single Resurf layer exhibits a high on-state breakdown voltage, the static breakdown voltage is degraded. A high-dose n-Resurf LDMOS, in which the impurity dose of n-Resurf is 148 % of the optimized n-Resurf dose, achieves a high on-state breakdown voltage of 21.3 V at a gate voltage of 5 V, as is seen in



(a) Conventional Resurf LDMOS (b) New Resurf LDMOS

Fig. 1 Cross-sectional view of (a) conventional Resurf LDMOS and (b) new Resurf LDMOS.

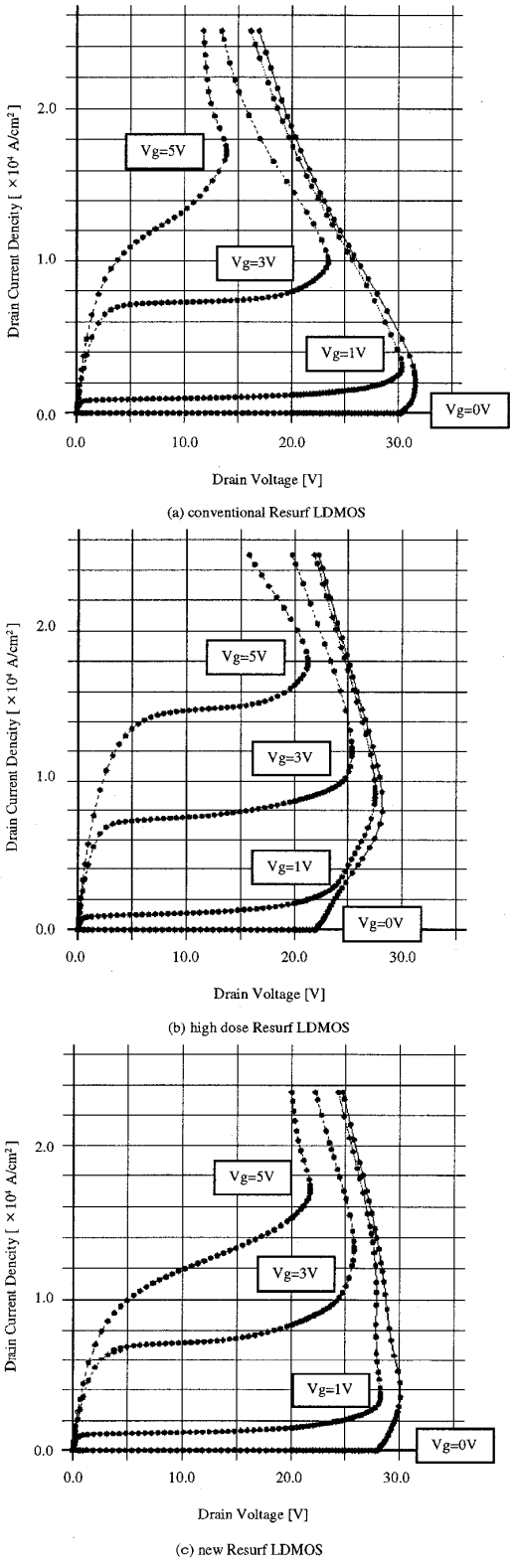


Fig. 2 The I-V characteristics of (a) optimized conventional Resurf LDMOS and (b) high-dose Resurf LDMOS (c) new Resurf LDMOS.

Fig. 2(b). However, the static breakdown voltage is degraded to 22.0 V. Fig. 4 shows the dependence of static and on-state breakdown voltages and on-resistance on the n-Resurf dose. As the n-Resurf dose grows higher, the on-state breakdown voltage increases, but the static breakdown voltage decreases.

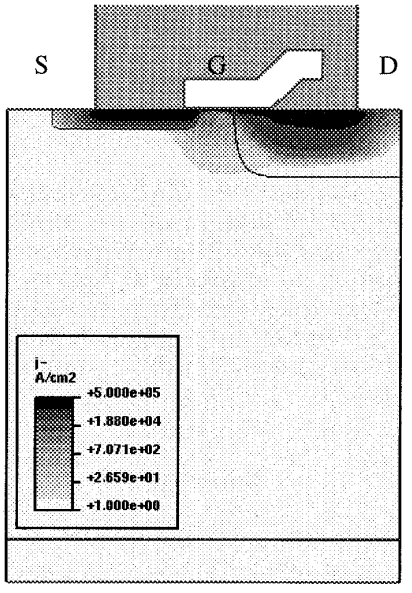


Fig. 3 Drain current density distribution of a conventional Resurf LDMOS when the device breaks down for a 5 V gate voltage. The black region means high current density.

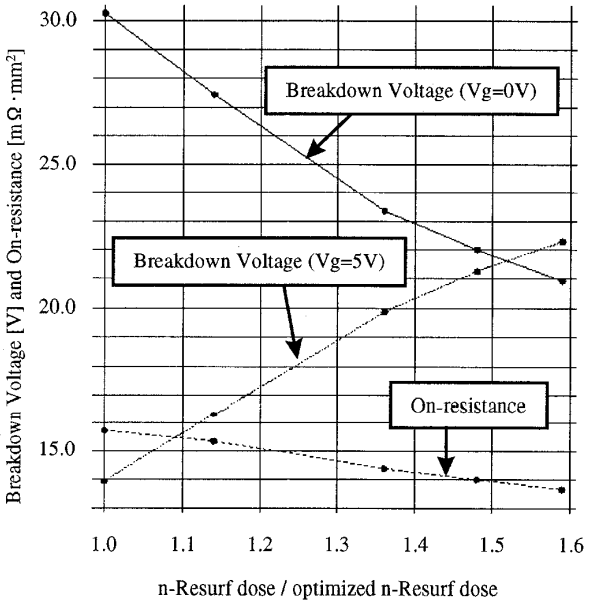


Fig. 4 Static and on-state breakdown voltages and on-resistance versus n-Resurf dose.

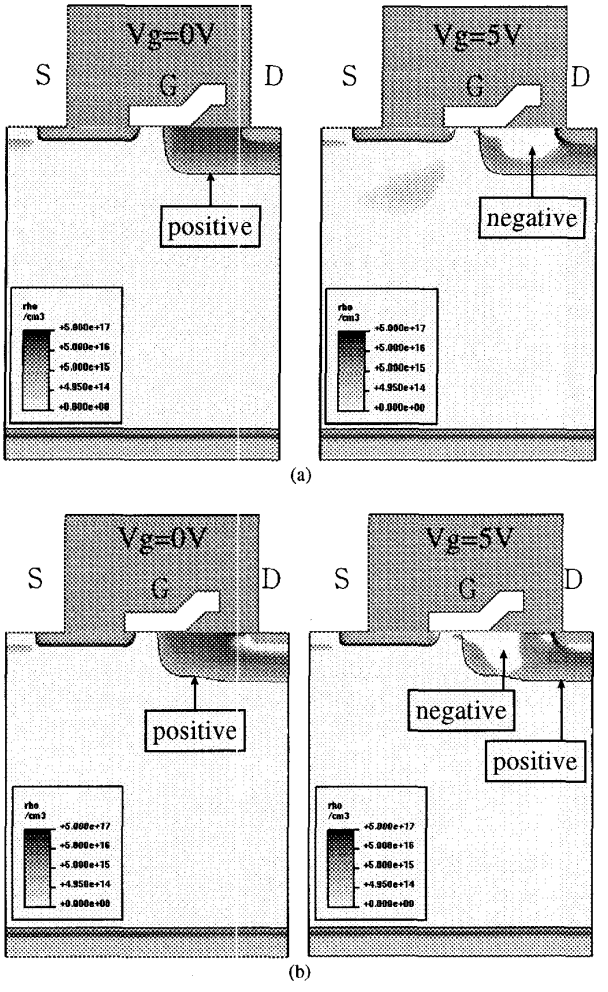


Fig. 5 Space charge distribution of (a) conventional Resurf LDMOS at Vg = 0 V, 5 V and (b) new Resurf LDMOS at Vg = 0 V, 5 V. In these figures, the white region means that net charge is negative and the black region means net charge positive.

One way to obtain a high breakdown voltage in the on-state without a decrease in the static breakdown voltage is to lengthen the n-Resurf. Because its saturation current is limited by the higher resistance of the long n-Resurf, the on-state breakdown voltage is improved. An LDMOS with a 2.0 μm n-Resurf length and a 5.0 μm physical cell pitch achieves a high static breakdown voltage of 32.5 V and a high on-state breakdown voltage of 20.4 V at a gate voltage of 5 V. However, the on-resistance of this device is increased to 31.8 mΩ·mm^2.

B. New device structure

Fig. 1(b) shows the structure of a new 20 V LDMOS on a p-epi wafer with an n+ buried layer. The structure is characterized by the additional n-Resurf layer. The physical cell pitch in Fig. 1(b) is 4.25 μm. The optimization parameters of the new Resurf LDMOS are the n-Resurf layer depth and impurity dose, and the second n-Resurf layer length and impurity dose. In order to add a second n-Resurf layer without degradation of the static breakdown voltage, the optimum value of the first n-Resurf dose of this structure is lower than that of the n-Resurf dose of a conventional device. Because the value of the second n-Resurf dose is typically 2 or 3 times greater than the optimum value of a conventional Resurf layer, the total Resurf layer resistance of the new device can be as low as that of a conventional Resurf LDMOS.

Fig. 6 shows the dependence of static and on-state breakdown voltages and on-resistance on the second n-Resurf dose. As the second n-Resurf dose grows higher, the on-state breakdown voltage increases. The best calculated on-resistance, static breakdown voltage, and on-state breakdown voltage for a 5 V gate voltage are 17.7 mΩ·mm^2, 28.0 V, and 21.8 V, respectively, when the second n-Resurf dose is chosen to be almost the same value as $\rho_{Resurf\ dose} + I_D / qv_s$.

The adaptive Resurf provides the optimum positive Resurf charge in the case of a large drain current flow. Fig. 2(c) shows the calculated I-V curve for the new Resurf LDMOS adopting the optimized 2-step adaptive Resurf layers. The on-state breakdown voltage of 21.8 V is retained at a gate voltage of 5 V. Fig. 5(b) shows the space charge distribution when the breakdown occurs for 0 V and 5 V gate voltages. These figures indicate that the positive space charge of the first n-Resurf region is compensated by the negative charge of current flow when the gate voltage is 5 V, but the positive space charge of the second n-Resurf region remains. This positive space charge region sustains a high on-state breakdown voltage.

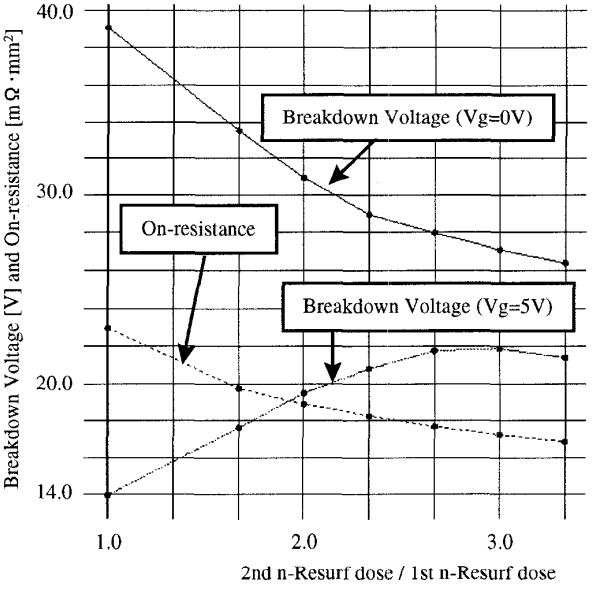


Fig. 6 Dependence of static and on-state breakdown voltages and on-resistance on the second n-Resurf dose.

Fig. 7 shows the breakdown voltage dependence on the gate voltage for the three devices: conventional Resurf LDMOS, high-dose Resurf LDMOS and new Resurf LDMOS. The new Resurf LDMOS achieves high breakdown voltages at each gate voltages.

Conclusion

We have presented a new adaptive Resurf 20 V LDMOS. The proposed device achieves a sufficiently low on-resistance and a high static breakdown voltage without breakdown voltage degradation under large drain current flow conditions. Table 1 compares the breakdown voltage and on-resistance of the three devices. The new Resurf concept achieves a sufficiently low on-resistance without breakdown voltage degradation due to a large drain current flow.

Table 1. Breakdown voltage and on-resistance of the three devices. The new Resurf LDMOS achieves a low on-resistance without breakdown voltage degradation due to a large current flow.

	breakdown voltage [V]		on-resistance [mΩ·mm²]
	$V_g = 0$ V	$V_g = 5$ V	
Conventional Resurf LDMOS	30.2	13.9	15.7
High-dose Resurf LDMOS	22.0	21.3	14.0
New Resurf LDMOS	28.0	21.8	17.7

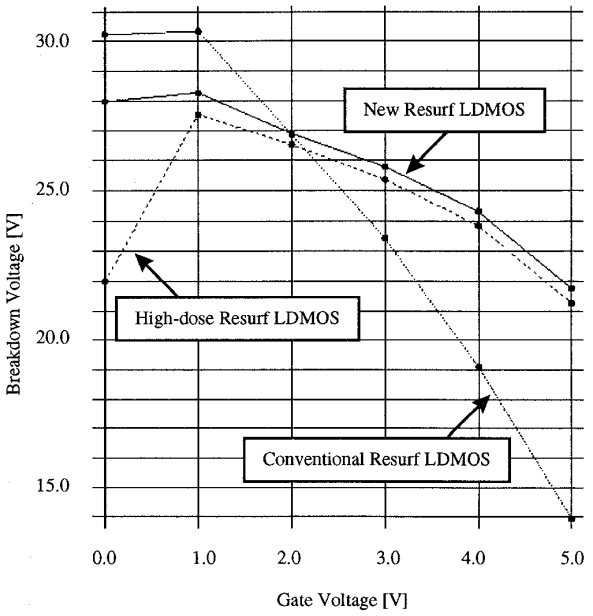


Fig. 7 Breakdown voltage dependence on the gate voltage for the three devices. The new Resurf LDMOS achieves a high breakdown voltage at gate voltages of 0 V and 5 V.

Acknowledgments

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