Lateral SOI Diode Design Optimization for High Ruggedness and Low Temperature Dependence of Reverse Recovery Characteristics

Hideyuki Funaki, Yoshihiro Yamaguchi, Keizo Hirayama, and Akio Nakagawa

Advanced Semiconductor Devices Research Laboratories, Toshiba Corporation
1 Komukai Toshiba-cho Saiwai-ku, Kawasaki 210-8582, Japan,
Tel: +81-44-549-2139, Fax: +81-44-520-1501, E-mail: hideyuki.funaki@toshiba.co.jp

Abstract

The present paper compares, for the first time, the maximum controllable current, or SOA of three different diode structures with low efficiency emitters. Low anode emitter efficiency is achieved either by introducing n^+ diffusions in the p-type anode region (n^+/p^+ diodes), or by adopting low surface concentration anode (p^-/p^+ diodes), or by shallow p diffusion (shallow p/p^+ diodes). It was found that n^+/p^+ diode easily destroyed in the reverse recovery transient at high temperature of 150°C because of a parasitic npn transistor action. The best optimization was found in p^-/p^+ diodes. Shallow p/p^+ diodes exhibited the same ruggedness, if the dose of shallow p layer was optimized.

I. Introduction

High voltage SOI technology has been attracting interest, because high voltage devices can be integrated with control and protection circuits, and even with an MPU at reasonable cost. High voltage high speed lateral SOI diodes are key devices to reduce the total power loss in 1 chip inverter ICs, using lateral IGBTs. Several high speed diode structures have already been proposed [1,2] to improve reverse recovery characteristics by reducing emitter injection efficiency. However, no papers have discussed the ruggedness of the injection efficiency controlled lateral diodes. The present paper compares, for the first time, the maximum controllable current, or Safe Operating Area of three different diode structures with low efficiency emitters.

II. Device Structures and Fabrication

High speed switching can be realized either by reducing carrier lifetime or by reducing emitter injection efficiency. Lifetime control process greatly affects the electrical characteristics of low voltage BiCMOS logic and analog devices. Thus, emitter injection efficiency controlled diodes are desirable, if they

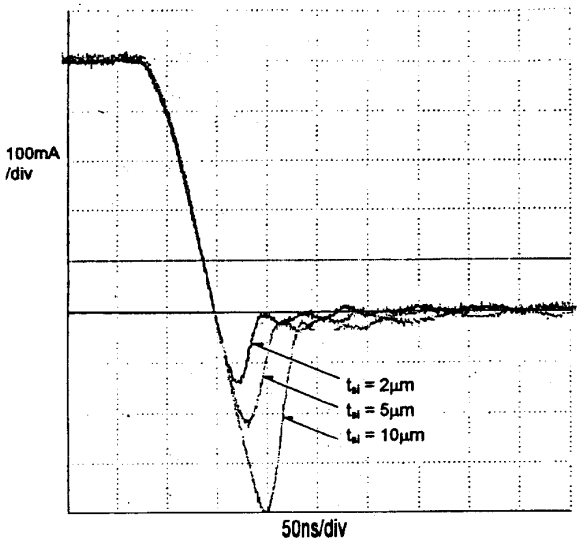


Fig. 1 Reverse recovery waveforms for diodes with three different SOI layer thickness of 2μm, 5μm and 10μm.

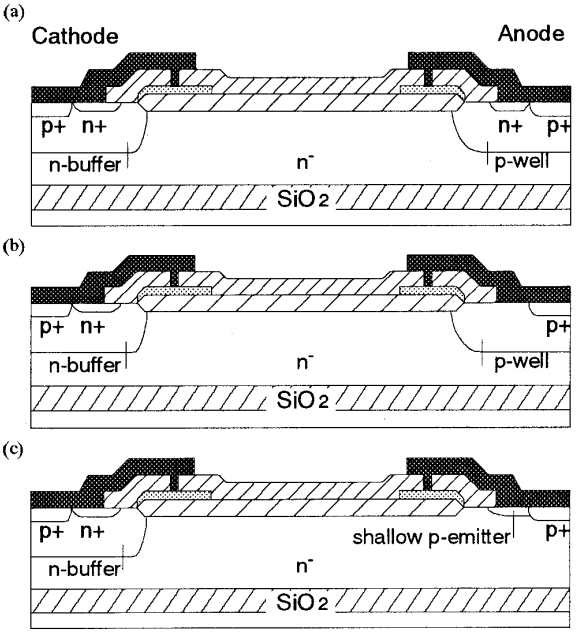


Fig. 2 Cross sectional views of (a) n+/p+, (b) p-/p+ and (c) shallow-p/p+ anode diodes on SOI.

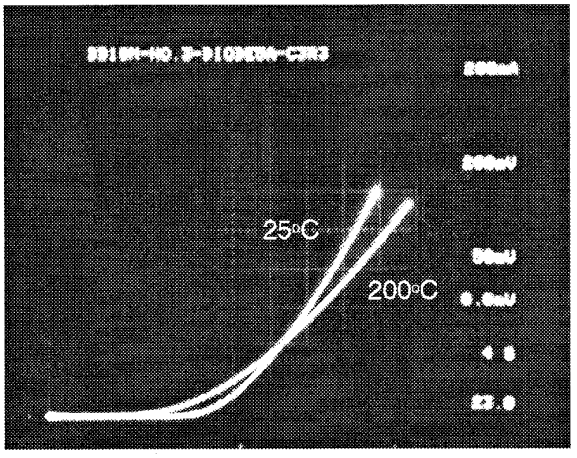


Fig. 3 Experimentally obtained current-voltage curves for the p-/p+ diode at 25°C and 200°C.

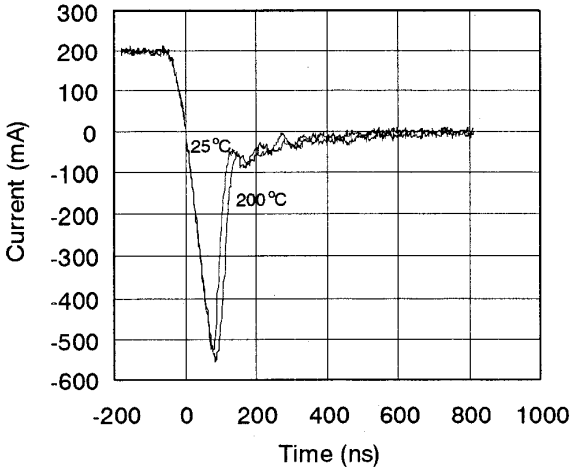


Fig. 4 Measured reverse recovery waveforms for the p-/p+ diode at 25°C and 200°C.

achieve sufficiently good electrical characteristics.

SOI diode switching characteristics are deeply related to SOI layer thickness as well as drift layer length. A high speed diode is automatically realized by simply using relatively thin SOI layer. This is because the total depletion layer volume becomes smaller and the amount of stored charges reduce as the SOI layer becomes thinner.

Figure 1 shows the reverse recovery characteristics of three SOI diodes, fabricated in three different SOI layers with thicknesses of 10μm, 5μm and 2μm. It is seen that the switching speed is greatly improved by reducing SOI layer thickness. Thus, thinnest possible SOI layers should be adopted for power ICs.

The reported diodes in this paper were fabricated on a 15μm thick n-layer (1.0 x 10^{12} cm^{-2} of impurity dose) over 3μm thick buried oxide, and the obtained breakdown voltage was 520V. All diodes have the device length and width of 1mm and 0.25mm, respectively.

Comparisons were made among the diodes, having almost the same forward voltages and reverse recovery characteristics by adjusting the emitter efficiency of the three different emitter structures. Figure 2 shows the cross sections of the three diode structures. Three different methods were used to reduce anode emitter injection efficiency. Figure 2 (a) adopted an additional n^+ diffusion layer and a p^+ ohmic contact diffusion in the p-well (called as n^+/p^+ diode). Figure 2 (b) adopted merged schottky contact and p^+ ohmic contact to the p-well (called as p^-/p^+ diode). Figure 2 (c) adopted merged low dose shallow p-emitter and shallow p^+ emitter (called as shallow p/p^+ diode). The cathode structures with the same low emitter injection efficiency were adopted for all the three diodes.

III. Experimental Results

A. Electrical Characteristics at High Temperatures

Figure 3 shows the measured current-voltage curves for the p^-/p^+ diode at 25°C and 200°C. The similar waveforms were observed for all diodes.

Figure 4 shows the experimentally obtained reverse recovery waveforms for the same diode. Reverse recovery measurement were carried out with an applied dI/dt of 6 A/μs and applied reverse voltage of 40V. The temperature dependence of t_{rr} was very small.

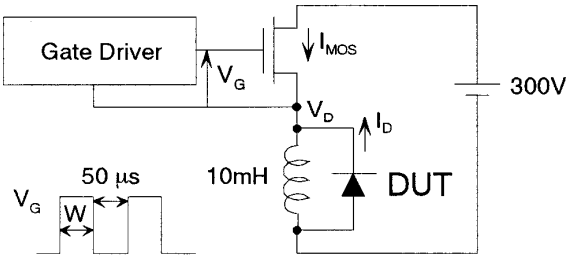
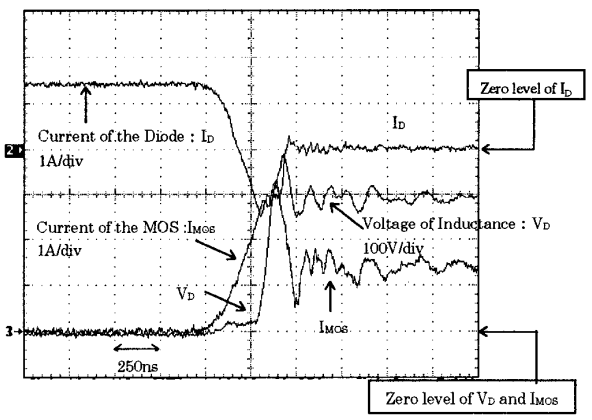


Fig. 5 Circuit configuration for the measurement of maximum controllable current in reverse recovery transient.

(a)



(b)

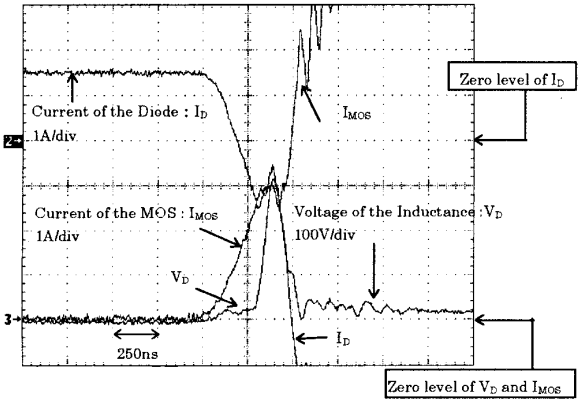


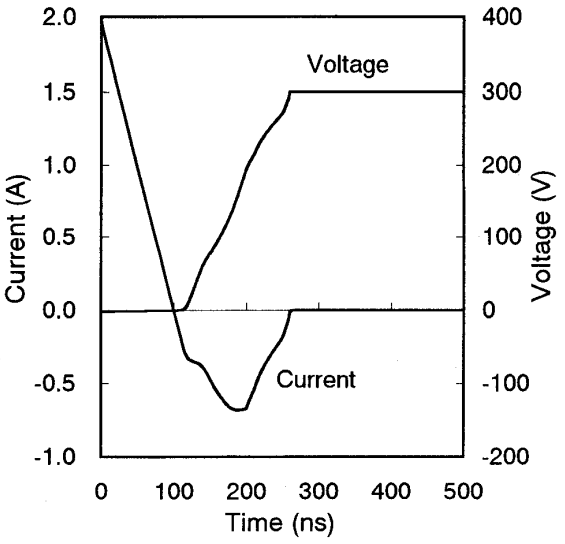
Fig. 6 Measured reverse recovery waveforms for a diode (a) before destruction and (b) after distribution at 150°C.

B. Maximum Controllable Current

We measured the maximum controllable current in the reverse recovery transient at 150°C for three diodes under the circuit configuration as shown in fig. 5, which simulates actual inverter circuits.

In the measurements, the MOSFET is turned-on, and the stored energy in the inductor. Then, the MOSFET is turned-off, the stored energy discharges through the diode under test. The diode is then turned-off by switching-on, again, the MOSFET. The magnitude of the diode current is adjusted by the MOSFET on-state duration.

(a)



(b)

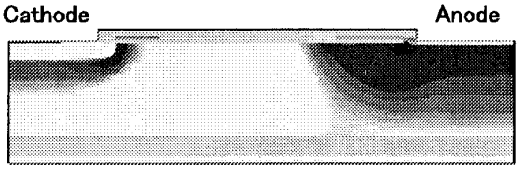


Fig. 7 Calculated (a) reverse recovery waveforms for the p-/p+ diode and (b) distribution of the impact ionization rate at 200 ns.

Figure 6 shows the measured maximum controllable current waveforms for a diode before and after destruction. It was found that n^+/p^+ diode easily destroyed in the reverse recovery transient at high temperature of 150°C because of a parasitic npn transistor action. The best optimization was found in p^-/p^+ diodes. The 1 ampere rated p^-/p^+ diodes have a capability of 4 ampere current turn-off, as seen in fig. 8, where the applied dI/dt and dV/dt was 13 A/μs and 3 kV/μs, respectively.

Figure 7 (a) shows the calculated reverse recovery waveforms for the p^-/p^+ diode. The calculations were performed at the high forward current density of 500 A/cm^2. The reverse recovery current has two peaks when a large reverse voltage is applied. The first peak appeared when the diode is initially reversed biased. The second peak is caused by a rapid dV/dt recovery and is often accompanied by impact ionization

The distribution of the impact ionization at 200ns is shown in fig. 7 (b). Significant impact ionization occurs mostly in the

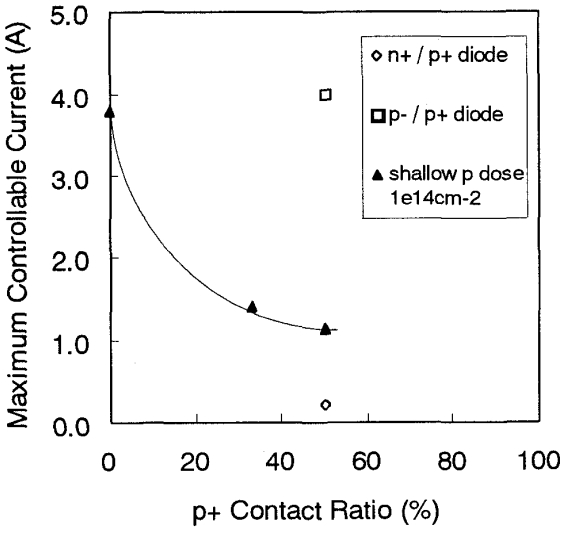


Fig. 8 Maximum controllable current as a function of p+ contact ratio over total p-emitter area. Maximum controllable current of n+/p+ and p-/p+ diodes are shown together.

drift region near the anode pn junction. This peak current induced the large Joule loss in the diode, resulting in the destruction.

Figure 8 shows the maximum controllable current of shallow p / p^+ diodes as a function of p^+ contact diffusion ratio over total p-emitter area. The measured maximum current of the n^+/p^+ diode and the p^-/p^+ diode are shown together in the figure. Shallow p/p^+ diodes exhibited the same ruggedness, if the dose of shallow p layer was optimized, and p^+ contact ratio was eliminated.

Figure 9 shows the circuit configuration of 3-phase inverter IC, using six 1A rated p^-/p^+ diodes and LIGBTs. We demonstrated the operation of motor speed control at 200°C.

IV. Conclusion

We measured the maximum controllable current in the reverse recovery transient at 150°C for three diodes. It was found that n^+/p^+ diode easily destroyed in the reverse recovery transient at high temperature of 150°C because of a parasitic npn transistor action. The best optimization was found in p^-/p^+ diodes. Shallow p/p^+ diodes exhibited the same ruggedness, if the dose of shallow p layer was optimized. We demonstrated the operation of motor speed control at 200°C.

Acknowledgment

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[2] H. Funaki, T. Matsudai, A. Nakagawa, N. Yasuhara and Y. Yamaguchi, *Proc. of 9th ISPSD*, 1997, pp.33-36.

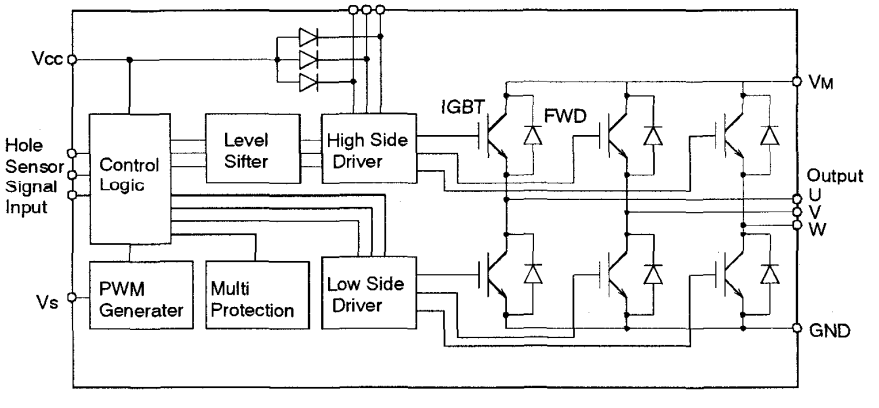

Fig. 9 Circuit configuration of 3-phase inverter IC, using six 1A rated p-/p+ diodes and LIGBTs.