New 1200V MOSFET Structure on SOI with SIPOS Shielding Layer

Hideyuki Funaki, Yoshihiro Yamaguchi, Keizo Hirayama, and Akio Nakagawa

Advanced Semiconductor Devices Research Laboratories, Toshiba Corporation
1 Komukai Toshiba-cho Saiwai-ku, Kawasaki 210-8582, Japan,
Tel: +81-44-549-2139, Fax: +81-44-520-1501, E-mail: hideyuki.funaki@toshiba.co.jp

Abstract

In this paper, we have experimentally obtained, for the first time, the 1200V lateral diodes and MOSFETs on SOI. The SOI structure is characterized by a SIPOS layer inserted between the silicon layer and the buried oxide. It was found that the new SOI diode breakdown voltage is determined by the conventional bulk pn junction theory and not by Resurf principle.

I. Introduction

It has been believed that the breakdown voltage of high voltage lateral devices, fabricated on SOI, depends on the buried oxide thickness as well as silicon layer thickness [1]. Figure 1 shows typical experimental results, showing how the diode or MOSFET breakdown voltage depends on the two parameters. It is very difficult to achieve a high breakdown voltage exceeding 600V, because a thicker buried oxide layer of 4 μm or more is required in the conventional structure. The authors have already proposed a new high voltage SOI device structure, which is free from the above constraints [2]. In this paper, we have experimentally obtained, for the first time, the 1200V lateral diodes and MOSFETs on SOI.

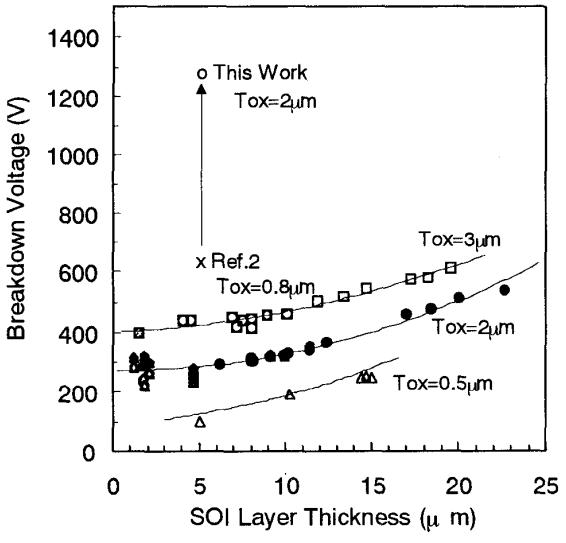


Fig. 1 Diode breakdown voltage as a function of SOI layer thickness with buried oxide thickness as a parameter.

II. Device Structures

Figure 2 shows the cross sectional views of the new diode on SOI with SIPOS shielding layer. The SOI structure is characterized by a SIPOS (Semi-insulating Poly-crystalline Silicon) layer inserted between the silicon layer and the buried oxide. The reported devices in this paper were fabricated on a 5.0μm thick n-layer over 2.0μm thick buried oxide. The thickness of SIPOS layer was varied from 0.1μm to 1.0μm. The drift length of every device was set at 120μm.

Figure 3 shows the plain layout of the diode. To reduce the surface electrical field, we adopted the p-resurf layer (impurity dose of 7.0×10^{11} cm^{-2}) and the spiral shaped resistive field plate of poly-silicon (SRFP) [3].

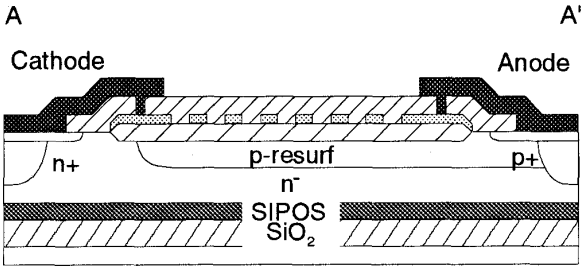


Fig. 2 Cross sectional view of diode on 5μm SOI with 1μm SIPOS and 2μm buried oxide layer.

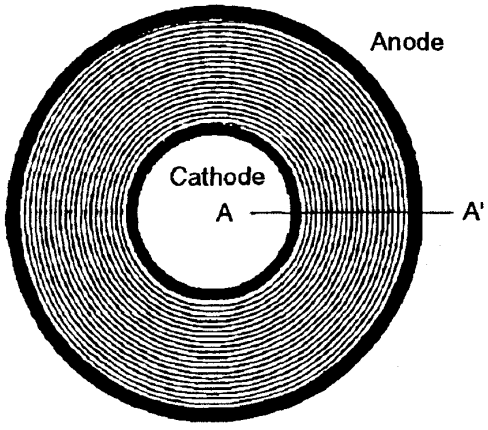


Fig. 3 Plain view of a diode on SOI with SIPOS layer. The diode has the spiral shaped resistive field plate to reduce the surface electrical field.

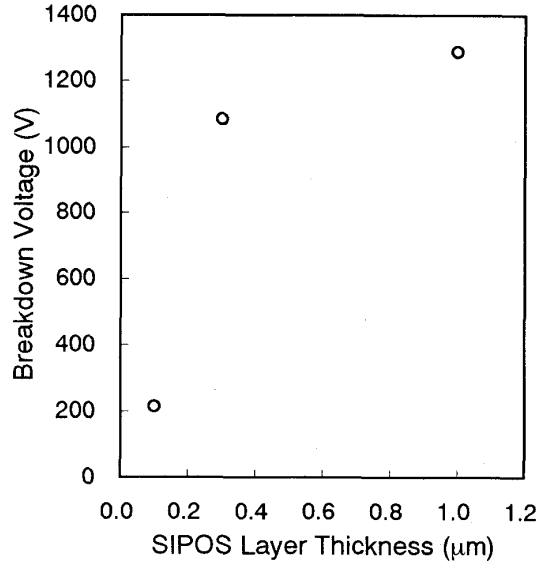


Fig. 5 Diode breakdown voltage as a function of the thickness of SIPOS layer.

III. Experimental Results

A. Breakdown Voltages of Diodes

As the SIPOS layer effectively shields the influence of the substrate bias, 1300V breakdown voltage was obtained by using only 2.0μm thick buried oxide with 1.0μm thick SIPOS layer as shown in figure 4. The results are also plotted in figure 1 as a comparison. The breakdown voltage of the new diode is even greater than that of diodes on 10μm thick silicon layer / 20μm thick buried oxide [1].

Figure 5 shows the breakdown voltages of the fabricated diodes as a function of the thickness of SIPOS layer. The breakdown voltage depends on the thickness of SIPOS layer.

Figure 6 shows the breakdown voltages for the diodes on SOI with 1.0μm thick SIPOS as a function of the net implant impurity dose (Q_D–Q_A) of the n-drift layer with and without metal wire layers. No breakdown voltage degradation by metal

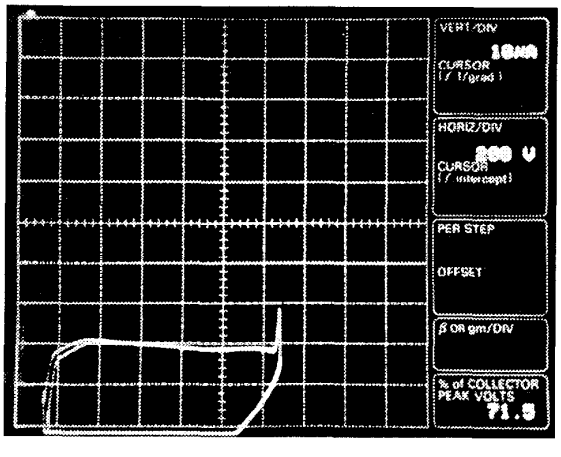


Fig. 4 *Experimentally obtained reverse current-voltage curve for the diode on* SOI with 1μm thick SIPOS layer.

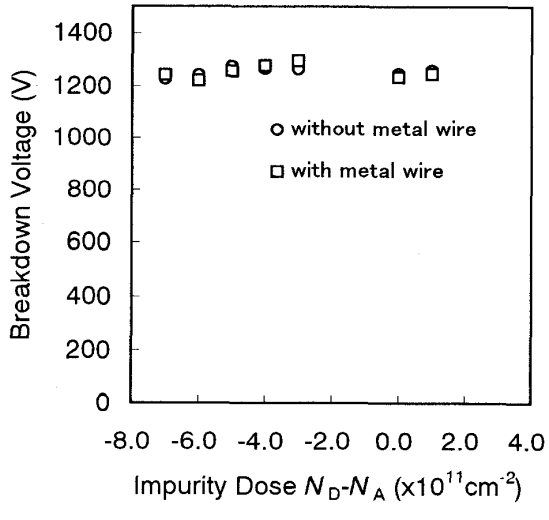


Fig. 6 Breakdown voltage for the diodes on SOI with 1μm thick SIPOS layer as a function of the net implant impurity dose of the n-drift layer with and without metal wire.

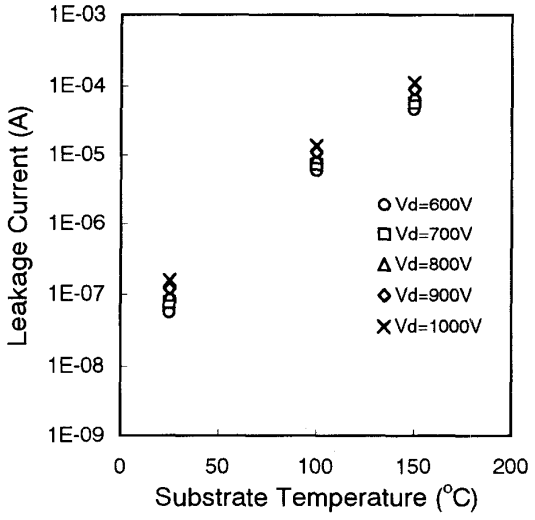
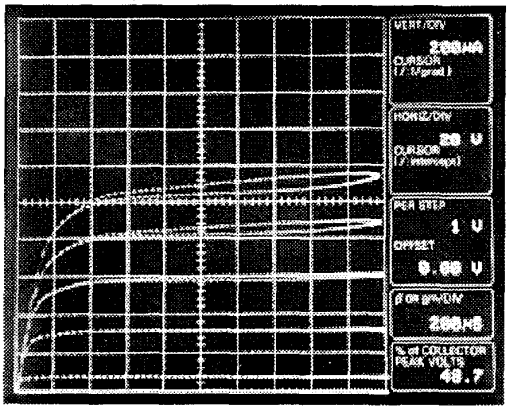


Fig. 7 Leakage current for the diode on SOI with 1μm thick SIPOS layer as a function of the substrate temperature with applied voltage as a parameter.

wire was observed if the spiral resistive field plate was used. The obtained breakdown voltages did not depend on p- and n-type impurity within the experimentally examined impurity dose. It was found that the new SOI diode breakdown voltage of 1300V is determined by the conventional bulk pn junction theory and not by Resurf principle, which is believed to be valid for the conventional SOI device breakdown. In other words, the breakdown voltage is determined by the high resistivity silicon layer impurity concentration and not by the total impurity dose of the SOI layer.

Figure 7 shows the leakage current for the diode on SOI with

(a)



(b)

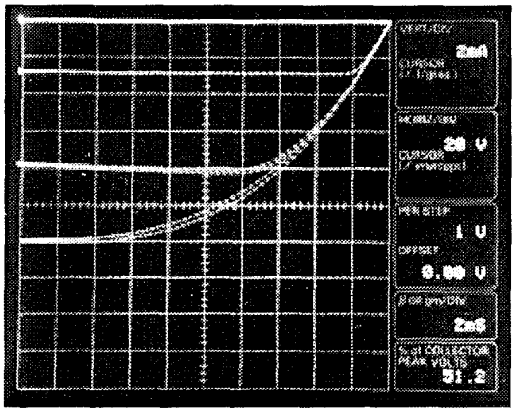
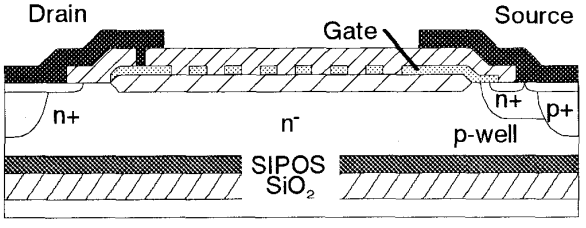


Fig. 9 Current-voltage curves of fabricated (a) n-ch and (b) p-ch MOSFETs on SOI with SIPOS layer.

(a)



(b)

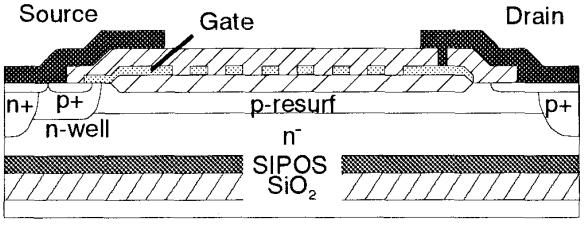


Fig. 8 Cross sectional views of (a) n-ch and (b) p-ch MOSFETs on SOI with SIPOS layer.

1.0μm thick SIPOS layer as a function of the substrate temperature with applied voltage as a parameter. The leakage current increased exponentially with temperature.

B. On-state Characteristics of MOSFETs

Figure 8 shows the cross sectional views of the fabricated n-channel (no p-resurf) and p-channel lateral MOSFETs on SOI with SIPOS shielding layer.

Figure 9 shows the current-voltage characteristics of the n-ch and p-ch MOSFETs. The new structure has successfully increased the device breakdown voltage without sacrificing the device electrical characteristics. The on-resistance of n-ch MOSFET was one order higher than that of the p-ch MOSFET. This suggests that the impurity atoms in n-drift layer diffused into the SIPOS layer through the thermal processes.

IV. Conclusion

We have experimentally obtained the 1200V lateral diodes and MOSFETs on SOI. The SOI structure is characterized by a SIPOS layer inserted between the silicon layer and the buried oxide. It was found that the new SOI diode breakdown voltage is determined by the conventional bulk pn junction theory and not by Resurf principle. The new structure has successfully increased the device breakdown voltage without sacrificing the device electrical characteristics.

Acknowledgment

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