High Voltage Lateral MOS Thyristor Cascode Switch on SOI — Safe Operating Area of SOI-Resurf Devices —

Hideyuki Funaki, Norio Yasuhara, and Akio Nakagawa

Materials and Devices Research Laboratories, Toshiba Corporation
1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan
Phone: +81-44-549-2139; Fax: +81-44-520-1802

Abstract

A high voltage lateral MOS thyristor cascode switch on SOI was proposed. It consists of a high voltage MOS thyristor, a low voltage MOSFET and a pn diode. Excellent on-state and switching characteristics were numerically and experimentally obtained. The safe operating area (SOA) of SOI-Resurf devices were discussed.

Introduction

Lateral MOS-gated thyristors fabricated on SOI are attractive devices for use in high voltage power ICs because they are expected to have lower on-state voltage drops than lateral IGBTs. The devices such as EST and MCT have been already studied by many researchers [1,2]. In this paper, we propose a high voltage lateral MOS thyristor cascode switch [3] on SOI, consisting of a high voltage MOS thyristor, a low voltage MOSFET and a pn diode. This kind of hybrid devices can be easily integrated in the same chip by trench isolation.

The present paper also discusses Safe Operation Area of SOI devices. Resent papers have shown that SOI devices realize high static breakdown voltage under the Resurf principle [4,5]. However, the dynamic breakdown mechanism may reduce the device sustaining voltage due to the carrier (hole) storage during switching transients.

Device Structure and Operation

The cross-sectional view of the proposed device structure is shown in Fig. 1. The devices were fabricated using 2 μm design rule on SOI of a 10 μm thick n-type silicon with the 1.0×10^{12} cm^{-2} impurity dose over 2 μm buried oxide. Figure 2 shows the equivalent circuit of the hybrid device. If the two MOS gates are positively biased and the forward voltage drop of the MOSFET becomes lower than the diode forward voltage, the MOS thyristor latches on. Regarding the turn-off, the n^+ emitter and p-base junction is reverse biased and the injection of electrons from the n^+ emitter is stopped by switching off the MOSFET. The hybrid device is, thus, able to be turned off.

Figure 3 shows the schematic layout of the hybrid device. Each device is isolated by 1 μm width trenches. The gate lengths of the MOS thyristor and the MOSFET are 3 μm and 6 μm, respectively. The electrodes of the MOSFET have a comb like shape and the total gate width is typically 20 mm. The total device area including the MOSFET and the pn diode is 1 mm × 0.5 mm, which is only twice as large as that of the LIGBT.

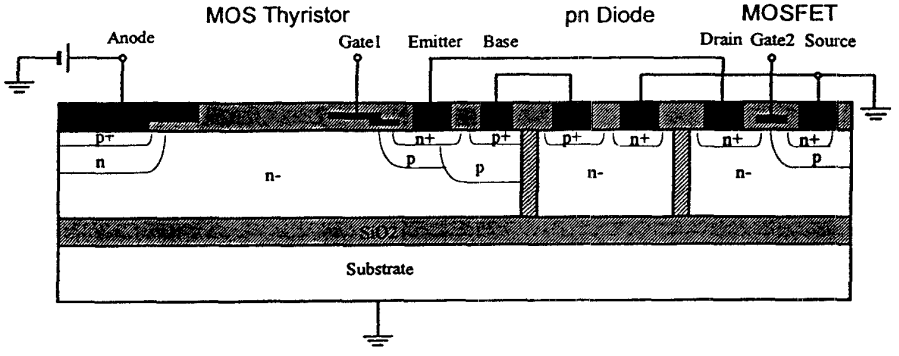

Fig. 1 Cross sectional-view of a high voltage lateral MOS thyristor cascode switch on SOI.

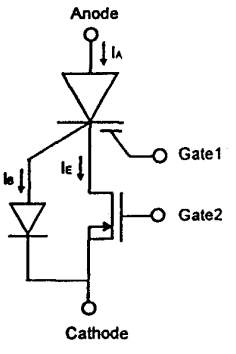

Fig. 2 Equivalent circuit of the hybrid device.

0-7803-3106-0/96$5.00©1996 IEEE

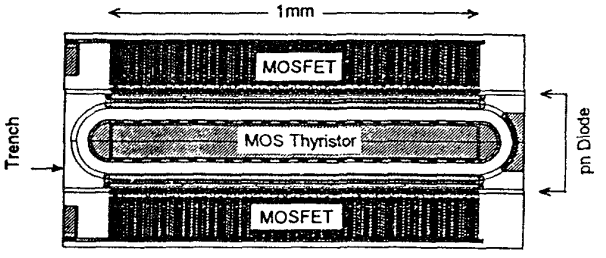

Fig. 3 Schematic layout of the hybrid device.

Electrical Characteristics

A. Device Breakdown Voltages

Figure 4 shows the measured forward blocking curves for the hybrid device. The breakdown voltage was 340V, which was the same as that of the MOS thyristor. The breakdown voltage of the MOSFET was 18 V.

B. On-State Characteristics

Figure 5 compares the calculated current-voltage curves for the cascode device and the conventional LIGBT with on-resistance of the MOSFET as a parameter [4]. The MOSFET switch was treated as the external circuit in the calculations. The current density of the cascode device was predicted to be more than five or six times larger than that of LIGBTs which have the same device area as that of the MOS thyristor.

Figure 6 shows the calculated anode, cathode and p-base currents as a function of the p-base potential or the diode voltage drop. The anode current has maximum at the diode voltage drop of 1.25 V in the case of the anode voltage of 2.5V.

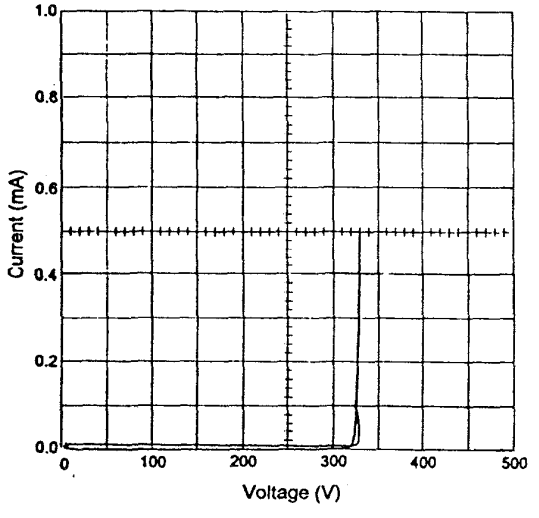

Fig. 4 Forward blocking curves for the hybrid device. The breakdown voltage of 340 V was obtained.

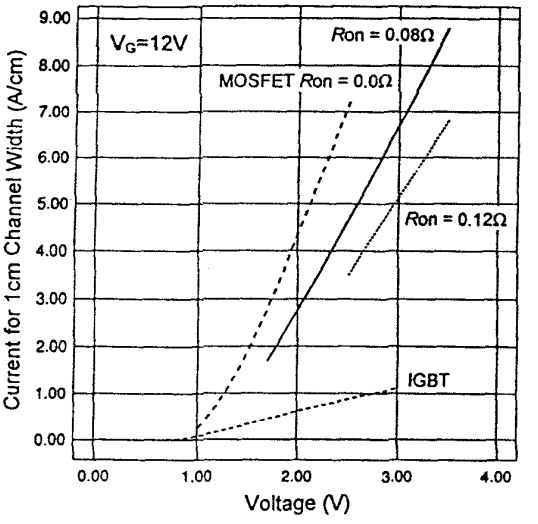

Fig. 5 Calculated current-voltage curves for the hybrid device and conventional LIGBT with MOSFET *R*on as a parameter.

The experimentally obtained current-voltage curves ware shown in Fig. 7. The large anode current capability of 980 mA (200 A/cm^2) was obtained at the forward voltage drop of 2.0 V in contrast to 160 mA for the LIGBT.

C. Switching Characteristics

Figure 8 shows the calculated turn-off waveforms for the cascode devices. Both the Gate 1 and 2 were turned off simultaneously. The calculations are under resistive load and the applied voltage of (a) 100 V and (b) 200 V. In the case of 100V, the turn-off time of the cascode switch is about 0.1 μs and extremely faster than that of the conventional LIGBT. This is because the initial current density is much larger than that of the LIGBT. In the case of 200 V, after

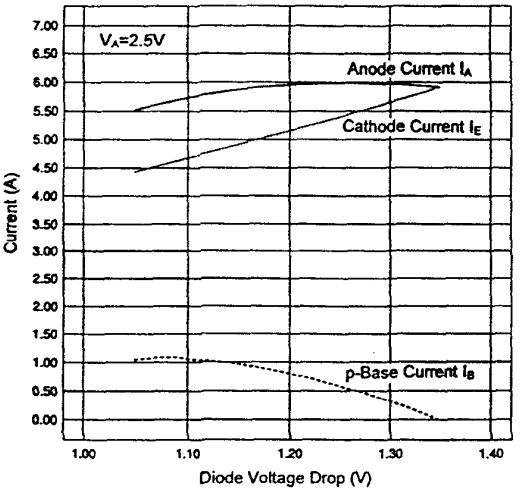

Fig. 6 Calculated anode, cathode and p-base currents as a function of the p-base potential or the diode voltage drop.

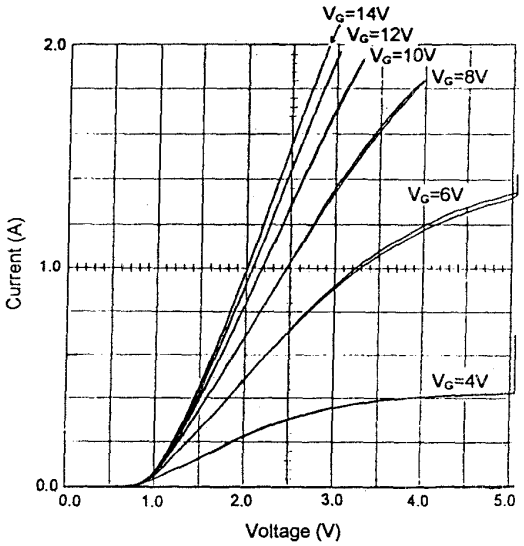

Fig. 7 Measured current-voltage curves.

MOSFET gate voltage is reduced to zero, the anode voltage increase and the current initially decrease rapidly. However, the waveform oscillates above the 120 V anode voltage due to impact ionization, and the device was not turned off.

Figure 9 indicates the measured turn-off waveforms for the cascode devices. The turn-off time is about 1μs. The waveform for the applied voltage of 200V had the same terrace shape tail current as that for the LIGBT because of the induced p-channel on the buried oxide [5]. However, the terrace current was lower than that for the LIGBT. The measured maximum turn-off current reached up to 2A and did not depend much on the structures of the cathode side.

Figure 10 shows a turn-off waveforms for a specific case where the MOS thyristor gate voltage(Gate 1 in Fig. 2) was reduced to zero with 20 μs delay time after MOSFET gate voltage (Gate 2) was reduced to zero in advance. As the Gate 2 was turned off with keeping the positive Gate 1 voltage above the threshold, the n^+ emitter electrode potential rose to 5V and the stable anode current of 100 mA was observed during the Gate 1 is on. This current increases as the applied source voltage increases and it is identified as the current supplied by the avalanche multiplication in the junction of the n+ emitter and the p-base [7]. The maximum current can be increased by using the proposed delayed turn-off of the thyristor gate.

Safe Operating Area of SOI-Resurf Devices

In this section, we propose a new model, limiting the safe operating area of SOI devices.

As is shown in the Fig. 8b, the maximum anode current is limited by the avalanche multiplication. These phenomena generally happens in all the SOI devices such as IGBTs and

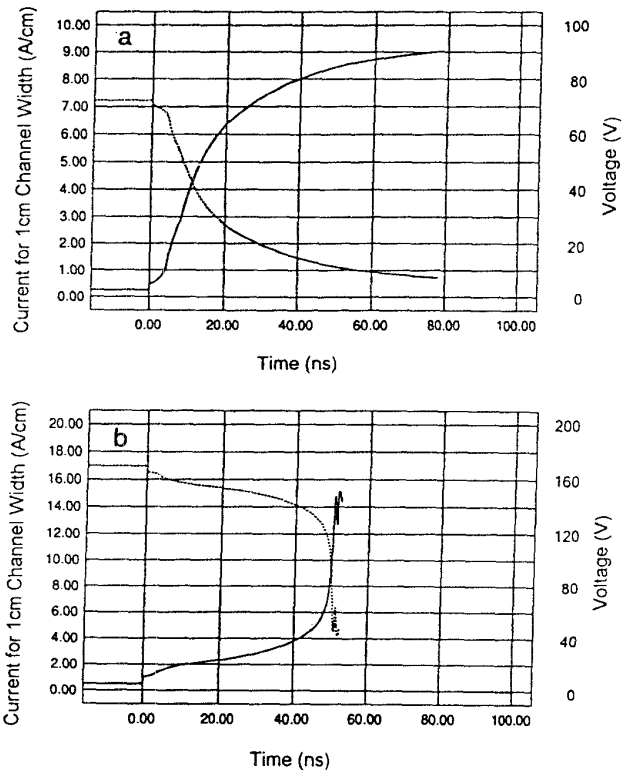

Fig. 8 Calculated turn-off waveforms under the source voltage of (a) 100V and (b) 200V.

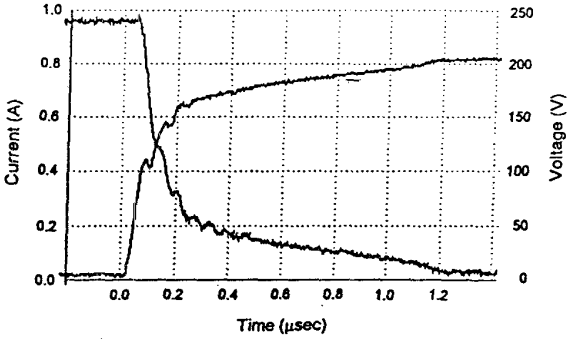

Fig. 9 Measured turn-off waveform.

ESTs, which switches current by so called emitter-open mode. Thus, the results obtained in this section are applicable for all such SOI devices.

In order to explain the oscillation of the waveform (or SOA limit) in Fig. 8b, the total positive charge concentration N_D+p and the carrier generation distributions in the depletion region near the MOS-gate of the thyristor were illustrated in Fig. 11a and 11b, respectively. The total positive charge increases in the depletion layer due to the large hole current flow because the all of the current is carried by holes after the electron injection from n^+ emitter is

stopped. Figure 12 shows the current flow lines in the MOS thyristor portion. The hole current dose not flow homogeneously under the MOS gate. The net positive charge increases in the depletion layer finally exceeds the optimum charge determined by Resurf principle. This results in the reduction in the SOI device breakdown voltage during the turn-off period. Figure 13 schematically shows the SOA for SOI devices. The dynamic breakdown voltage depends on the current for the unit device width. The SOA curve is identical to the static breakdown voltage curve when the current is zero.

Our experimental results under the short-circuit operation indicate that the breakdown voltage of the SOI devices which have the static breakdown voltages of 340V was dynamically reduced by about 40% for the current density of 800 A/cm^2.

Acknowledgment

The authors would like to thank General Manager Makoto Azuma and Dr. Yasuo Ikawa for their support.

References

[1] Y.S.Huang, S.Sridhar and B.J.Baliga, "Junction and Dielectrically Isolated Lateral ESTs for Power ICs," *Proc. of 5th ISPSD*, pp. 259-263, 1993.

[2] M.N.Darwish, "A New Lateral MOS-Controlled Thyristors," *IEEE Electron Device Lett.*, vol. EDL-11, pp. 256-257, 1990.

[3] M.S.Adler, "A Comparison between BiMOS Device Types," *IEEE Power Electronics Specialists Conference Record*, pp. 371-377, 1982.

[4] S.Merchant, E.Arnold, H.Baumgart, S.Mukherjee, H.Pein, and R.Pinker, "Realization of High Breakdown Voltage (>700V) in Thin SOI Devices," *Proc. of 3rd ISPSD*, pp. 31-35, 1991.

[5] I.Omura, N.Yasuhara, A.Nakagawa and Y.Suzuki, "Numerical Analysis of SOI IGBT Switching Characteristics — Switching Speed Enhancement by Reducing the SOI Thickness," *Proc. of 5th ISPSD*, pp. 248-253, 1993.

[6] I.Omura and A.Nakagawa, "Bipolar MOS Power Devices Simulator TONADDE II C Taking into Account External Circuit," *Proc. of 2nd ISPSD*, pp. 32-37, 1990.

[7] N.Iwamuro, M.S.Shekar and B.J.Baliga, "A Study of EST's Short-Circuit SOA," *Proc. of 5th ISPSD*, pp. 71-76, 1993.

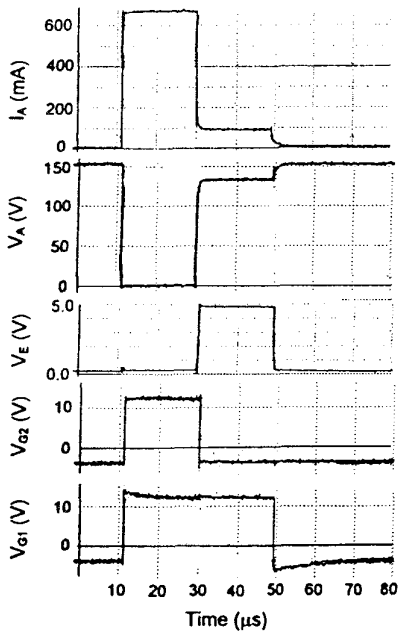

Fig. 10 Measured turn-off waveforms when the Gate 1 was turned off with 20 μs delay time after the Gate 2 voltage was reduced to zero.

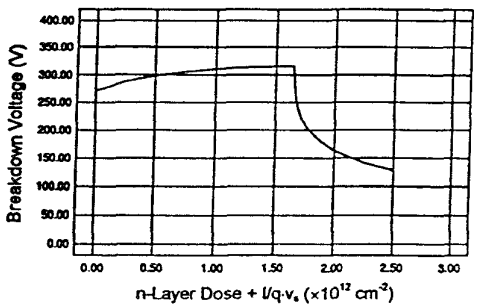

Fig. 13 SOA for SOI devices. Here, I is the current for the 1cm device width and v_s is the saturation velocity.

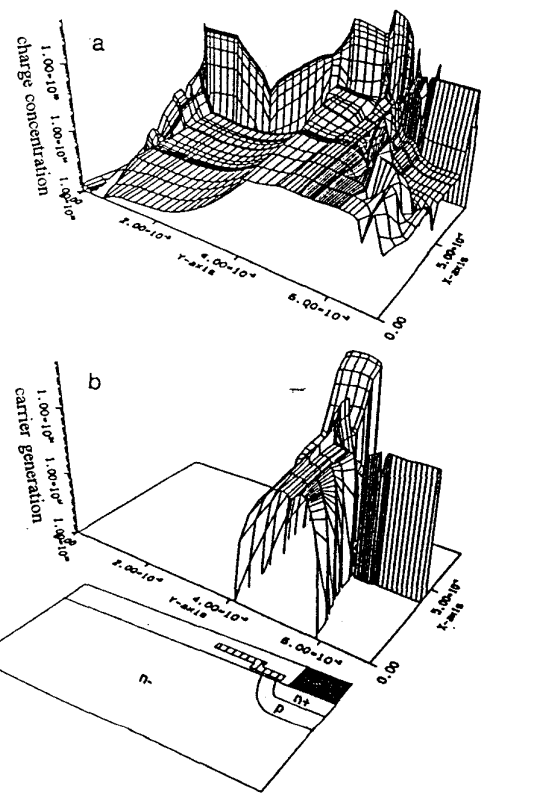

Fig. 11 (a) Total charge concentration and (b) carrier generation distributions near the MOS-gate of the thyristor.

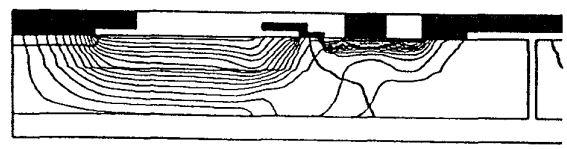

Fig. 12 Current flow lines in the MOS thyristor portion.