Numerical Predictions of p-channel SOI LIGBT Electrical Characteristics

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Abstract

We have, for the first time, numerically investigated the electrical characteristics including breakdown voltage of the p-channel SOI LIGBTs. It was found that the impurity dose of the n-drift layer for the SOI double Resurf structure can be increased without lowering the breakdown voltage, and that the on-resistance and switching characteristics of 250 V p-channel IGBTs on SOI are sufficiently good and almost comparable to those of n-channel IGBTs due to the effects of SOI-Resurf.

I. Introduction

P-channel lateral IGBTs on thin SOIs are attractive devices for high-side switching application in power ICs because, for example, the level shifters and the high-side gate drivers become simple for the circuits in inverter ICs. We have already proposed high voltage p-channel MOSFET/IGBT structures on SOIs [1]. We show, for the first time, that SOI structures, which consist of p-diffusion layer on n-type SOI, acts as a SOI double Resurf layer. Recent work has shown that the device breakdown voltage on SOI abruptly decreases as the impurity dose of the n-drift layer increases beyond the critical value [2]. On the other hand, Vaes et al. suggested that a diode formed by a double Resurf layer (p-drift/n-drift/p-substrate) can increase the critical value of the n-drift impurity dose and that it realizes a lower on-resistance than that obtained by a simple Resurf structure (n-drift/p-substrate) [3]. We confirmed that this is also true for a double Resurf layer on SOI. We, further, numerically confirmed that the on-resistance and switching characteristics of the 250 V p-channel SOI LIGBTs are as good as those for equivalent n-channel LIGBTs.

II. Device Structures

A cross-sectional view of simulated 250 V p-channel SOI LIGBTs is shown in Fig. 1. A 1 μm surface p-type diffusion layer was formed on a 5 μm n-type SOI layer to serve as a p-drift layer as well as a double Resurf layer. The distance between the drain and the gate (the n-drift layer length) was assumed

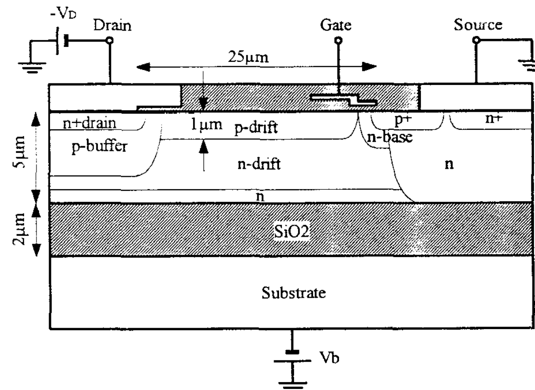

Fig. 1. Cross-sectional view of simulated 250 V p-channel SOI LIGBTs.

to be 25 μm, and the buried oxide thickness was 2 μm. A 1 μm deep n-type diffusion layer was formed on the buried oxide to obtain higher breakdown voltages.

III. Device Breakdown Voltage

The TONADDE II B program was used for the breakdown voltage calculations [4]. Figure 2 shows the electric field distribution for a SOI double Resurf structure at an applied voltage of 280 V. In this figure, three high electric field portions are identified. These are the portion (A), marked in the figure near the surface of the p-drift, the portion (B) at the bottom of n^+ layer, and the portion (C) at the junction of p- and n-drift layers.

Figure 3 shows the calculated breakdown voltages as a function of n-drift impurity dose with p-drift impurity dose as a parameter. The solid line in the figure represents the results for the simple SOI Resurf structure without p-drift layer. It appears that the critical value of the impurity dose of the n-drift layer for the SOI double Resurf structure can be increased by about 40% from 1.9×10^{12} cm^{-2} to 2.7×10^{12} cm^{-2}, whereas the breakdown voltage rises only by about 5% because it basically limited by the breakdown voltage of the drain n^+/n^-/oxide structure. Figure 4 shows the calculated breakdown voltages as a function of p-drift impurity dose with n-drift

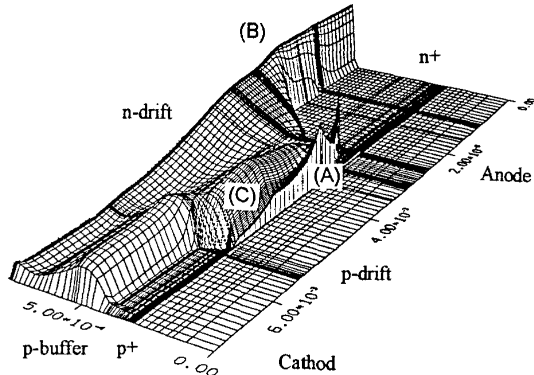

Fig. 2. Calculated electric field distribution at an applied voltage of 280 V.

impurity dose as a parameter.

Figure 5 shows the phase diagram of breakdown as functions of p-drift and n-drift impurity dose. In the case of lower n-drift dose and higher p-drift dose (Case 1), the breakdown takes place at the portion (A), shown in Fig. 2. In the case of lower p-drift dose and higher n-drift dose (Case 2) and higher n-drift dose (Case 3), the breakdown takes place at the portions (B) and (C), respectively. This diagram shows that the maximum breakdown voltage and optimized dose was obtained at the cross point Y, and that, when the p-drift impurity dose exceeds 1.8×10^{12} cm^{-2}, the breakdown directly changes from Case 1 to Case 3 with the increase in the n-drift impurity dose.

IV. Electrical Characteristics

A. Current-Voltage Characteristics

Figure 6 shows the calculated current-voltage characteristics with p-buffer impurity dose as a parameter. The broken curve in Fig. 6 represents the result for the p-buffer impurity dose of 5.0×10^{13} cm^{-2}. Figure 7A shows the hole density distribution at the 2 V drain voltage. The low excess hole density in the n-drift layer indicates that the sufficient conductivity modulation has not occurred. Whereas the I-V curves for lower impurity dose (solid and dotted curves) show that the conductivity modulation occurs in both the p- and n-drift regions above 1.5V drain voltage. Forward voltage drop for a p-buffer dose of 2.5×10^{13} cm^{-2} is 2.2 V at 100 A/cm^2 current density. These p-channel IGBTs have on-resistance as low as those of n-channel IGBTs.

Figure 8 shows substrate bias effects on the current-voltage characteristics for the device of 2.5×10^{13} cm^{-2} p-buffer dose. The magnitude of the drain current for the same drain-source voltage increases as the substrate bias changes from 0 V to -100 V. The hole density distribution for the -100V of substrate bias is shown in Fig. 7C. A p-channel (inversion layer) is induced on the buried oxide and a part of the hole current flows through the channel, contributing to reduction of the total device resistance.

B. Switching Characteristics

The switching simulations were carried out under a resistive load, using the TONADDE II C program [5]. Figure 9 shows a high side switch configuration.

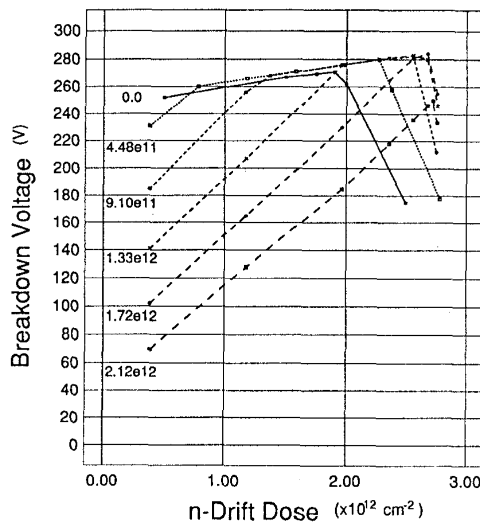

Fig. 3. Calculated breakdown voltages as a function of n-drift impurity dose with p-drift impurity dose as a parameter.

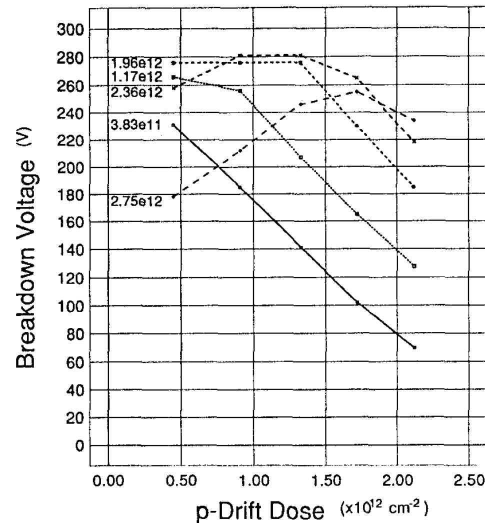

Fig. 4. Calculated breakdown voltages as a function of p-drift impurity dose with n-drift impurity dose as a parameter.

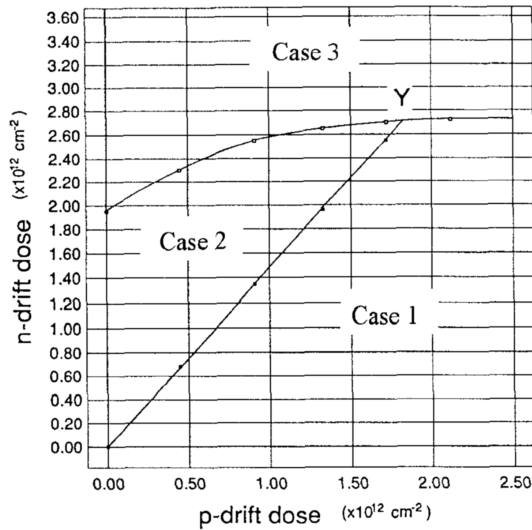

Fig. 5. Phase diagram of breakdown as functions of p-drift and n-drift impurity dose.

Figure 10 shows the calculated switching waveform of the p-channel LIGBT with an applied voltage of 100 V. The calculated turn-off time is 0.5 μs when a 1 μs carrier lifetime is assumed for the n-drift region. This switching speed is comparable to those of 250 V n-channel lateral IGBTs on SOI. The high switching speed was obtained because both the p- and n-drift layers are rapidly depleted by double Resurf effects.

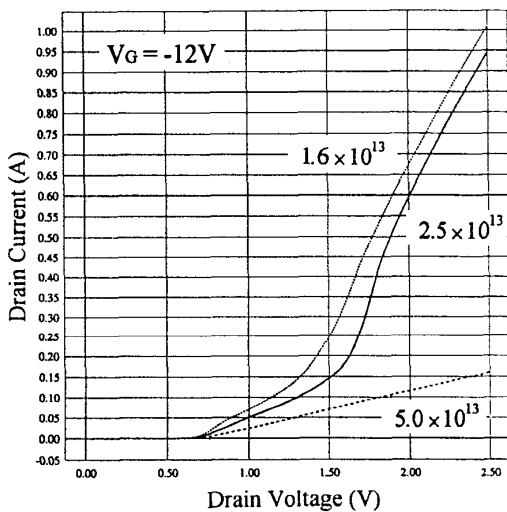

Fig. 6. Current-voltage characteristics with p-buffer impurity dose as a parameter: (A) 5.0x10^{13} cm^{-2}, (B) 2.5x10^{13} cm^{-2} and (C) 1.6x10^{13} cm^{-2}.

V. Conclusion

We have numerically investigated the electrical characteristics including the breakdown mechanism of double Resurf structures in p-channel lateral IGBTs on SOIs. It was found that the critical value of the n-drift impurity dose for the SOI double Resurf structure can increase by about 40% over that for the simple SOI Resurf structure without p-drift layer. A forward voltage drop of 2.2 V at 100 A/cm^2 current density and the turn-off time of 0.5 μs were obtained for 250 V p-channel IGBTs. These are sufficiently good, and almost comparable to those of n-channel IGBTs due to the effects of SOI-Resurf.

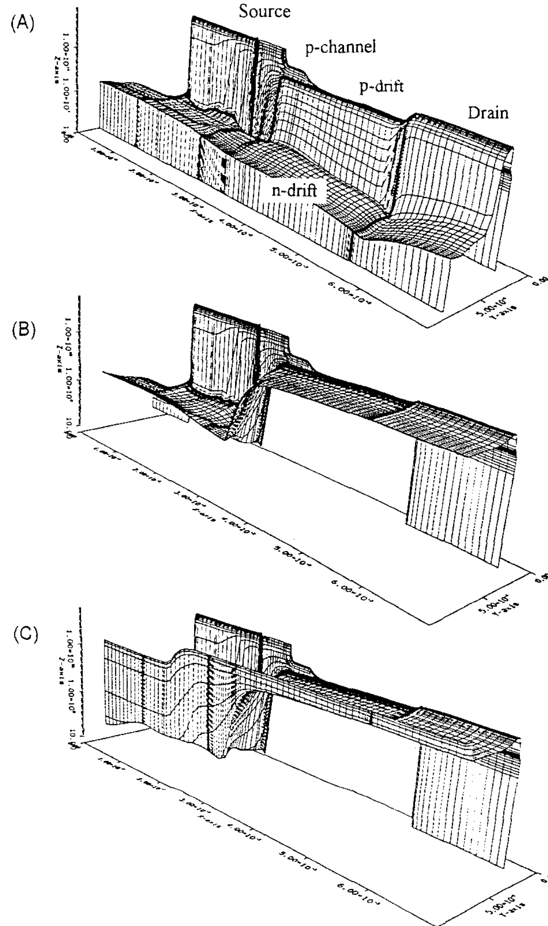

Fig. 7. Hole density distributions at 2 V drain voltage: (A) 5.0x10^{13} cm^{-2} p-buffer impurity dose and 0V substrate bias, (B) 2.5x10^{13} cm^{-2} and 0 V, and (C) 2.5x10^{13}cm^{-2} and -100 V.

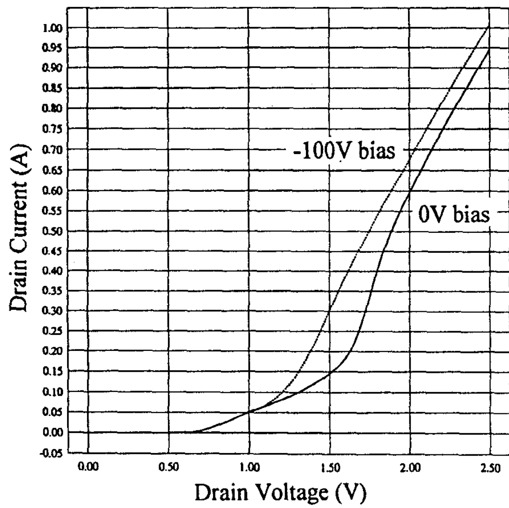

Fig. 8. Substrate bias effects on the current-voltage characteristics for the device of $2.5x10^{13}$ cm^{-2} p-buffer impurity dose.

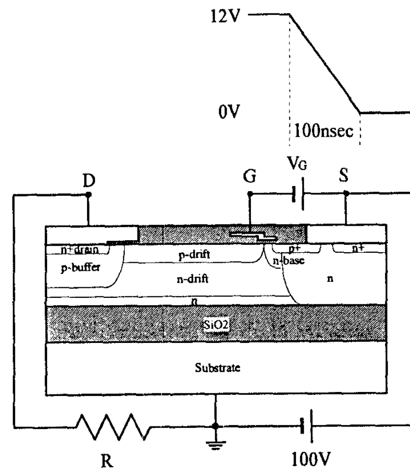

Fig. 9. Simulated circuit.

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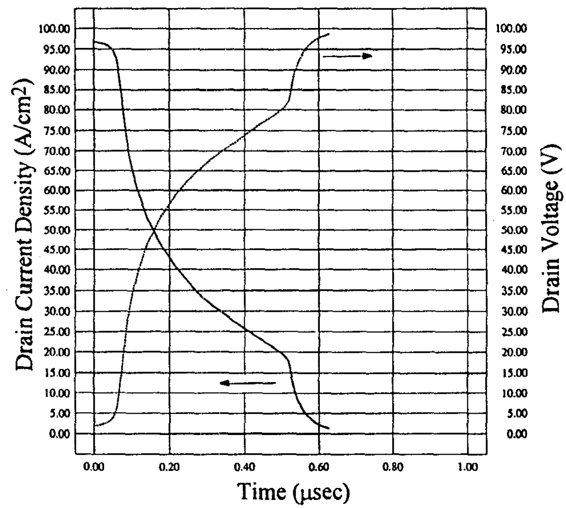

Fig. 10. Calculated switching waveforms. The p-buffer impurity dose was assumed to be $2.5x10^{13}$ cm^{-2}.