

Subcircuit SPICE Modeling of a Lateral IGBT for High Voltage Power IC Design

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Abstract

In this paper, a subcircuit model of lateral IGBTs on SOI substrate for SPICE simulation is presented. The model accurately takes into account the characteristics of lateral IGBTs based on the results of 2-D device simulators. Static and transient analysis of a lateral IGBT was carried out, using this model. The simulation results agreed very well with experimental results. An application of the proposed model to a over current protection circuit design is presented.

I. Introduction

Lateral IGBTs on thin SOIs are increasingly accepted as switching devices in high voltage power ICs because of their low on resistance due to conductivity modulation, and their compatibility with LSI processes. In order to design a large scale circuit including power devices, a CAD tool for IGBTs is indispensable. SPICE is the most generally used circuit simulator but it doesn't include models of IGBTs. There have been several reports of development of models of IGBTs suitable for SPICE[1-4]. Subcircuit modeling is one of the approaches to simulate a circuit including an IGBT. Shen et al. [2] proposed a model for SPICE of a vertical IGBT, and showed that it is in good agreement with experimental results. However, the existing models of vertical IGBTs cannot be applied to lateral IGBTs because lateral IGBTs have the unique terrace shaped turn-off waveforms as seen in Fig. 1. This paper presents, for the first time, a subcircuit model for lateral IGBTs, accurately taking into account the terrace shaped tail current based on the results of 2-D device simulations.

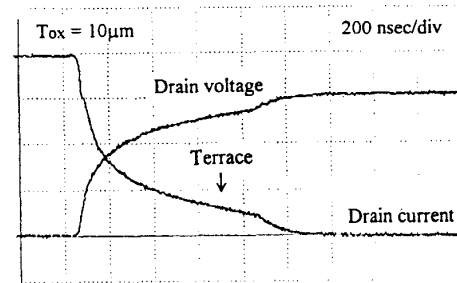


Fig. 1 Experimentally obtained turn-off waveform of lateral IGBT on a 10 μm SOI.

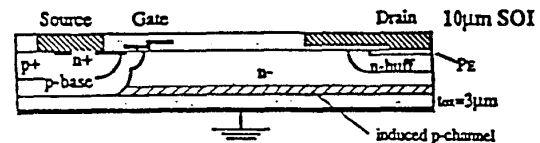


Fig. 2 Cross sectional view of a lateral IGBT.

II. Modeling of lateral IGBT on SOI substrate

A cross-sectional view of a lateral IGBT on SOI is shown in Fig. 2. This kind of n-channel IGBT can be modeled as a pnp bipolar transistor, whose base current is supplied by an n-channel MOSFET. A new subcircuit representation of a lateral IGBT is proposed in Fig. 3. This model is characterized by an additional high voltage p-channel MOSFET and a capacitor. Fig. 1 is an experimentally obtained switching waveform of a lateral IGBT on a 10 μm SOI, which is characterized by unique terrace shaped tail current with abrupt decay at the end of turn-off. Two dimensional device simulation was presented in Ref.[5] to analyze this phenomenon.

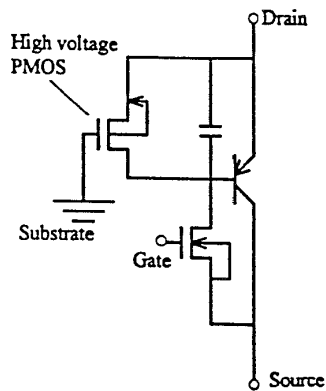


Fig. 3 A new subcircuit representation of a lateral IGBT

During the turn-off period, a depletion layer (space charge region) develops. When the drain voltage recovers to a high value, a p-channel is induced in SOI layer on the bottom oxide. In the depletion layer, most of the hole current flows through the induced p-channel on the buried the oxide. The induced p-channel continue to supply a relatively large terrace current for a while during turn-off period (the terrace current period). The resistance of the bottom p-channel depends on the applied drain voltage, because the p-channel is induced by the MOS (substrate/oxide/SOI-layer) structure. The terrace current starts to abruptly decay when the entire stored carrier has been removed. Therefore, when the drain voltage is too low to induce the bottom p-channel, the terrace current does not appear in its turn-off waveform.

In the proposed model, the added capacitor represents the stored excess carriers in the SOI-layer and the additional p-channel MOSFET represents the induced p-channel on the buried oxide. The p-channel MOSFET has a high threshold voltage such as 100 V, because the thick buried oxide serves as a gate oxide and the p-channel is induced when the drain voltage exceeds this threshold voltage.

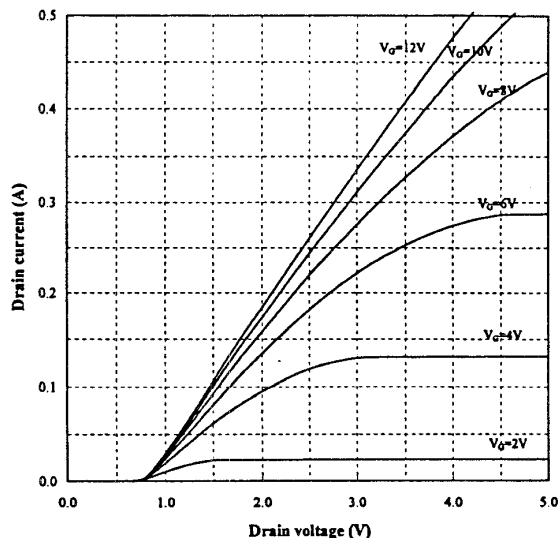


Fig. 4 Simulated current voltage curve of a lateral IGBT on SOI.

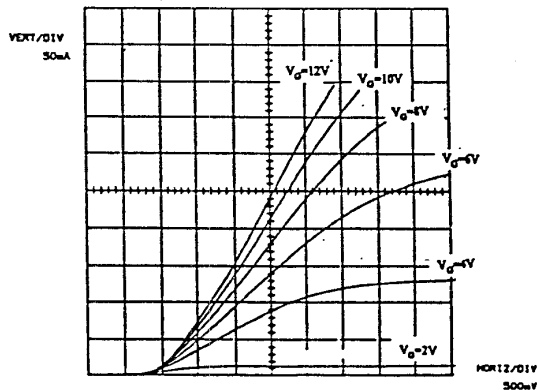


Fig. 5 Experimentally obtained current voltage curve of a lateral IGBT on SOI.

III. Simulation Results

The proposed model can accurately simulate experimentally obtained current-voltage curves of a lateral IGBT. The simulated curves, shown in Fig. 4, agrees very well with experimental data of Fig. 5.

Device turn-off simulations were carried out for IGBTs on 10 μm SOIs. Fig. 6 shows a

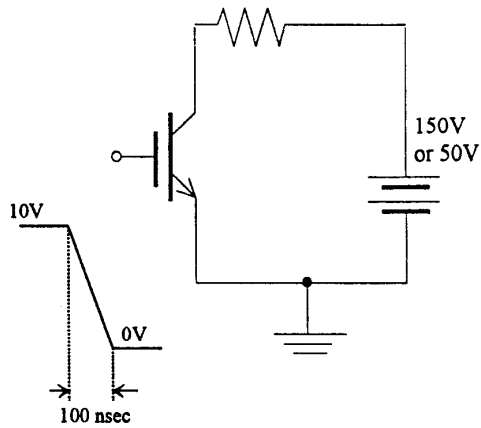


Fig. 6 Simulated circuit.

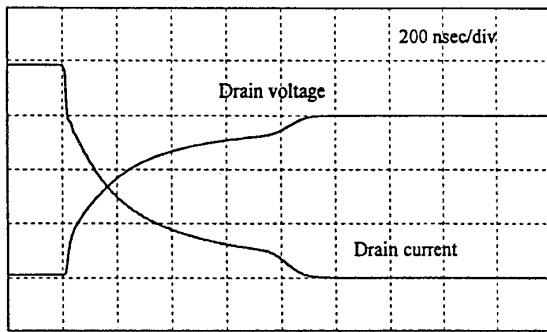


Fig. 7 Simulated turn-off waveform for a lateral IGBT for 150 V of source voltage using the proposed model. Good agreement with results of measurement shown in Fig. 1.

simulated external circuit. The external source voltage was 150 V or 50 V, and the initial drain current was set at 200mA. Fig. 7 shows simulated turn-off waveforms for a lateral IGBT on SOI, using the proposed model. The obtained waveforms for 150 V external voltage source agrees very well with the experimentally obtained waveforms shown in Fig. 1. The simulated waveforms for the 50 V source voltage case have a long tail current and no terrace current appears as seen in Fig. 8. The results also agreed with experimental results shown in Fig. 9.

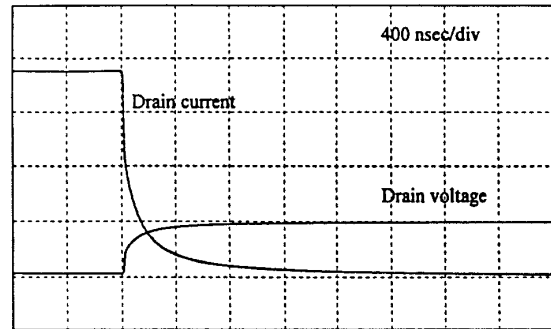


Fig. 8 Simulated turn-off waveform for a lateral IGBT for 50 V of source voltage using the proposed model. Good agreement with results of measurement shown in Fig. 9.

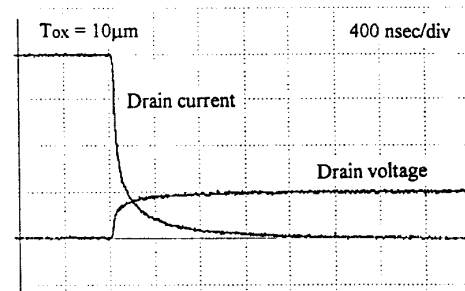


Fig. 9 Experimentally obtained turn-off waveform for 50 V of source voltage.

IV. Application to circuit design

In consideration of a requirement of CAD tools for power ICs, a major advantage of subcircuit modeling in the SPICE simulator is its ability to simulate of large scale circuits including power devices. In this section, as an example, application of the model to an overcurrent protection circuit design is presented.

An overcurrent protection circuit is designed so as to prevent high voltage LIGBTs from destruction when the load resistance is suddenly made short-circuited. A typical overcurrent protection circuit is designed to works as follows. When over current is detected, the gate voltage of

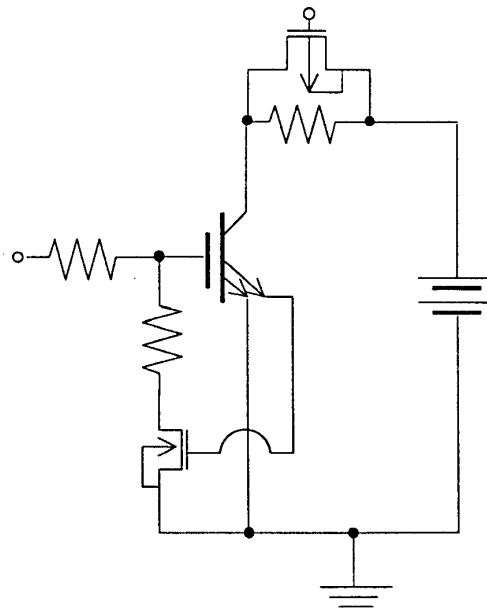


Fig. 10 Simulated overcurrent protection circuit.

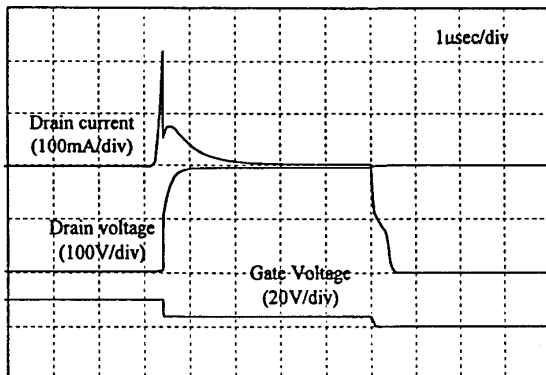


Fig. 11 Simulation result of the circuit of Fig. 10.

IGBTs is immediately reduced to a low value by a prompt protection circuit to reduce conducting current and dissipating power loss. The gate voltage is finally reduced to zero by a CPU or an equivalent function circuit, when the abnormal condition signal is transferred to the CPU. Fig. 10 shows an example of over current protection circuit and Fig. 11 shows a

simulation result of this circuit using the proposed model. The turn-off waveform agreed with experimental result. This result shows the possibility of simulating whole LSI circuits including lateral IGBTs by SPICE simulation using the proposed model.

V. Conclusion

A subcircuit model of lateral IGBT on SOIs is presented. Several example simulations were carried out using the proposed model and they showed good agreement with experimental results as well as with 2-D device simulation results. As an example of application, simulation of an overcurrent protection circuit was presented. These results indicate that subcircuit modeling approach using SPICE simulator can be applicable for a circuit design of power ICs including lateral IGBTs.

Acknowledgment

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References

- [1] Z. Shen and T. P. Chow, "An Analytical IGBT Model for Power Circuit Simulation", Proc. of 3rd ISPSD, pp. 79 - 82, 1991
- [2] Z. Shen and T. P. Chow, "Modeling and Characterization of the Insulated Gate Bipolar Transistor (IGBT) for SPICE Simulation", Proc. of 5th ISPSD, pp. 165 - 170, 1993
- [3] B. Fatemizdeh and D. Silber, "A Versatile Electrical Model for IGBT Including Thermal Effects", IEEE PESC Record, pp. 85 - 92, 1993
- [4] B. Fatemizdeh and D. Silber, "Modeling of LDMOS and LIGBT Structure at High Temperatures", Proc. of 5th ISPSD, pp. 137 - 142, 1994
- [5] I. Omura, N. Yasuhara, A. Nakagawa, and Y. Suzuki, "Numerical analysis of SOI IGBT switching characteristics -- Switching speed enhancement by reducing the SOI thickness", Proc. of 5th ISPSD, pp. 248 - 253, 1993