Thin SOI IGBT leakage current and a new device structure for high temperature operation

Tomoko Matsudai, Yoshihiro Yamaguchi, Norio Yasuhara, Akio Nakagawa
and
Hiroshi Mochizuki

Research & Development Center, Toshiba Corp.
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan
Phone:+81-44-549-2139, Fax:+81-44-549-2259

Abstract

This paper describes and compares the temperature dependence of leakage current and on-state resistance of MOSFETs (Diodes) and LIGBTs on thin SOI. The leakage current decreases effectively as the SOI layer thickness decreases. The forward voltage-drop of IGBTs on thin SOI is not significantly deteriorated at a high temperature, such as 200 ℃. On the other hand, switching speed improves as the SOI layer thickness decreases. Thus, a thin SOI device is a good candidate for high temperature operation.

1. Introduction

Thin SOI technology is of great interest because high-voltage devices can be integrated on the same chip together with CMOS circuitry by simply using shallow trench isolation. The authors have theoretically[1] and experimentally[2] shown that lateral IGBTs fabricated on a thin SOI exhibit high switching speed without the need for any special device design. This means that high-voltage, high-speed output devices can be fabricated on a thin SOI by using conventional CMOS processes without lifetime control.

Recently, the same authors have also experimentally shown[3], for the first time, the advantage of a thin SOI for the high temperature operation of high voltage power devices such as IGBTs. Power ICs[3,4] that operate at 200 ℃ are frequently required in automotive and motor control applications. For example, the switching speed of IGBTs on a 1.5 μm SOI is not deteriorated at a high temperature. The turn-off fall-time was only 360 ns, even at 200 ℃, which was only 50 % larger than that for room temperature. They have found that an SOI thinner than 5 μm is a good candidate for high temperature operation.

The present paper discusses the leakage current and the forward voltage-drop of thin SOI devices. This paper also gives a high breakdown voltage structure on a few micron SOI, which is implementing double implanted resurf layers.

2. Voltage blocking capability at high temperature

2-1. Device structure

Figure 1 shows the cross-sectional view of a lateral IGBT on a thin SOI layer. The SOI wafers were prepared by the silicon wafer direct bonding method[5]. The SOI layer thickness ranged from 1.5 μm to 10 μm on a 2 μm thick bottom oxide film. The high resistivity drift regions were 30 μm to 60 μm in length and the layers were uniformly doped by blanket implants. The n-buffer layer and the p-base layer reached the bottom oxide film when the SOI layer was less than 5 μm.

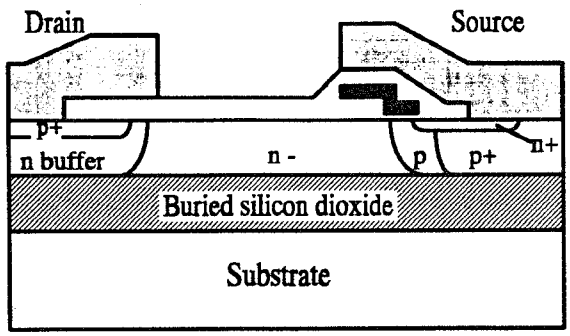

Fig.1 Lateral IGBT structure on 1.5 μm SOI

2-2. Leakage current

Figure 2 shows the temperature dependence of the MOSFET (or diode) leakage current as a function of the SOI layer thickness. The leakage current increases as the temperature increases. It has been found that the leakage current decreases effectively as the SOI layer thickness decreases. The leakage current for a MOSFET on a 1.5 μm SOI was less than 2 nA at room temperature and 100 nA even at 200 ℃. These values were one order of magnitude smaller than those of 10 μm SOI MOSFETs.

Figure 3 shows the leakage current versus the applied voltage for lateral IGBTs and MOSFETs on a 10 μm SOI. These values for IGBTs were two orders of magnitude larger than those for SOI MOSFETs. It has been found that the leakage current voltage curves for IGBTs at room

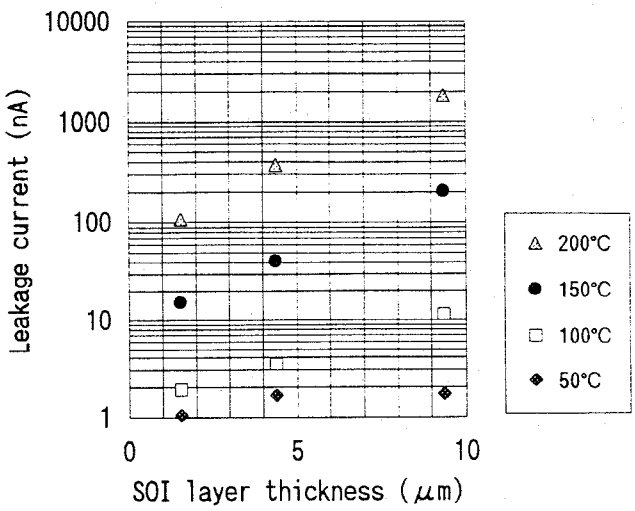

Fig.2 MOSFET leakage current versus SOI layer thickness from 50 ℃ to 200 ℃

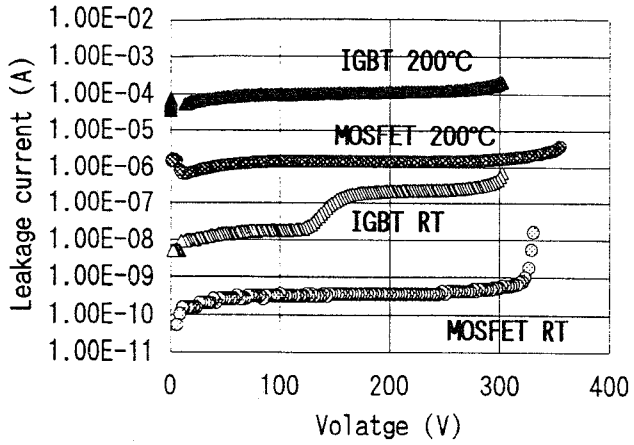

Fig.3 Leakage current versus applied voltage for lateral IGBTs and MOSFETs on 10 μm SOI

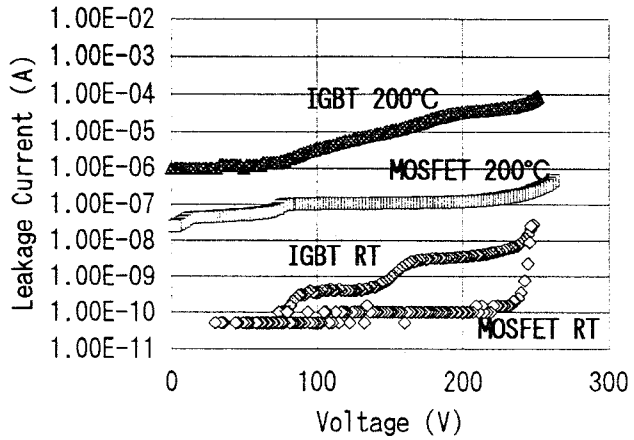

Fig.4 Leakage current versus applied voltage for lateral IGBTs and MOSFETs on 1.5 μm SOI

temperature always have characteristic terrace shapes. The leakage current increased stepwise at almost the same voltage as the applied voltage increased when the SOI layer thicknesses were the same. It has also been found that only the leakage current of 1.5 μm SOI IGBTs increased significantly at 200 ℃ with the applied voltage, as shown in Fig. 4, whereas those of MOSFETs and 10 μm SOI IGBTs did not.

The generation lifetimes, τ_g, were calculated by equating the observed leakage current and the depletion region volume times (n_i/τ_g), and were compared with the recombination lifetime, which were measured from the diode reverse recovery characteristics. Table 1 shows the results. It has been found that the generation lifetimes are more than one order of magnitude larger than the recombination lifetimes. The generation lifetime did not depend on

Table 1

SOI thickness	1.5 μm	5 μm	10 μm
Recombination lifetime	102.2 ns	151.4 ns	235.7 ns
Generation lifetime	3.46 μs	5.34 μs	4.59 μs

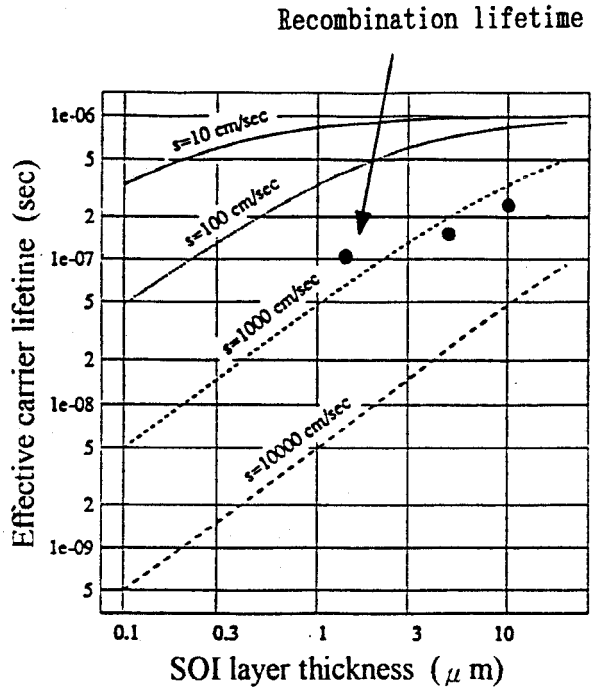

Fig.5 Effective carrier lifetime for thin SOI as a function of SOI layer thickness with surface recombination velocity

the SOI layer thickness, although the recombination lifetime increased with the SOI thickness.

It has been theoretically shown[1] that the surface recombination velocity dominantly determines the recombination lifetime. A plot of the recombination lifetime versus the SOI layer thickness gives information on the surface recombination velocity, as seen in Fig. 5. The estimated surface recombination velocity is 1000 cm/s from Fig. 5.

These results imply that the surface generation velocity must be small, although the surface recombination velocity is large. The recombination lifetime, dominantly determined by the surface recombination velocity, increases with the increase in SOI thickness, although the generation lifetime does not depend on the SOI thickness because it depends on the bulk lifetime. These results show

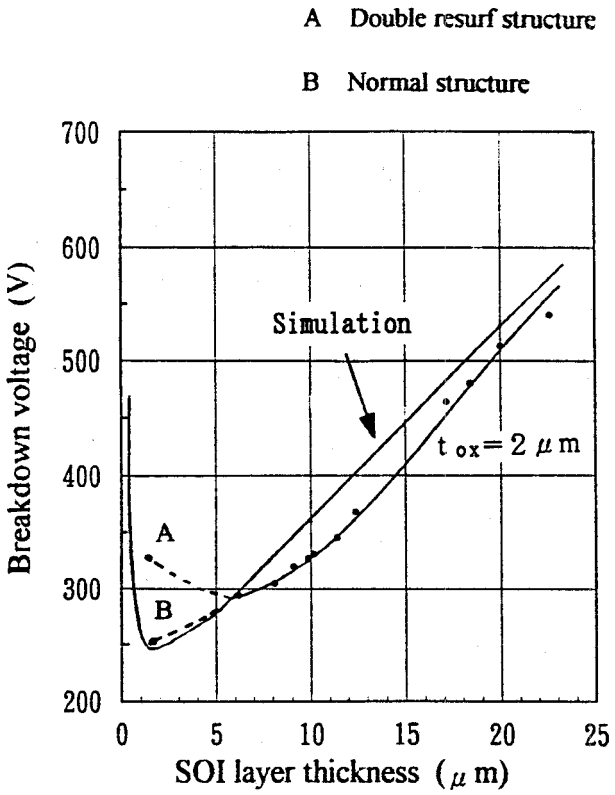

Fig.6 Breakdown voltage as a function of SOI layer thickness with 2 μm buried oxide

that low leakage current and high switching speed are simultaneously realized by the devices on a few micron SOI.

3. Increasing the breakdown voltage of devices on a thin SOI

A few micron thick SOI is a good candidate for double injection devices such as IGBTs because both a low forward voltage and high-speed switching are simultaneously realized. However, it has been theoretically shown that the breakdown voltage depends on the SOI layer thickness and takes its minimum at a few microns in SOI layer thickness, as seen in Fig. 6. This paper proposes an effective method to increase the breakdown voltage of devices on a few micron SOI.

Figure 7 shows the proposed structure of implementing double implanted resurf layers. The measured breakdown voltage of normal SOI diodes on a 1.5 μm SOI was 250 V, which agreed with the calculated breakdown voltage. On the other hand, the double resurf structure had a 330 V breakdown voltage on the same 1.5 μm thick SOI. This value is

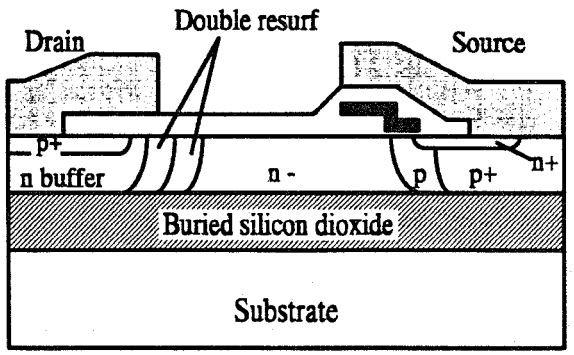

Fig.7 LIGBT structure on 1.5 μm SOI with double resurf layers

larger than the normal 1.5 μm SOI diodes by 80 V. Figure 8 shows the calculated potential distribution of the double resurf diode using a 1.5 μm thick SOI. A 300 V positive voltage was applied to the cathode layer with the substrate having the earth potential, and equi-potential lines were drawn with a 16 V step. The highest electric field appeared at the edge of the n-buffer layer in case of the normal diode. A high breakdown voltage was obtained for the double resurf device, because the high electric field was relaxed by the double resurf implants.

4. The temperature dependence of the static electrical characteristics

Figure 9 shows the on-state resistance and area product of IGBTs as a function of the temperature. The measured current voltage relations for a 1.5 μm SOI IGBT were quite good, when the surface recombination velocity was less than 1000 cm/s. The forward voltage was 2.8 V at 100 A/cm^2 current density for 12 V gate voltage at room temperature. A thin SOI IGBT had the same temperature dependence as that of a thick SOI IGBT,

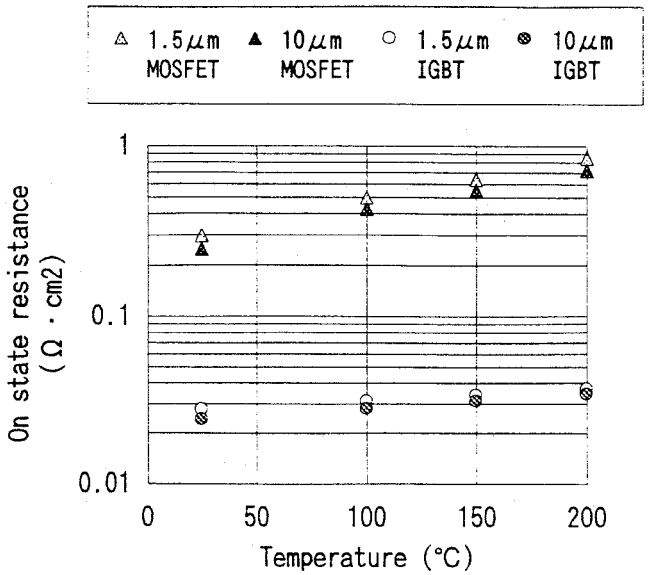

Fig.9 Forward voltage-drop as a function of temperature for IGBT and MOSFET

although the drift region resistance was higher for the thin SOI. The temperature dependence of the SOI IGBT on-resistance was relatively small, as compared with that of an SOI MOSFET. The large temperature dependence of SOI MOSFET on-resistance is also shown in Fig. 9. That reason is that the mobility decreases as the temperature increases. Furthermore, the on-resistance of SOI MOSFETs increased by 20 % as the SOI thickness decreased from 10 μm to 1.5 μm, although the blanket ion implant doses for the drift layers were the same. The reason is that the electron mobility in the drift layer decreases as the SOI thickness decreases and the impurity concentration increases.

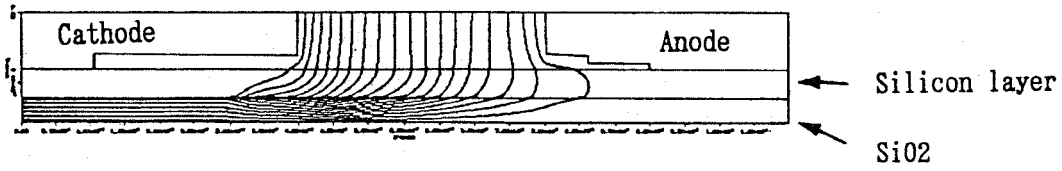

Fig.8 Calculated potential distribution for double resurf structure

Conclusion

A thin SOI of less than 5 μm is suitable for simple dielectric isolation of power ICs. The electrical characteristics of thin SOI IGBTs from 25 ℃ to 200 ℃ have been shown. An especially thin SOI is a good candidate for high temperature operation. The forward voltage-drop was only slightly affected by decreasing the SOI thickness. The leakage current for a 1.5 μm SOI device was very small even at high temperature. Furthermore, the breakdown voltage was much improved using double resurf layers. These results indicate the possibility of a great extension in the application of thin SOI power ICs.

Acknowledgments

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