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500V Three Phase Inverter ICs Based on a New Dielectric Isolation Technique

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Abstract

500V three-phase inverter ICs for DC brushless motor drives has been developed, for the first time, using a new dielectric isolation method based on silicon wafer direct-bonding(DISDB). The new DI method has an advantage that it is completely compatible with conventional junction isolation and Resurf principle.

600V high speed lateral IGBTs has been developed without using carrier lifetime control process. Thus, the developed ICs can be fabricated using only conventional LSI processes.

The developed 500V inverter ICs operate at 16kHz PWM frequency, and realize compact low noise DC brushless motors when installed inside the motor.

A new shortcircuit protection function is also proposed.

1. Introduction

500V three-phase inverter ICs for DC brushless motor drives, which integrate six lateral IGBTs and 600 BiCMOS logic devices, have been developed, for the first time, by using new dielectric isolation (DI) technique. A DI technique has conventionally been used to prevent interactions among the devices in high voltage ICs above 200V. This paper proposes a new DI technique, which merges dielectric isolation and junction isolation(JI). Low voltage BiCMOS logics can be formed by conventional JI processes in a single DI island. The conventional DI technique(EPIC) is not suitable for low voltage bipolar logics because of relatively large area consumption. The proposed new DI has further advantages that resurf principle can be applied to high voltage devices and that well matured junction isolated analog logic libraries can be simply utilized.

High speed lateral IGBTs have been developed without introducing lifetime killers. Thus, the developed high voltage power IC processes do not include a lifetime reduction process and are highly compatible with those of conventional LSI.

2. SOI wafer fabrication and device isolation

Dielectric isolation is inevitable for isolating high voltage double injection devices, which are indispensable output devices for high voltage power ICs. If IGBTs are simply isolated from each other by the junction isolation method, an IGBT cannot maintain its blocking capability when the neighboring IGBT is in its on-state. Figure 1 shows this example, where three 500V lateral IGBTs were fabricated by the conventional JI method. Figure 2 demonstrates that the drain current flows in an IGBT even in the off-state and the IGBT loses its blocking capability if the neighboring IGBT is in its conduction state. The amount of current flowing in the IGBT depends on how much current is flowing in the neighboring IGBT and also on the carrier lifetimes of the high rsistivity layers.

Figure 3 shows a developed fabrication process of new DI wafers, merging DI and JI techniques, based on silicon wafer direct bonding (SDB) [1]. First, a thermally oxidized high resistivity P^- wafer is directly bonded to another substrate wafer. The thickness of the P^- layer is adjusted by conventional lapping technique. Then, N^- layer is epitaxially grown after buried N-diffusion layer formation on a P^- layer. V-grooves are formed and planarized by polysilicon filling and grinding, after a thick thermal oxide film is grown. Grinding process is stopped by the thick oxide film so that the epitaxial N^- layer automatically remains.

Figure 4 shows a cross section of a new DI wafer, showing merged DI and JI technique. A number of logic bipolar and CMOS can be fabricated in single DI

island by the conventional junction isolation method. This makes it possible to utilize well matured conventional analog and digital logic libraries.

3. High speed lateral IGBTs and diodes

Lifetime control processes have conventionally been adopted to achieve high switching speeds in discrete power devices. However, lifetime control processes have not been adopted in conventional IC fabrication processes. Thus, our principle is to attain high speed switching in high voltage output devices by optimizing device structure without introducing lifetime control processes.

A schematic cross section for a developed high speed 600V lateral insulated gate bipolar transistor(LIGBT), fabricated on the new DI wafer, is shown in Fig.5. A new anode structure, characterized by an additional N^+ region formed in a shallow P-drain layer, realizes a short fall time, such as 0.15μs, without lifetime control, as is shown in Fig.6 [2].

This new structure behaves exactly in the same way as conventional anode short structure in the high injection condition. However, in the low injection condition, the structure is the same as ordinary LIGBTs. Thus, low forward voltage is maintained for low current density level, while attaining a high switching speed.

I-V characteristics and switching speed is influenced by the location of N^+ region in the drain layer as well as the boron dose in the shallow P-drain layer beneath the N^+ region. Figure 7 shows how the relation between the drain current density for 3V forward voltage and fall time is changed by the location of the N^+ region in the P-drain layer.

This new structure was also applied to realize high speed switching in the free wheeling diodes (FWDs).

A combination of SIPOS resistive field plate and polysilicon field plates were adopted to prevent breakdown voltage reduction caused by metal interconnections over high voltage junctions.

4. 500V 1A Inverter ICs

Figure 8 shows a die photograph of a fabricated 500V-1A inverter IC, designed to control a three phase DC brushless motor, integrating six LIGBTs, six FWDs and 600 low voltage BiCMOS logics. Both upper and lower gate drive circuits are controlled by CMOS logic timing circuits which accept signals from Pulse-Width-Modulation (PWM) circuit and protection circuits(over temperature, over current self-protection etc.). The detailed circuit functions are described in the following section.

4.1 Circuit functions

A block diagram of the circuit is shown in Fig.9. 500V 1A LIGBTs, FWDs, gate drivers for high side IGBTs and bootstrap diodes are dielectrically isolated by V grooves.

Conventionally, PWM control is performed in the low side IGBTs. However, in our circuit, PWM control is performed in the high side IGBTs and not in the low side IGBTs. This was found to be strongly effective to reduce the capacity of bootstrap capacitor, because the capacitor was charged up during the PWM operation.

Conventional over temperature and over current protection functions were adopted and implemented.

This IC operates at PWM frequency of 16 kHz. The PWM frequency is above the audible range, so that low noise motor operation was achieved. Figure 10 shows typical switching waveforms and output current of fabricated inverter ICs. The developed new ICs can be installed inside DC brushless motors, thus realizing high system performance and size reduction.

4.2 New protection function --- shortcircuit protection

Conventional over current protection circuits are slow, since they require current sensing resistors and processing logics, resulting in a long feedback path. Thus, they are not adequate for shortcircuit protection. We propose a new device structure[3] and a high speed feedback protection method for such purpose.

New method detects an abnormally large voltage drop in the channel instead of the drain current and shuts off the device. Figure 11 shows the new lateral IGBT, which has a floating source layer. The potential of the floating source layer is the same as that of the N- layer near the channel and increases linearly with the increase in the drain current.

Figure 12 shows the relation between drain current and the measured voltage of the floating source. It is difficult to know the absolute current value, since the channel resistance depends on the applied gate voltage.

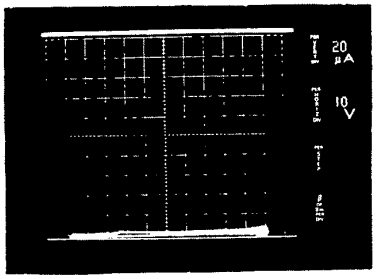
However, this feature is sufficient for shortcircuit protection. The shortcircuit protection is activated when the floating source potential exceeds 5 or 10V. Figure 13 shows a CMOS circuit detecting the floating source voltage. Figure 14 shows actual operation waveforms of the protection function.

5. Conclusion

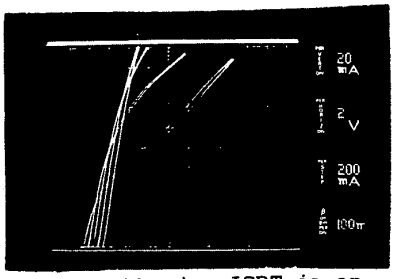
500V three-phase inverter ICs for DC brushless motor drives have been developed, for the first time, using a new dielectric isolation method based on silicon wafer direct-bonding(SDB). The new DI method has advantages that resurf principle can be applied to high voltage devices and that well matured junction isolated analog logic libraries can be simply utilized.

High speed lateral IGBTs were developed without introducing lifetime killers. Thus, the developed high voltage power IC processes do not include a lifetime reduction process and are highly compatible with those of conventional LSI.

The developed 500V inverter ICs operate at 16kHz PWM frequency, and realize compact low noise DC brushless motors when installed inside the motor.



All IGBTs are off.



Neighboring IGBT is on.

Fig.2 Drain current vs. Drain voltage. IGBT loses its bolcking capability when neighboring IGBT is on.

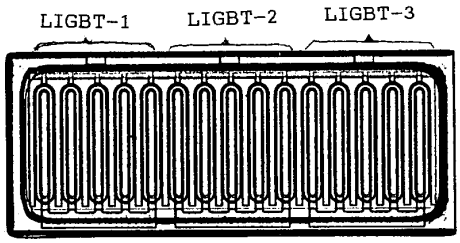


Fig.1 Junction isolated three lateral IGBTs

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[2]Y.Yamaguchi et. al., SSDM'90, p.677.
[3]USP4,994,904
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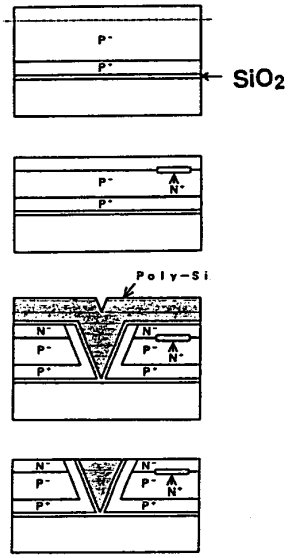

Fig.3
Fabrication processes of new DI(DISDB) wafers

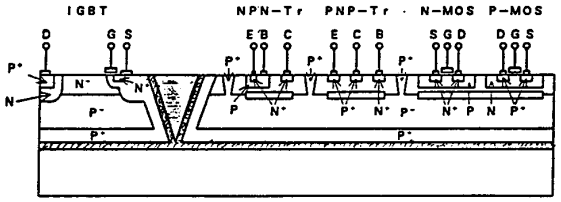

Fig.4 Cross section of new DI wafer

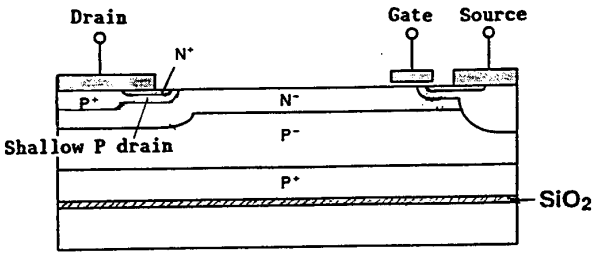

Fig.5 Cross section of new LIGBT

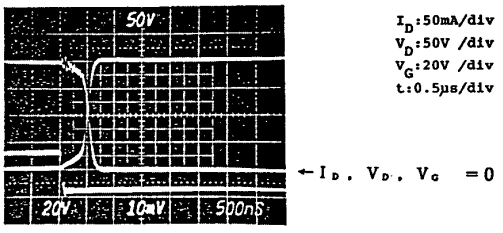

Fig.6 Turn-off waveforms of new IGBT

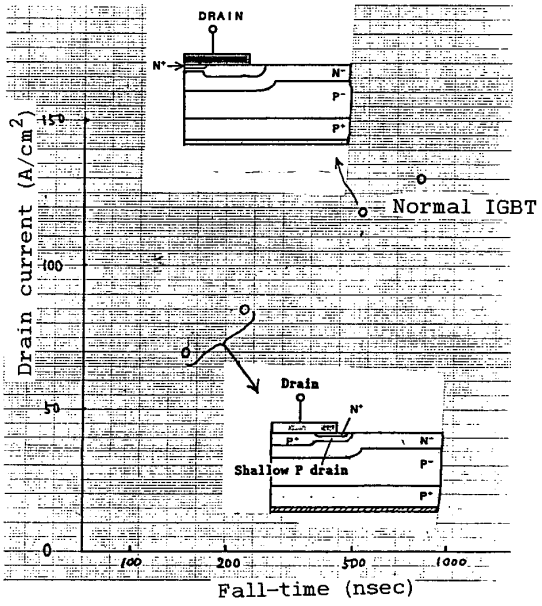

Fig.7 Trade-off relation between drain current for 3V forward voltage and fall-time.

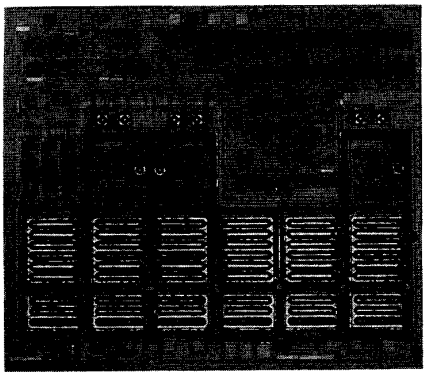

Fig.8 500V 1A inverter IC chip

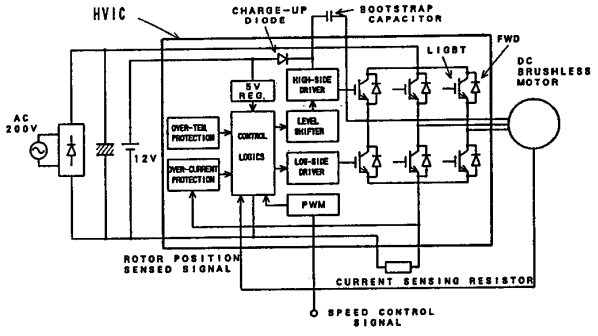

Fig.9 Bolck diagram of inverter IC

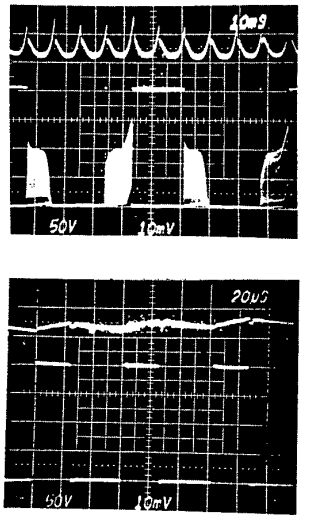

Fig.10 Switching waveforms of typical inverter operation

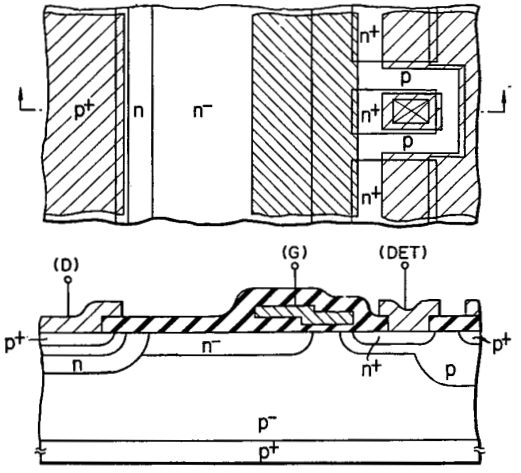

Fig.11 New IGBT with voltage sensing terminal
The voltage sensing terminal DET is formed on a floating N^+ region.

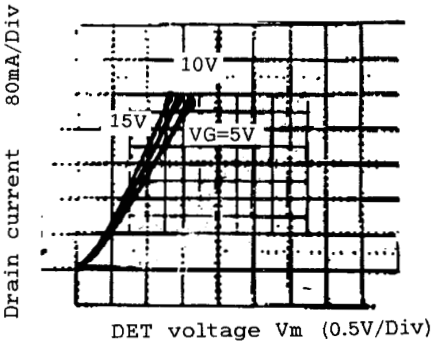

Fig.12 Drain current vs. terminal voltage of voltage sensing.
Good linear relationship is seen between the drain current and the DET terminal voltage Vm.

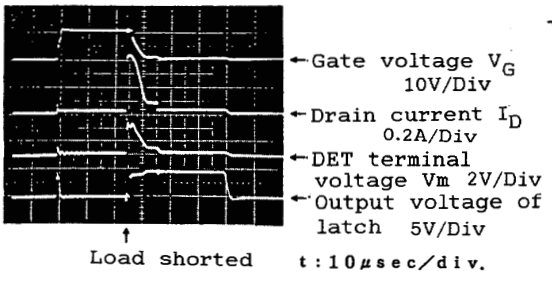

Fig.14 Typical operation of shortcircuit protection

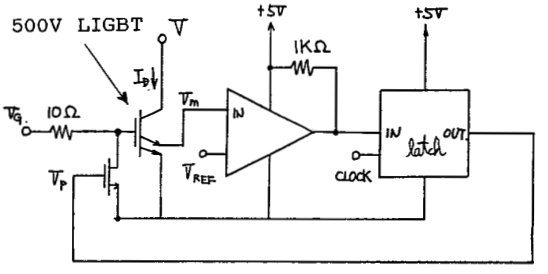

Fig.13 CMOS circuit for shortcircuit protection