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A Study on IGBT's Steady State SOA with Newly Developed Simulation

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ABSTRACT

The steady state SOA of a 600V vertical n-ch IGBT was studied by 2D device simulator TONADDE II C taking into account impact ionization effect. It was shown that IGBTs have a large SOA beyond the critical limit for n-p-n bipolar transistors. To clarify this, the relation was investigated between current density distributions and the electric field distribution in the device. It was found that positive and negative charge plasma are distributed under the MOS gate in such a way that the high electric field in the depletion layer is relaxed and the impact ionization is reduced.

1. INTRODUCTION

n-ch Insulated Gate Bipolar Transistors (IGBTs) combine the n-channel type MOSFETs with p type drains. IGBTs have achieved good characteristics: easy gate controllability, low on-resistance, high voltage capability, and high speed switching. In addition, it has a very large Safe Operating Area (SOA) [1-4] compared with n-p-n bipolar transistors, whose power dissipation doesn't exceed a particular value, $2x10^5 W/cm^2$[5]. This limit is caused by avalanche injection.

However, there is a weak point in the IGBT. It includes a parasitic thyristor part, because of the additional p-drain. If this parasitic thyristor is once latched-up, the IGBT loses insulated gate controllability. The SOA is defined as the area where the IGBT does not lose its gate controllability[6].

Then, the authors tried to analyze the SOA for on IGBT in the steady state. The purpose was to clarify why the IGBT has a large SOA, compared with the bipolar transistor. The I-V characteristics were simulated with and without the carrier generation effect. The SOA analysis has rarely been carried out, including the generation effect, because of the limit to the computer capability, especially for steady state. The next section gives an outline of the authors' simulation method and calculation condition. Section 3 shows results and discusses them. Finally, the conclusions are presented.

2. SIMULATION

The 2D device simulator TONADDE II C adopts a coupled method and treats variables in Newton's iteration scheme[7]. For the SOA analysis, this effect must be considered. The following well-known impact ionization formula was used[8];

$$G = \frac{1}{q}\left(\alpha_n |\vec{J_n}| + \alpha_p |\vec{J_p}| \right),$$

$$\alpha_i = A_i \exp\left(- b_i / |\vec{E}|\right) \qquad (i = n, p). \qquad (1)$$

Here, J_n and J_p are electron and the hole current densities, respectively. $|\vec{E}|$ is the absolute value for the electric field. "A" and "b" are certain constants and are given as $A=3.8x10^6 cm^{-1}$, $b=1.75x10^6 Vcm^{-1}$ for electron and $A=2.25x10^7 cm^{-1}$, $b=3.26x10^6 Vcm^{-1}$ for hole.

The device and circuit model is shown in Fig.1. A 600V vertical type IGBT with an n-buffer was studied. Electron and hole carrier lifetimes in n-base were assumed to be 4μs and 1μs, respectively. The gate

voltage was 20V.

When the simulation were carried out, the following methods were used. First, the I-V curve was calculated without the generation effect and the results at each point were saved for later use. Subsequently, the I-V curve was calculated with the generation effect, using those results as initial conditions. The effect was introduced time-dependently and steady state solutions were obtained by putting time forward to infinity. Practically, when the drain current is sufficiently constant, it is regarded as steady state.

In the simulation, temperature was fixed at 300K.

3. RESULTS and DISCUSSIONS

The I-V curve results are shown in Fig.2. The solid line shows the result, neglecting the impact ionization formula. The broken line shows the result considering the generation effect. The drain current density is significantly increased, due to impact ionization, for drain voltages over 400V and the latch-up phenomenon occurs at 557V. At this point, the drain current density diverged and the simulation could not be carried out. The calculated power dissipation for this point was $9.5 \times 10^5 W/cm^2$. This value agrees very well with the experimentally obtained critical power limit[3]. Apparently, this breakdown point exceeds the limit for n-p-n bipolar transistors indicated by the dotted line.

To clarify this large SOA, the authors checked the distributions for carrier densities, electric field and current densities in the device. Carrier densities and potential distributions at 556V drain voltage are shown in Fig.3. Electrons were injected from the MOS gate to the n-base by a localized path in the depletion layer. Holes were injected from drain and distributed due to charge neutrality. In contrasted to electrons, holes are distributed more uniformly in the n-base region. Figure 4 shows carrier generation density distribution. Most of the carrier generation occurred in the n-base region. Especially, the maximum point exists in the main junction boundary, where the electric field is maximized. From those results, one of the keys for

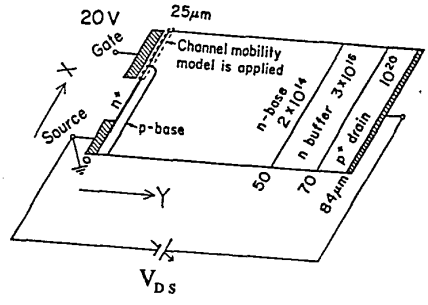


Fig.1. Device structure and external circuit.

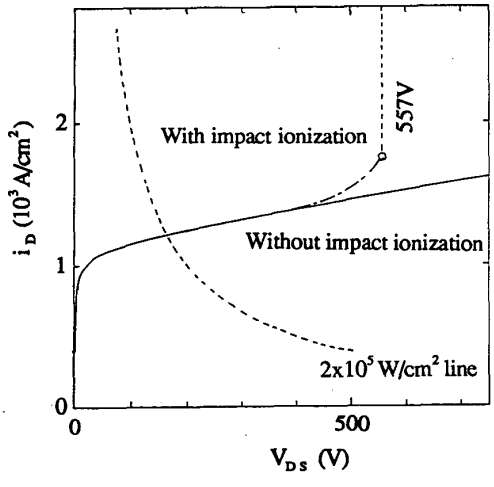
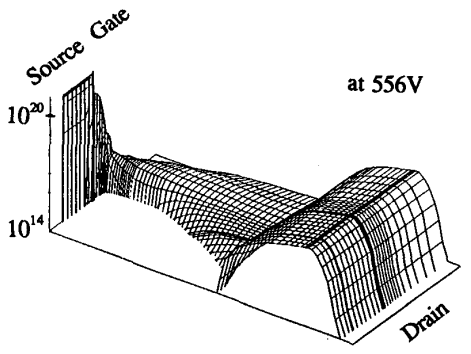


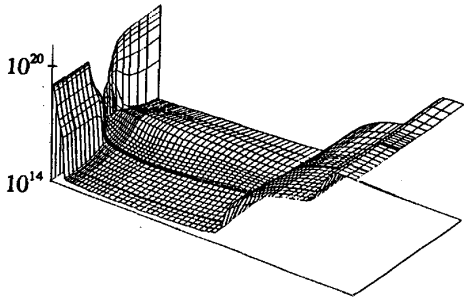
Fig.2. I-V characteristics.

clarifying the SOA is analyzing the characteristics in the depletion layer.

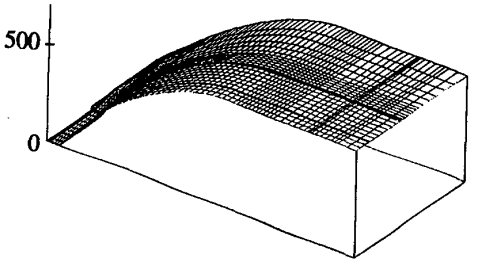
Figure 5 shows the distributions for y-components in electron and hole current densities along the main junction boundary. Here, x-components for current densities are small and negligible. Individual currents flow through the localized region under the MOS gate. The electric field y-component distribution along the main junction boundary is shown in Fig.6. Also, the x-component is negligible. Comparing Fig.5 with Fig.6, peaks exist at different positions. Currents flow mainly in the low electric field region, and are small in the high electric region[4]. Whenever electrons are injected into the n-base through the MOS gate, the holes



(a) Electron



(b) Hole



(c) Potential

Fig.3. Carrier density and potential distributions.

are also injected from the p-drain, to satisfy charge neutrality. Conductivity modulation occurs and the internal high electric field disappears. If the maximum current is limited by avalanche injection, and if avalanche injection occurs under the p-base, it is possible that apparent power dissipation exceeds the transistor theoretical limit.

Breakdown voltage in the n-base was estimated as follows[4,9];

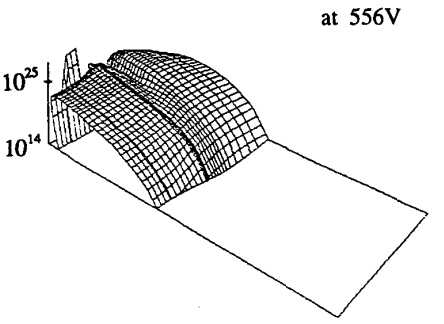


Fig.4. Carrier generation density distribution.

$$BV = 60(E_G/1.1)^{1.5}\left(\frac{N^+}{10^{16}}\right)^{-\frac{3}{4}},$$

$$N^+ = N_D + \frac{I_D - (1+\alpha)I_{ch}}{qv_sS}, \qquad (2)$$

where E_G is the silicon energy gap, N_D the donor concentration, S the effective p-base area, I_{ch} the channel electron current, v_s the saturated hole velocity and α the factor which takes into account the enhanced hole current density under the gate electrode due to the

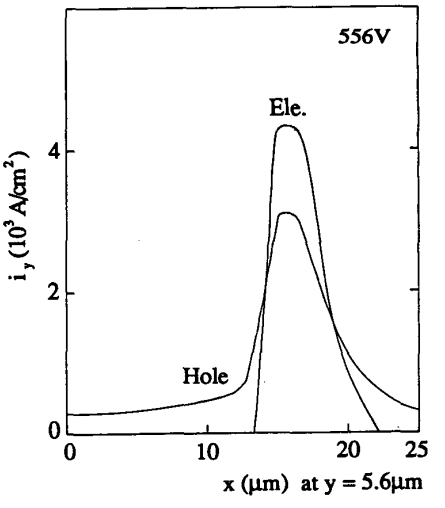


Fig.5. Current density y-components along main junction.

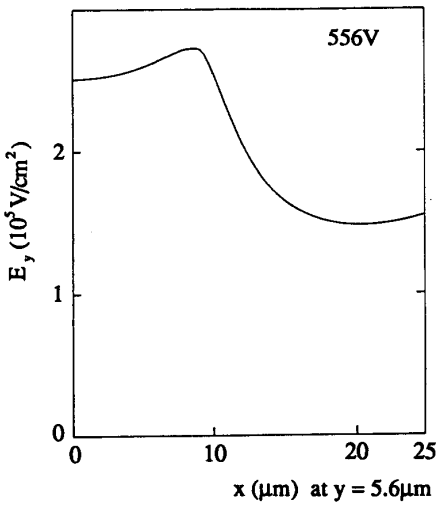


Fig.6. Electric field y-components along main junction.

existence of electron-hole plasma.

Equation (2) essentially used for estimating the static breakdown voltage in the n-base. This formula can be applicable for analysing the steady state SOA by following reason. While channel electron current exists, the hole current density flowing under the p-base is lower than the average current density, because most of the current flows in the high conductivity area under the MOS gate where electrons and holes exist. And the effect of impact ionization by hole is small[10]. The situation under the p-base is regarded as the quasi-static one.

Figure 7 shows generation density distribution along the main junction boundary. There are two peaks, corresponding to those for current densities and electric field, respectively. Both peaks are the same order. Avalanche injection occurs both under the p-base and in the region where currents flow, equally. Thus, it has sufficient basis that equation (2) can be used for estimating the SOA of the n type IGBT. In contrast, equation (2) is not suitable for the p-ch IGBT, because the electron current flows under the n-base and the effect of impact ionization by electron is large, compared to hole[11]. Static breakdown voltage equation is not valid for p-ch IGBT SOA prediction.

In case of the bipolar transistor, electrons and holes fill the collector-base junction and deeply enters into the collector region while the high injection state is realized. The strong electric field in the depletion layer is moved to the collector N^--N^+ junction by the base pushout effect. Considering n-p-n transistors, collector current is carried by only electrons and the high electric field is created by negative electron charges. In contrast to IGBTs, no holes are injected into the region where the high electric field exists and, thus, the high electric field is not relaxed. Especially, avalanche injection easily occurs in the n-p-n transistor, because impact ionization rate for electrons is larger than holes.

In the IGBT turn-off process, all of the current is carried by holes after the channel electron current ceases. It is well assumed that the SOA in the turn-off process is smaller than the steady state, because the hole current is the cause for parasitic thyristor latch-up. One of authors and co-workers discussed a large SOA

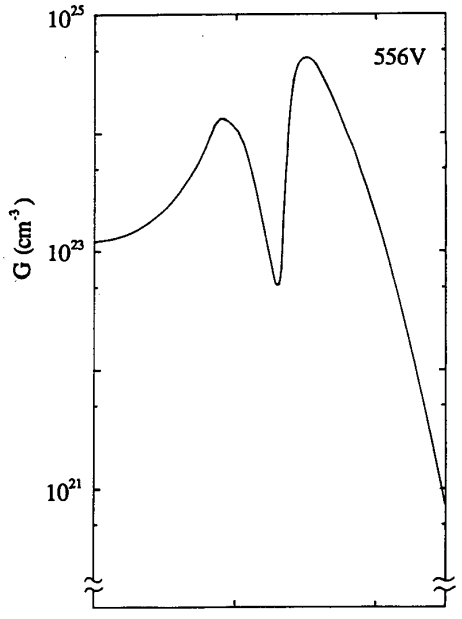


Fig.7. Carrier generation density along main junction.

for IGBT in the turn-off process simulation[4]. It was shown that the electron current existence, after the drain voltage has recovered, is effective for a large SOA in IGBT.

4. CONCLUSIONS

A large SOA for IGBT, compared with bipolar transistors, was investigated. It is important for a large SOA that positive and negative charges be distributed in the device, because impact ionization was reduced by the conductivity modulation.

In the n type IGBT, equation (2) is applicable for estimating breakdown voltage, because the avalanche injection equally occurs both under the p-base region and in the region where most of current flows.

The great difference between conventional double injection devices and IGBT is that the electron injection is controlled by the MOS gate. Thus, current concentration is prevented, in spite of using a double injection device, as long as parasitic thyristor latch-up is suppressed.

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