Proceedings of 1992 International Symposium on Power Semiconductor Devices & ICs, Tokyo, pp. 272-277

SIMULATION OF A 700 V HIGH-VOLTAGE DEVICE STRUCTURE ON A THIN SOI
----- SUBSTRATE BIAS EFFECT ON SOI DEVICES -----

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Abstract

This paper shows for the first time that a 700 V breakdown voltage is easily realized in a uniformly doped thin SOI structure without using a complicated impurity profile when a SIPOS resistive field plate is utilized. The electric field inside the thin SOI is uniformly distributed by the influence of the SIPOS layer when they are closely located to each other. This paper also shows the effects of substrate bias on the SOI device characteristics. Relatively thick SOI devices become free from substrate bias effects, since the negative substrate bias is shielded by a created p-channel on the bottom oxide.

1. INTRODUCTION

The two major techniques for device isolation are pn junction isolation(JI) and dielectric isolation(DI). Junction isolation is not suitable to isolate thyristor-like devices such as IGBTs and GTOs. Dielectric isolation is a reliable technique for high voltage power ICs, especially those ICs with breakdown voltages above 500 V.

In conventional DI methods, thick silicon islands have been required to attain high breakdown voltages. Recently, SOI technology has greatly advanced since the invention of the silicon direct-bonding technology(SDB)[1]. Research activities for the application of SOI to high voltage power ICs have gained attention. This is because device isolation can be easily achieved by simple processes such as trenches or even LOCOS if the thickness of the SOI layer is sufficiently thin.

High voltage SOI technology is classified into two methods. The first is similar to conventional EPIC. A thick SOI layer is separated by V-grooves, and all the applied voltage is sustained by the depletion layer inside the isolated silicon islands. The authors have already developed the DISDB technique in 1986[2], and have applied it to 500 V 1 A inverter ICs[3].

Although the V-groove technique can separate thick silicon layers, the V-groove regions are large compared with the device regions, and this technique cannot pack devices with a high density. Better ideal isolation techniques are trenches or LOCOS. However, the available trench depth is limited to below 15 μm. LOCOS is applicable to SOI layers less than 1 μm. Thus, it is necessary to obtain high breakdown voltages with thin SOI layers.

The second method is to attain a high voltage, taking advantage of the bottom oxide layer, and applying a high voltage to both the depletion layer and the bottom oxide.

It has been experimentally verified that a 650 V breakdown voltage can be achieved in lateral devices on a 14 μm thick SOI with a 3 μm thick bottom oxide[4]. The individual

devices were isolated by trenches.

On the other hand, it has been shown[5] that an extremely thin SOI layer such as 1000 Å is also a good candidate for high voltage ICs. However, the proposed thin SOI structure requires a complicated impurity profile.

The present paper proposes a simple high voltage device structure on a very thin SOI. This paper also gives the results of analyzing the substrate bias effects on the SOI device characteristics.

2. HIGH VOLTAGE DEVICES ON AN EXTREMELY THIN SOI

2.1 Device structure

Figure 1 shows a proposed high voltage diode structure. The device is characterized by a 1000 Å silicon layer on a 3 μm thick bottom oxide film and a SIPOS resistive field plate. The distance between the anode and the cathode is 70 μm. The silicon layer is a uniformly doped n-type high resistivity layer. There are polysilicon field plates in the anode and the cathode regions to relax the electric field in the silicon layer.

2.2 Calculated device characteristics

Calculations were carried out by applying a positive high voltage to the cathode layer with the substrate of earth potential. All of the vertical voltage was applied across the bottom oxide film under the cathode layer, because the n+ region reache the oxide. A 3 μm thick bottom oxide film is sufficient for high voltage, because the critical electric field for oxide breakdown is greater than that for silicon.

Figure 2 shows the calculated electric potential distribution for the diode by a device simulator TONADDEIIB[6]. The thickness of the oxide layer between the SIPOS and the silicon layers was chosen to be 1 μm for the initial series of calculations. In the figure, a 300 V positive voltage was applied to the cathode layer, and the equi-potential lines were drawn with a 20 V step.

Figure 3 shows the high electric field points of the calculated device. In the figure, the highest electric field appeared at the point marked A near the edge of the n+ junction.

The breakdown voltage depends on the impurity dose of the silicon layer, as shown in Fig.4. The highest breakdown voltage can be realized by a SIPOS resistive field plate and an optimized uniform silicon layer impurity dose. The breakdown voltage increased with an increase in the silicon layer impurity dose. However, if the impurity dose is excessively high, the depletion layer does not spread throughout the silicon layer, and breakdown occurs at a lower voltage at point B. The obtained highest breakdown voltage was 400 V for the case of a 1.6×10^{17} cm^{-3} SOI layer impurity dose.

The electric potential inside SIPOS is uniformly distributed due to the nature of SIPOS itself. However, this was not reflected in the calculated electric field distribution in the thin silicon layer. This is because the oxide film between SIPOS and the silicon layer was too thick as compared with the silicon layer thickness. Thus, a next series of calculations were carried out using a thinner oxide film thickness between SIPOS and the silicon layer.

Figure 5 shows the calculated electric potential distribution for one of the optimized diodes. The silicon dioxide film between SIPOS and silicon was 1000 Å. A 700 V positive voltage was applied to the cathode layer. The electric field inside the silicon layer was forced to be aligned with that of

SIPOS, and was uniformly distributed. A 700 V breakdown voltage was achieved for a silicon layer impurity dose of 1.6×10^{17} cm^{-3}. And breakdown was observed at point B in Fig.3.

Figure 6 shows the breakdown voltage dependence on the oxide film thickness between SIPOS and the silicon layers. The silicon layer impurity dose was kept at 1.6×10^{12} cm^{-2}. The breakdown voltage can be greatly increased with a decrease in the oxide film thickness between SIPOS and the silicon layers. This is true especially for thicknesses of less than 0.2 μm.

3. PREDICTED MOSFET CHARACTERISTICS ON A VERY THIN SOI

The proposed diode structure can be modified to form a high voltage MOSFET or IGBT. Figure 7 shows the structure of a high voltage lateral MOSFET, which has exactly the same dimensions and doping profile except for the drift region length of 55 μm and an added source layer and gate electrode. Figure 8 shows the calculated current-voltage characteristic for the four different substrate potentials. The calculated on-resistance and area product, 0.39 Ωcm^2, is sufficiently small even for extremely thin SOI MOSFETs, when the substrate bias is 0 V. This is because the optimum total impurity dose in the SOI layer takes around the same value regardless of the thickness of the SOI layer, following the Resurf principle.

It has been found that the on-resistance is greatly influenced by the substrate bias, as seen in the figure. This is because a part of the N-drift region is depleted if the substrate is negatively biased against the source electrode. Figure 9 show a three dimensional electron density distribution when the substrate bias is -100 V. It is seen that the N-drift region is mostly depleted.

4. EFFECTS OF SUBSTRATE BIAS ON THE SOI DEVICE CHARACTERISTICS

A negative substrate bias generally increases the on-resistances of very thin SOI MOSFETs. However, if the SOI layer is thicker than the effective inversion layer thickness, it has been found that the substrate bias can be dynamically shielded by creating a p-channel on the bottom oxide.

Figure 10 shows that the substrate bias is shielded by the bottom p-channel and that most of the SOI layer remains undepleted for an IGBT on a 15 μm thick SOI, as shown in Fig.11. This means that relatively thick SOI MOSFETs can be used as high side switches. Moreover, a thyristor-like device, such as IGBTs, is completely free from substrate bias effects due to the carrier plasma, and has the same current-voltage curve regardless of the substrate bias level. Figure 12 shows that the calculated current-voltage curve of an IGBT on a 15 μm thick SOI does not depend on the substrate bias.

CONCLUSION

It has been shown that breakdown voltages exceeding 700 V can be obtained by a 1000 Å thick SOI using a 3 μm thick bottom oxide film and a SIPOS resistive field plate. The negative substrate bias on the SOI device is shielded by the effective inversion layer on the bottom oxide. High voltage functions can be implemented in VLSIs with completely compatible processes. This will lead to wider application fields of VLSIs on SOI.

ACKNOWLEDGMENT

The authors wish to thank Mr.F.Umibe for reviewing the original manuscript, and suggesting revisions in its English.

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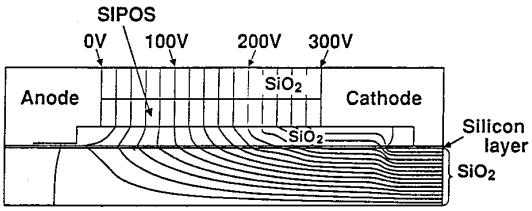


Fig.2 Calculated potential distribution for a non-optimized diode with a 1000 Å thick SOI and a 3 μm thick bottom oxide except for a relatively thick oxide film between SIPOS and the silicon layer (300 V case)

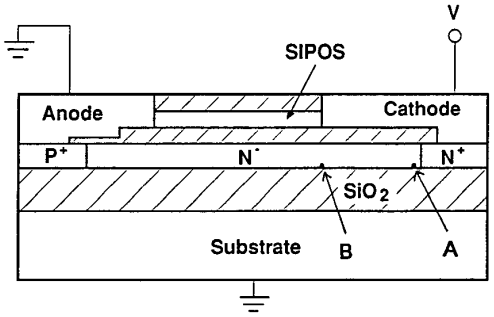


Fig.3 High electric field points of the calculated device

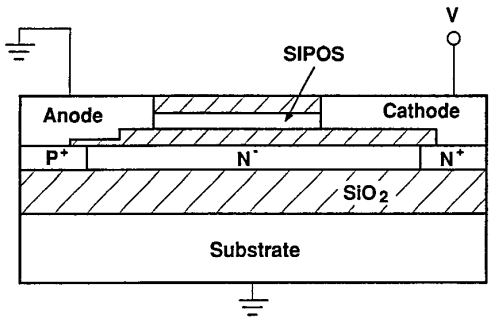


Fig.1 Proposed high voltage diode structure

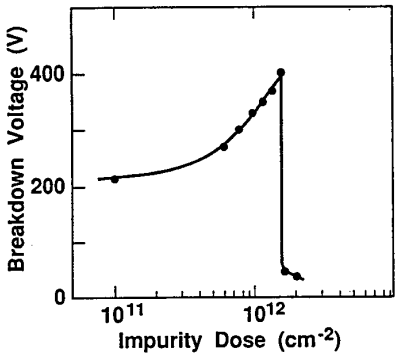


Fig.4 Breakdown voltage vs.impurity dose for the SOI layer

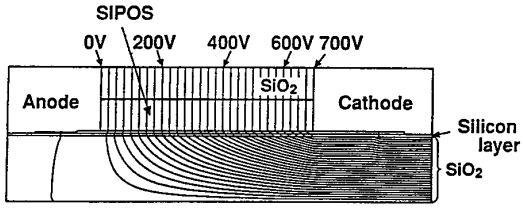


Fig.5 Calculated potential distribution for an optimized high voltage diode (700 V case)

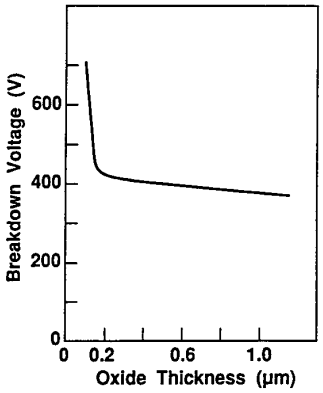


Fig.6 Breakdown voltage vs.oxide film thickness between SIPOS and the silicon layer

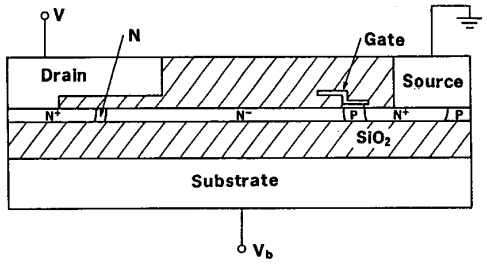


Fig.7 A high voltage lateral MOSFET structure

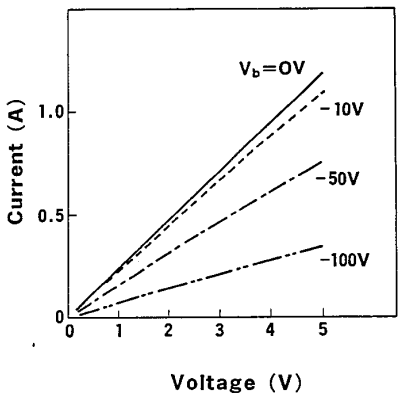


Fig.8 Calculated current-voltage characteristic of thin MOSFET for four different substrate potentials

On-resistance was 43.5 Ω for the substrate of earth potential. The area of this MOSFET:90×10^{-4} cm^2

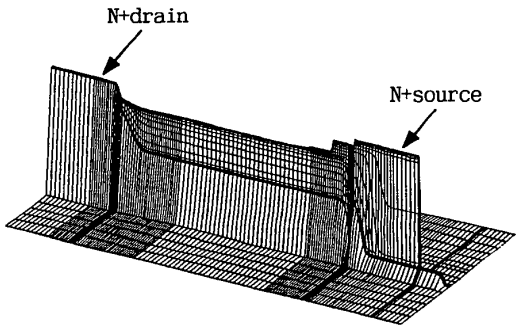


Fig.9 Three dimensional electron density distribution of a very thin SOI MOSFET for -100 V substrate bias

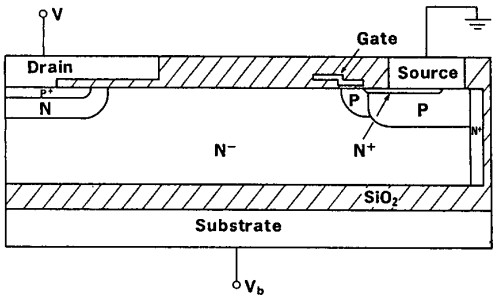
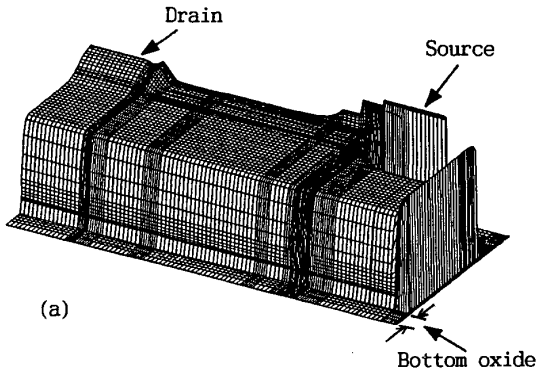


Fig.10 15 μm thick SOI IGBT structure



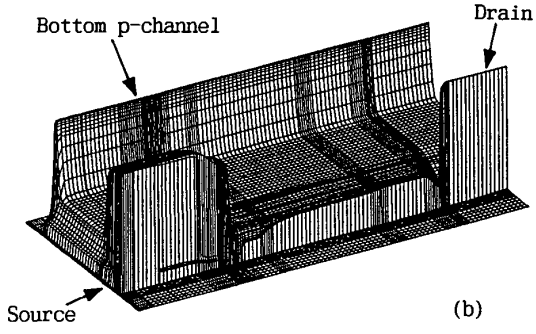


Fig.11 Three dimensional (a) electron and (b) hole density distributions for relatively thick SOI IGBTs

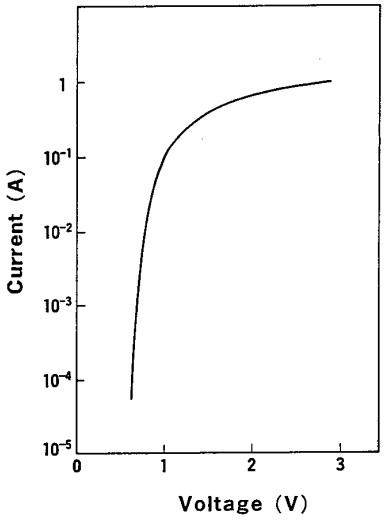


Fig.12 Calculated current-voltage characteristic of an IGBT on a 15 μm thick SOI for a -100 V substrate bias The characteristics hardly depends on the substrate bias.