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HIGH VOLTAGE (4KV) EMITTER SHORT TYPE DIODE (ESD)

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ABSTRACT

This paper reports for the first time, the effects of emitter short structures, ESD(a), ESD(b)(see Fig.1), as well as the effect of a very shallow emitter on the reverse recovery characteristics for 4kV high voltage diodes. It was found that a diode with a shallow p-emitter and emitter short structures attains half of the reverse recovery current Irr, compared to conventional punch-through type p-i-n diode. It was also found that ESD has a further advantage, in that the leakage current is as low as conventional p-n junction diodes, even at 125 ℃. ESD structures with a fine n+ and p+ short structure attains no parasitic effect, even at current density 100 A/cm² and di/dt −1000 A/cm² /μs conditions.

INTRODUCTION

High speed semiconductor power devices, such as GTO thyristors and IGBTs, are widely accepted in various power systems [1][2]. However, their high speed switching capabilities have not yet been fully utilized, because of the lack of good high voltage, high speed diodes. Structures and processes for high voltage diodes, wherein they have over 1 kV reverse voltage, are different from those for low voltage diodes. Conventionally, they have deep main junctions (50 to 60μm deep) and bevel structures (junction termination structures). The deep main junctions are formed by a high temperature (1200-1250 ℃) and long time (30-100 Hr) diffusion, using a dopant with large diffusion constant (for example Ga, Al). Since such a conventional device fabrication design garantees high breakdown voltages, device engineers have been conservative in introducing new processes and design [3][4]. Figure 1 shows commercially available diode 800GXH21 structure which has nonpunch-through type p-i-n structure. This diode has a 850 μm thick and 240 Ω·cm resistivity i-region, a 60 μm deep p+ emitter, and a bevel junction termination structure. Figure 1 shows the studied punch-through type p-i-n structure. Using punch-through structure, i-region width can be reduced to 450μm in the case of 4.5 kV breakdown voltage diode. In these diodes, a large concentration of minority carriers is injected into the i-region during the on-state. The conductivity modulation for the i-region, due to the injected carriers, produces a low forward voltage drop in the on-state. However, to switch these diodes to the blocking state, the minority carriers, stored in the i-region, must be removed. Due to the high emitter injection efficiency of these diodes, the carrier profiles in the on-state are symmetrical. By using lifetime control, swiching performances for these diodes are considerably improved [5][6]. One of the most important parameters of the high voltage diodes is emitter injection efficiency [5]-[8]. It is difficult to reduce emitter efficiency for conventional diodes with deep junctions. Several methods have been proposed to control emitter injection efficiency for low voltage diodes : shallow junction, Schottky junctions, a combination of p-n diode

and Schottky junctions [7]-[9]. However, these structures are not good for high voltage diodes, because these methods accompany higher leakage current and soft breakdown characteristics. Low leakage current and ohmic contact are necessary for high voltage power diodes, Schottky contacts and too shallow junctions are not good structures to control the emitter injection efficiency for high voltage diodes.

EMITTER SHORT DIODE

Emitter short diodes(ESD) are proposed to attain high speed, in high voltage diodes. Figure 1 show two ESD categories. In the ESD(a) structure, emitter short regions (n+) are formed on the p-emitter layer. In the ESD(b) structure, emitter short region (p+) are formed on the n-emitter layer. These short areas reduce the emitter efficiency and attain asymmetric carrier profiles for the i-region in the on-state. In this structure, the carrier density for the shorted emitter portion of the i-region is one tenth smaller than the other emitter portion. Figure 2 shows calculated asymmetrical hole distribution for the diode, ESD(a). Calculation is carried out in 2.6 V on-state voltage, 100 A/cm^2 forward current density conditions.

When a reverse voltage is applied to the ESD(a), a depletion region of the p-n junction expands into the i-region and p-emitter. The impurity doses for the p-emitter were chosen so that the depletion region does not reach the emitter short layers. ESD(a) attained the same low leakage current and hard breakdown characteristics that conventional p-n junction diodes have.

Both emitters have sufficient dose to attain high voltage. ESD structures accompany transistor structure: n+-p-i-n+ in ESD(a) and p+-n-i-p+ in ESD(b). Reverse recovery current and reverse recovery time increase, when these transistors structures switch on. To avoid these parasitic transistor effects and to attain high reverse blocking voltage, high impurity concentration for the emitter is needed. However, to reduce emitter injection efficiency, low impurity concentration for the emitter is needed. It was found that a fine n+ p+ emitter contact pattern is necessary to avoid parasitic transistor effect.

It is difficult for a diode with shallow main junction to achieve high reverse blocking voltage by conventional junction termination structures(bevel etc.). 4kV reverse blocking capability was attained by adopting a combination of a Resurf layer, a SIPOS resistive field plate and a metal field plate(Figs.5 and 6). The optimum junction termination designs for a shallow(4 μm deep) p-emitter were examined by a breakdown voltage simulator TONADDE2B(see Fig.7) [10].

NUMERICAL ANALYSIS FOR REVERSE RECOVERY CURRENT WAVEFORMS

ESD(a), ESD(b) and punch-through and nonpunch-through p-i-n diodes (see Fig.1) were investigated, considering forward voltage, reverse recovery characteristics for various emitter structures, using device simulator TONADDE2C[11]. Figure 3 show calculated reverse recovery current waveforms. Comparisons were made for the same conditions of 2.6 V on-state voltage at 100 A/cm^2 current density and -200 A/cm^2/μs di/dt. Figure 4 shows an external circuit that was used to calculate reverse recovery characteristics. At the point of time where t=0, the external source voltage is 1000 V, the diode forward voltage are 2.6 V and the forward current through the diode and series resistance is 100 A/cm^2. The forward current di/dt rate -200 A/μs at reverse recovery time was attained by changing the external source voltage from 1000 V to -1000 V in 1 μs (dv/dt=-2000 V/μs).

From the device simulations, ESD(a) achieves one eighth of the reverse recovery charge, Qrr, one third of the reverse recovery time, trr, one sixth of the reverse recovery current, Irr, of commercially available diode 800GXH21 and exhibits the so-called soft recovery characteristics. ESD(a) achieves one fourth of the reverse recovery charge, Qrr, two thirds of the reverse recovery time, trr, one third of the reverse recovery current, Irr, for conventional punch through p-i-n diode.

From the device simulation, compared to ESD(a), ESD(b) has large switching loss, because the space charge region spreads from the opposite side of the main junction at the i-region.

JUNCTION TERMINATION DESIGN

As mentioned above, it is difficult to attain high blocking voltage with shallow junctions, using conventional junction termination structures.

4kV reverse blocking was attained by adopting a combination of a Resurf layer, a SIPOS resistive field plate and a metal field plate (Fig.5). The optimum junction termination design for a shallow (4 μm deep) p-emitter were examined by a breakdown voltage simulator TONADDE2B. Figure 7 shows calculated results of reverse blocking voltage as a function of Resurf impurity dose at i-region impurity concentration 1×10^{13} cm^{-3}, 3 μm deep Resurf layers. This figure shows that the maximum breakdown voltage becomes higher as Resurf length increases. However, the optimum condition for the impurity dose of the Resurf layer is very critical. This nature is quite marked for shallow Resurf layer structure. The most suitable conditions regarding Resurf length and impurity dose for the shallow junction structure should be selected to attain high blocking voltage.

DEVICE FABRICATION

Based on the above analyses, 4kV ESD(a)s have actually been fabricated and evaluated. ESD(a)s were fabricated using an n-type high resistive wafers 300 Ω·cm and 450 μm thick. Both sides of emitters, 15μm deep n-emitter and 4μm deep p-emitter, were formed by phosphorus and boron diffusion. The p-emitter layers were formed by inducing minimum impurity doses, to attain 4kV reverse blocking voltage. On the p-emitter, thin and fine n+ and p+ contact layers were also formed by selective diffusion. The contact layers have 1 μm deep and 1×10^{19} cm^{-3} surface concentration, to obtain an ohmic contact with anode electrode. To reduce lateral resistance for p-emitter under n+ contact layers, the n+ areas were formed in a fine stripe pattern. The stripe widths for the n+ contacts were chosen from 1 to 6 μm. An aluminium electrode was formed on the contact layer, a vanadium-nickel-gold trimetal system was formed on the n-emitter. Chips size are 5×5 mm^2, chips activearea are 2.1×2.1 mm^2. Figure 10 is a photo of the investigated ESD chip. Cross sectional views of Resurf and RFP(Resistive Field Plate) are shown in Fig.5. Resurf p-layer is 4μm deep and 800 μm long. Total length of Resurf and RFP is 1.1 mm. Impurity doses for Resurf layer, RFP length and metal field plate length were examined, based on the result of calculation by break down voltage simulator TONADDE2B.

To avoid the parasitic effect at n+ contact layer, the lateral resistance at the p-emitter under the n+ contact layer was controlled. This was done by choosing the most suitable p-emitter impurity doses and n+ p+ fine pattern sizes in such a way that 0.5 V forward bias does not happen at the junctions that are formed between n+ contact layers and p-emitter in the reverse recovery time. After

separating the wafer into individual dies, the dies were assembled in TO3 packages.

EXPERIMENTAL RESULT

Figure 6 shows the 4kV reverse blocking waveform for ESD(a) at room temperature. Figure 9 shows reverse leakage currents at Tc=125 ℃ and room temperature. It was found that ESD(a)s have sufficient ability to reduce emitter injection efficiency (see Fig.8) and that perfect p-n junctions remained, even at 125 ℃. Figure 8 shows a comparison between ESD(a)(Ln=1, Lp=3) and a conventional punch-through p-i-n diode at the same on-state voltage 1.24 V at 100 A/cm² forward current density. From Fig.8 the ESD(a) has 30 A/cm² reverse recovery current, reverse recovery time is 0.7 μs, reverse charge is 10 μC/cm², conventional punch-through p-i-n diodes has reverse recovery current 54 A/cm², reverse recovery time trr 1.5 μs, reverse charge 40 μC/cm². The ESD(a) has half of reverse current Irr, half of reverse recovery time trr, and one fourth of reverse charge Qrr, and what is called soft recovery current waveform, compared to a conventional p-i-n diode at current density 100 A/μs, di/dt = -100 A/μs, at room temperature. Figure 11 shows on-state voltage and reverse recovery current for conventional punch-through p-i-n diode and the ESD(a). ESD(a) (Ln=1, Lp=3) has 1.24 V on-state voltage of at forward current 100 A/cm², and it has short recovery time and soft recovery current waveform (see Fig.8). For ESD(a)s (Ln= 1 to 3μm), no parasitic effects were observed under current density >100 A/cm², di/dt>1000 A/μs/cm² conditions.

SUMMARY

The ESD concept is proposed. The proposed emitter short structure controls reverse recovery current behavior and switching loss in reverse recovery time, without parasitic transistor effect.

It was experimentally confirmed that a diode with shallow p-emitter and emitter short structures attains a high speed 4kV diode. It achieves half of reverse current, Irr, half of reverse recovery time, trr, and one fourth of reverse charge, Qrr, and exhibits the so-called soft recovery characteristics, compared to a conventional punch-through p-i-n diode.

It was also confirmed that emitter efficiency values are most important factors to control reverse recovery current behavior, as numerical analysis predicted.

It was also found that ESD(a) has low leakage current, even at 125 ℃. The ESD(a) leakage current is as low as the leakage current for a conventional p-n junction diode. In this point, ESD has a further adventage over mere shallow p-emitter or Schottky diodes.

The ESD concept makes them suitable for use as high voltage power devices. Emitter short structures combined with shallow p-emitter and novel junction termination structures (combinations of Resurf layer, a SIPOS resistive field plate and a metal field plate) are promising techniques for future high voltage power diodes.

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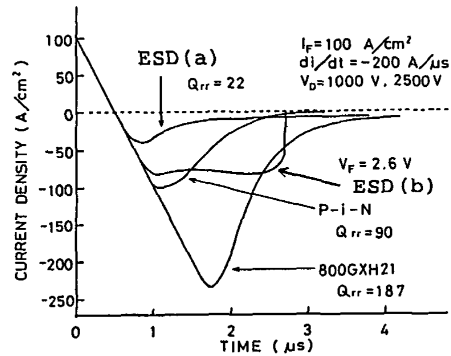

Fig.3 Reverse recovery current for ESD(a), ESD(b),conventional punch-through p-i-n diode and nonpunch-though p-i-n diode.

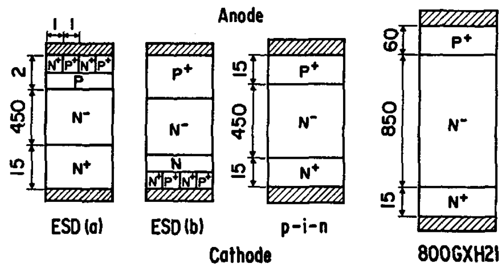

Fig.1 Cross-sectional views for ESD(a),(b), punch-through and non-punchthrough p-i-n diodes with same break down voltage.

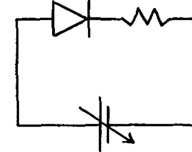

Fig.4 External circuit for calculating reverse recovery current waveforms.

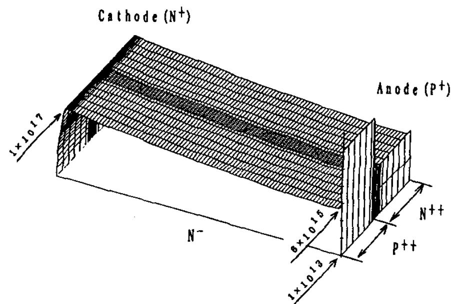

Fig.2 Hole density profile for ESD(a) during on-state.

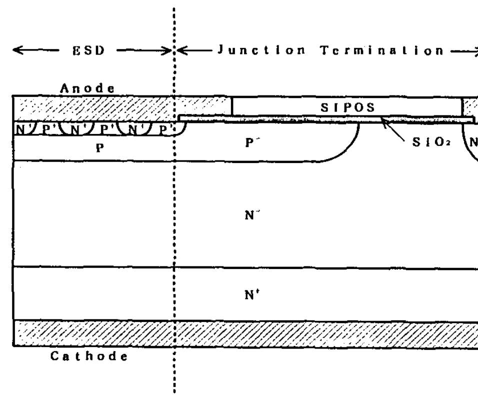

Fig.5 Cross-sectional view for ESD(a) with Resurf and RFP structure.

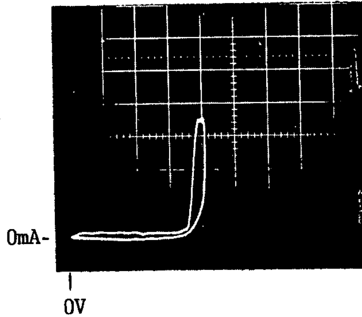

Fig.6 4kV Reverse blocking waveform(1kV/div., 1mV/div.)

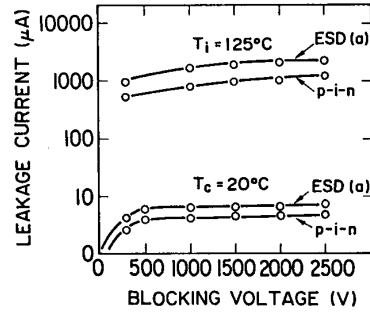

Fig.9 Reverse bias vs. leakage current for ESD(a) and conventional punch-through p-i-n diode.

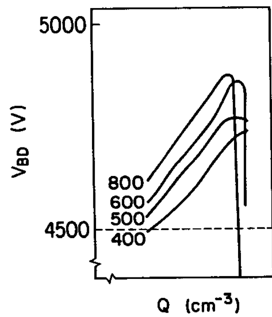

Fig.7 Reverse blocking voltage vs. Resurf impurity dose with Resurf length as a parameter (simulated results).

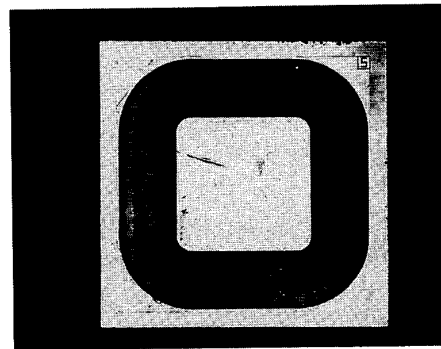
Fig.10 Fabricated ESD photo.

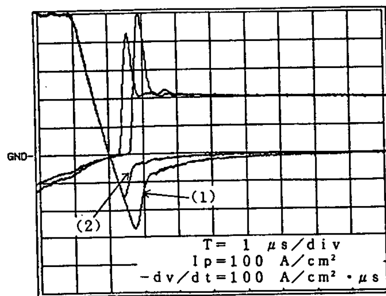

Fig.8 Reverse recovery current for (1):conventional punch-through p-i-n diode and (2):ESD(a) (experimental result)

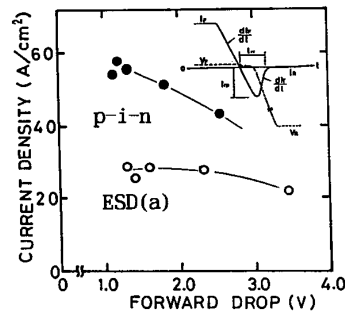

Fig.11 On-state voltage vs. reverse recovery current for ESD(a) and conventional punch-through p-i-n diode.