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4.5 kV GTO Turn-off Failure Analysis under an Inductive Load Including Snubber, Gate Circuit and Various Parasitics

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Abstract

GTO turn-off failure process has not yet been successfully analyzed by numerical methods while gate-turn-off thyristors(GTO) have gained their reputation in various applications. Because conventional numerical analyses on GTO turn off processes had been performed under simplified external circuits to avoid the difficulties in obtaining numerical convergence.

In this paper, the authors report for the first time that an exact simulation of the 4.5 kV GTO turn-off failure process has been successfully executed by taking into account complete external circuits including the snubber and all the parasitics. It has been shown that the failure process is closely coupled with impact ionization and the influence of the external circuits.

1. Introduction

GTO's are the most attractive devices for high power switching because of the large capability of controlling over 3kA at a voltage of over 4.5kV. Thus, their turn-off process, including turn-off failure process had been analyzed in both experimental and numerical way to find out a better design for a large safety operating area. In 1966, the conduction region squeezing during turn-off period was analyzed by Wolley for the first time [1]. Naito et al. introduced a 1-D numerical model to analyze the turn-off process in 1979 [2]. In 1981, the conduction squeezing process was included effectively into a 1-D model to analyzed the turn-off failure phenomena by Ohashi and Nakagawa based on experimental results [3]. Nakagawa also carried out temperature dependent turn-off simulation in both 1-D and 2-D model [4],[5]. Stoisiek et al. proposed an analytical model which include avalanche injection to try to explain the influence of the avalanche injection on the destruction during the turn-off [6]. However, non of these simulations had explained the dynamic turn-off failure phenomena, such as the sudden increase in the tail current at the destruction as well as the influence of impact ionization, external circuits and parasitics, because these simulations were carried out with simplified external circuits to avoid difficulties in the simulations with the complete external circuits.

It has been found that the turn-off simulations with complete external circuits are possible only if the external circuit equations are completely coupled with the set of device equations in the Newton scheme, i.e. both the circuit equations and the device equations are solved in a Newton iteration at once. The authors has been developed a new efficient solution technique [7] and implemented into the TONADDE II C program [8] to carry out the simulation. A typical number of the Newton iterations is four to attain the convergence even with complicated external circuits.

In this paper, the authors unveil the dynamic turn-off failure process by complete simulations of GTO turn-off under an inductive load including a snubber, a gate circuit and various parasitics as well as carrier generation due to impact ionization, which successfully reproduced the experimental destruction waveform.

Fig. 1 shows a typical experimental turn-off failure waveform for a GTO ([9]). The destruction point is often observed in the tail current period, where the anode current shoots up again with about 4 μsec time delay after the anode current interruption.

2. Simulation results

Fig. 2 represents the simulated system. The simulations were carried out under an inductive load with snubber circuit. The gate circuit was considered as well. There are many parasitics in an actual system and these parasitics greatly affect the turn-off behavior. For example, V_{DSP} (the anode voltage spike height) is mainly determined by parasitic inductance in the snubber circuit. Moreover, gate current dI_G/dt is determined by the parasitic inductance in the circuit. These parasitics can also affect the turn-off failure behavior, so that the simulation system included all the parasitics in the external circuits. The system has a load inductance L of 10μH and a snubber inductance Ls of 0.2 μH. The calculated base-cathode breakdown voltage is 56 V.

2.1 Simulation results for various snubber capacitances

Fig. 3 shows simulated GTO turn-off waveforms for various snubber capacitances(Cs) with a gate source voltage V_{GG} of -50 V and a gate inductance of 0.8 μH. The calculated waveforms for Cs=6 μF agrees well with the actual normal turn-off waveforms for a GTO. For the case of Cs=4 μF, the tail current slightly increases due to the increased dV_A/dt of the anode voltage and the resultant increase in impact ionization. For the case of Cs=3 μF, the anode current suddenly increased 4 μsec after the anode current was once interrupted. The calculated waveforms exactly reproduced the

experimentally observed turn-off failure, which is shown in Fig.1.

Fig. 4 shows the details of the turn-off failure waveforms for Cs=3 μF together with the amount of generated charges per unit time due to the impact ionization in the center junction. Fig. 5(a)-(e) represent bird's eye views for electron density distribution during the turn-off failure. As can be seen from Fig. 5(a), N-base region was filled with carriers at on-state. During the storage period, carriers squeezed into the central portion of the cell according to the increase in the gate current. This squeezing can be observed clearly in Fig. 5 (b) which represents electron density distribution at the end of storage period (t=9.88 μsec) . Electron injection from the N-emitter was interrupted when the anode voltage once peaked out at V_{DSP} of 1500V (Fig. 5 (c), t=11.68 μsec). Since then, electron density in the high electric field region had been kept in its low level as shown in Fig. 5 (d) until the carrier generation due to impact ionization in the region increased the electron density (Fig.5 (e)). Fig. 5 (f) represents the distribution at the beginning of rapid increase in the anode current (t=16.00 μsec) . It was found that electron began to be injected again from the center portion of N-emitter. Fig. 5 (g) represents the distribution at the destruction. A great amount of electron was injected from the N-emitter and greatly concentrated into the center of the device.

2.2 Simulation results for various gate source voltages

Simulations for various gate source voltages were also carried out for a snubber capacitance of 4 μF. Fig. 6 represents the obtained turn-off waveform for a gate source voltage V_{GG} of -50 V and a gate inductance of 0.8 μH with generated charge per unit time in the center junction due to impact ionization. Although the impact ionization in the center junction shifted the latter half of the tail current waveform slightly higher, the anode current was turned-off. The gate voltage had been kept around -56 V, which is the base-cathode breakdown voltage, during the tail current period because the avalanche current flew through the reverse biased base-cathode junction during the tail period. Fig. 7 represents turn-off waveform for V_{GG} = -40 V and a gate inductance of 0.4 μF. Waveforms for the anode voltage and the anode current are almost the same as those for V_{GG} = -50 V. However, the gate current decreased in a higher rate after the gate voltage drop so that the gate current finally met the tail current and the gate voltage suddenly recovered to -32 V. Turn-off failure was observed in the waveform for V_{GG} = -25 V and a gate inductance of 0.4μH,which is shown in Fig. 8. The gate voltage began to increase when the gate current decreased to the level of the tail current and finally recovered to a positive voltage. Then the anode current rapidly increased. The same gate voltage behavior is also observed in experimental results. Fig. 9 shows experimentally obtained waveforms for a GTO with two different V_{GG} of 17 V and 12 V. The gate inductances were chosen so that dI_G/dt for two cases were the same during storage period. As can be seen from the figure, the gate voltage did not recover in the tail current region for V_{GG} = 17V because the gate current was high enough to absorb all the tail current. However, the gate voltage for V_{GG} = 12V recovers when the gate current decreased to the level of the tail current.

3. Discussions

3.1 Destruction mechanism for 2-D case

As can be seen from the turn-off failure waveforms for V_{GG} = -50 V and Cs = 3μF shown in Fig. 4, the rapid increase in the anode current appeared in the tail current period after the anode current once turned-off. The anode current initially increased according to the carrier generation due to the impact ionization in the high electric field region in the center junction. The anode current was forced to increase so that finally exceeded the gate current. Then, the gate current had to increase and the gate voltage recovered. However, the gate current could not absorb all the increased anode current, because the increase rate of the gate current dI_G/dt was limited by the stray inductance L_G in the gate circuit. The excess current flew into P-base and forwardly biased the central portion of the P-base N-emitter junction, which induced electron injection again from the cathode N-emitter (Fig. 5(d)). Once electron was injected into the high electric field region, the anode current accelerately increased to around 2 kA, while the generated charge in the center junction decreases. This phenomenon is explained as follows. Fig. 10 represents transition of y-direction electric field along the center line of the device. The electric field uniformly increased before the start of the electron injection from N-emitter (t=14.41 μsec and 15.41 μsec). Once electron was injected, however, the injected electron relaxed the electric field strength, thus widened the high electric field region in the N-base. As can be seen from Fig. 11 which shows hole density along the center line of the device, the expanded high electric field region swept carriers which had been stored in the anode side of the N-base. The swept out carrier flew into P-base through the high electric field region and worked as effective positive gate current which accelerated the electron injection from the N-emitter into the high electric field region (Fig. 5(g)).

3.2 Wafer level destruction mechanism

During tail current period, the GTO turn-off can be considered as a pnp-transistor operation. The SOA for a pnp transistor is given by following inequality ([10]) by assuming that only hole current homogeneously flows in the high electric field region, (see Appendix)

$$I_A < Seff\, q\, v_s N_D (V_{BD} / V_A - 1). \quad Eq.(1)$$

Here, Seff, v_s and N_D give the effective device area, the saturation velocity for hole, and impurity concentration of N-base. V_{BD} and V_A are the breakdown voltage for the main junction and the anode voltage. Fig. 4 represents

the simulated turn-off failure waveform and the calculated critical anode current limit. The initial increase in the tail current appears just when the tail current exceeds this limit. In actual device, however, actual device destructions are often observed in much lower tail current than the calculated critical anode current limit for pnp-transistor (Eq.(1)). This is because the current strongly concentrates into a small area in a wafer at the end of the storage period so that current imbalance between cells can remain during tail current period, although the current concentration is assumed to be relaxed during the period. Thermal distribution and inhomogeneousity in doping profile can also affect the current imbalance ([11], [12]).

It is assumed to be the current concentration into a small area of the device that causes the tail current to increase by impact ionization in a lower current level than the theoretically predicted critical current limit, which is correct for 1-D case. Particular attention should be paid to the facts that the gate voltage does not reach near or to zero even if actual device failure occurs. This is because tail current increase in a localized area does not significantly affects the total tail current. This suggests that GTO turn-off failure must accompany larger amount of anode current increase due to impact ionization in the pnp-transistor mode in a localized current concentrated area. In order to approximately simulate actual GTO turn-off failure, which is 3-D phenomena, we carried out another simulation with keeping gate voltage at -56V throughout the tail time period. Fig.12 represents the obtained waveform for Cs = 3 μF. As can be seen from the figure, the tail current drastically increased when the tail current exceeded the critical current limit although the gate voltage had been kept at -56V, and the anode voltage steadily increased during the period. When the anode current increased, the increasing rate of the simulated anode voltage was slightly lowered because of the external circuit influence and it supress the carrier generaton due to impact ionization. However, the anode voltage increasing rate for an actual device cannot be lowered as far as the increase in the anode current in the localized current concentrated area does not affect the total anode current waveform. Therefore the tail current in the current concentrated area increases in a higher rate than that for the simulation result. This result suggest that a large amount of impact ionization in a localized current concentrated area can occur and causes the rapid increase in the total anode current. This finally causes electron injection from N-emitter if the local anode current exceeds the level of locally supplied gate current.

4.Conclusions

GTO turn-off failure process has been completely reproduced by numerical simulations under an inductive load considering with snubber, gate circuit and parasitics as well as carrier generation due to impact ionization. The simulation was carried out using the TONADDE II C program in which a new solution algorithm has been implemented for device-circuit mixed level simulation.

From the simulation results, the rapid increase in the anode current observed during tail current period and these results agreed with experimentally obtained waveforms. It is also found that the turn-off failure in the actual device is greatly affected by current imbalance between cells and accompanied with a large amount of impact ionization in the localized current concentrated area.

Acknowledgement

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Appendix

Assuming that only hole current homogeneously flows in the high electric field region with the saturation velocity v_s, the electric field in the region is given by solving following 1-D Poisson equation([10]).

$$dE/dx = -(q/\varepsilon)(N_D + Jp/(qv_s))$$

Here Jp gives hole current density in the high electric field region. The maximum electric field strength E_{max} and the applied voltage V_A are obtained as functions of the high electric field region length w and Jp.

$$E_{max} = (qw/\varepsilon)(N_D + Jp/(qv_s))$$

$$V_A = E_{max}\, w/2$$

Eliminating w from these equations,

$$E_{max}^{\ 2} = (2q / \varepsilon) (N_D + Jp / (qv_s)) V_A .$$

Thus the hole current density is expressed as a function of the V_A and E_{max}.

$$Jp = q v_s ((\varepsilon / q) E_{max}^{\ 2} / (2V_A) - N_D)$$

E_{max} is, however, limited by the breakdown voltage V_{BD}.

$$E_{max}^{\ 2} < 2q N_D V_{BD} / \varepsilon$$

Consequently, critical current density limit is given by the ratio of V_A to V_{BD},

$$Jp < q v_s N_D (V_{BD} / V_A - 1).$$

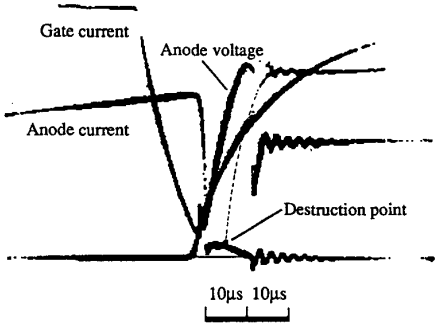


Fig. 1 A typical experimental turn-off failure waveform for a GTO.

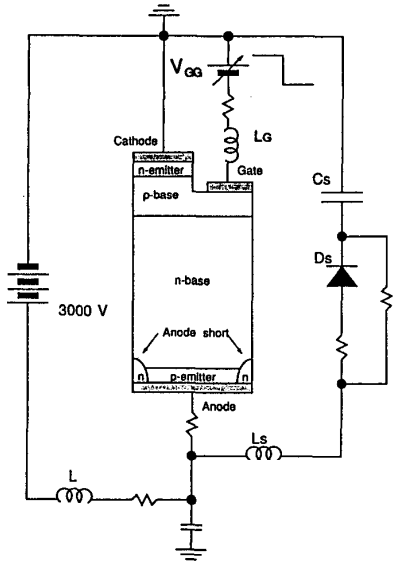


Fig. 2 Simulation system.

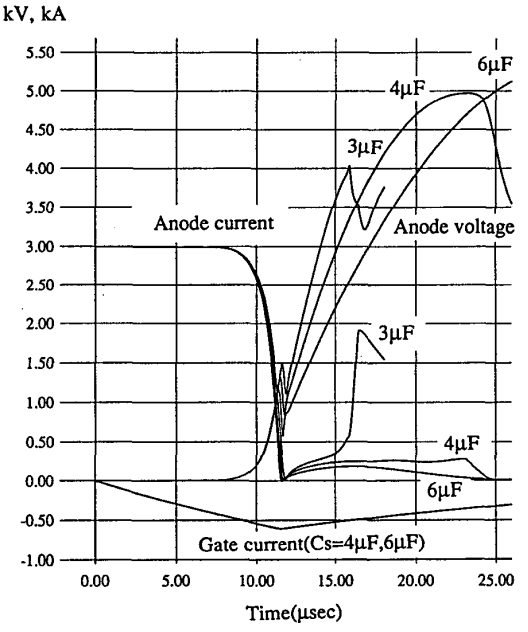


Fig. 3 Simulated GTO turn-off waveforms for various snubber capacitances(Cs). For the case of Cs=3 μF, the anode current suddenly increases 4 μsec after the anode current interruption, which agrees very well with experimental turn-off failure waveform (Fig.1) .

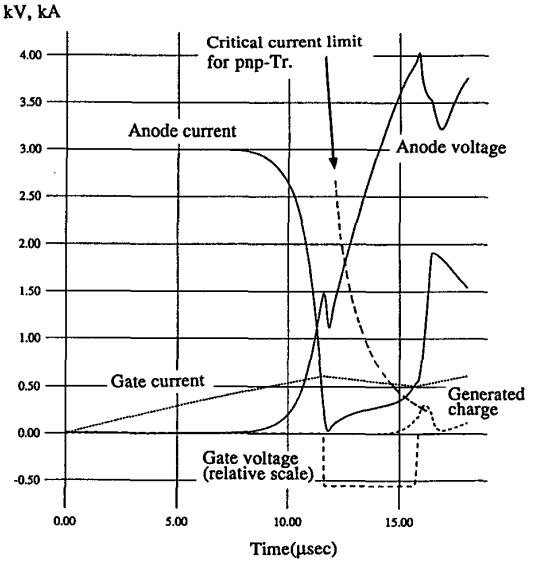


Fig. 4 The details of the destruction waveforms for Cs=3 μF together with the amount of generated charges per unit time due to the impact ionization in the center junction. The calculated critical current limit for pnp-transistor is shown as well.

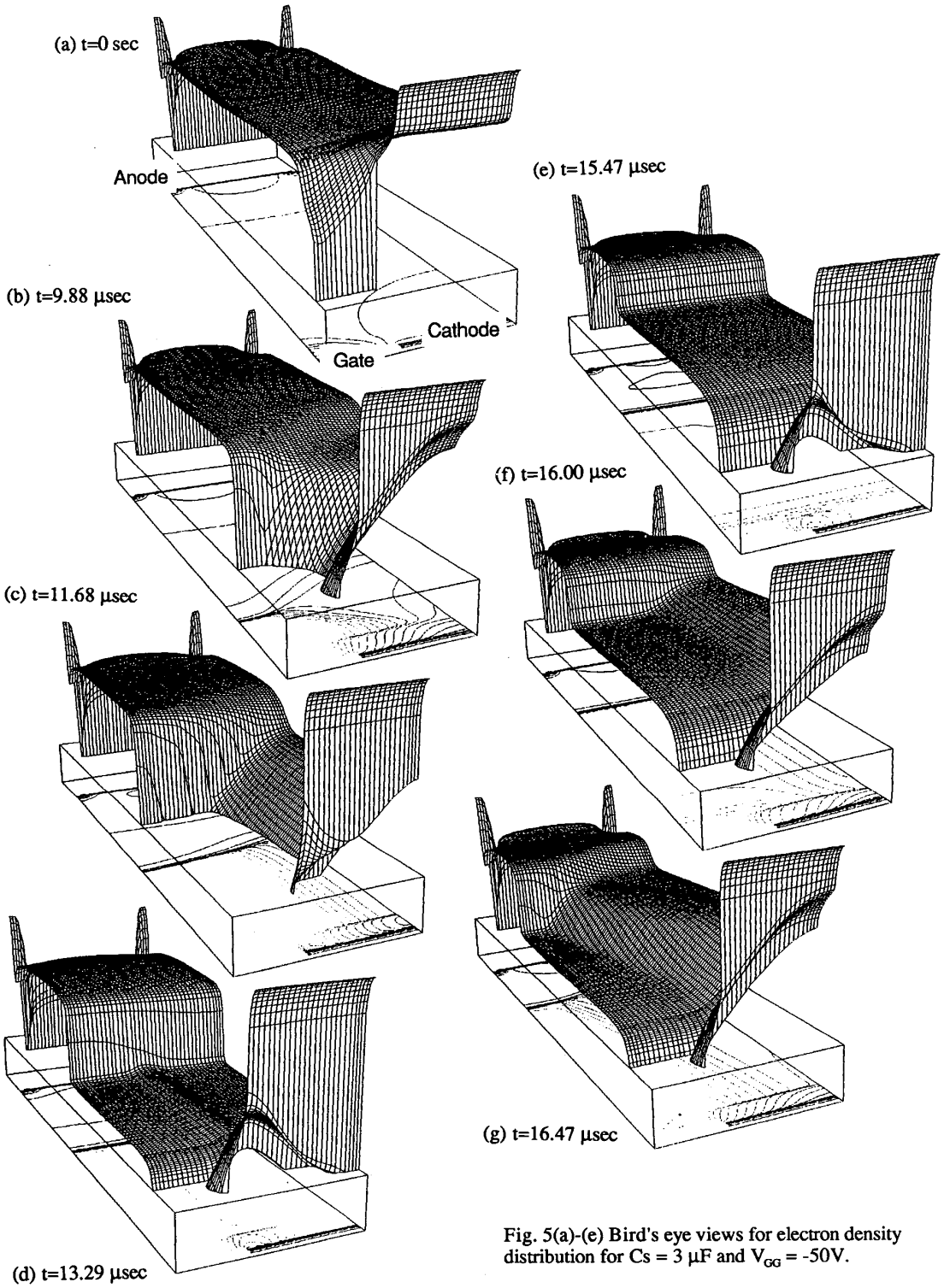
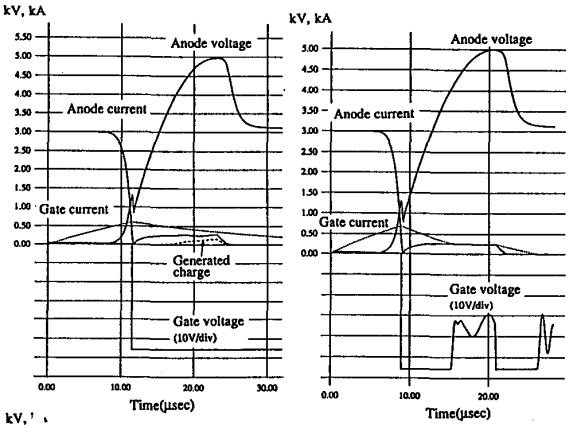


Fig. 5(a)-(e) Bird's eye views for electron density distribution for Cs = 3 μF and V_{GG} = -50V.



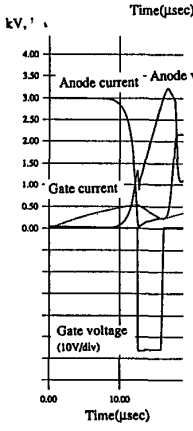


Fig. 6 Simulated turn-off waveform for Cs = 4μF, V_{GG} = -50 V and a gate inductance of 0.8 μH with generated charge per unit time in the center junction.

Fig. 7 Simulated turn-off waveform for Cs = 4μF, V_{GG} = -40V and a gate inductance of 0.4 μH.

Fig. 8 Simulated turn-off failure waveform for Cs = 4μF, V_{GG} = -25 V and a gate inductance of 0.4 μH.

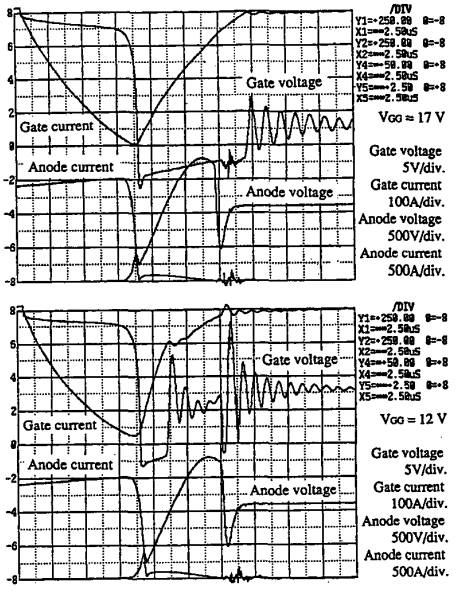


Fig. 9 Experimentally observed waveforms for a 4.5kV GTO with two different V_{GG} of 17 V and 12 V.

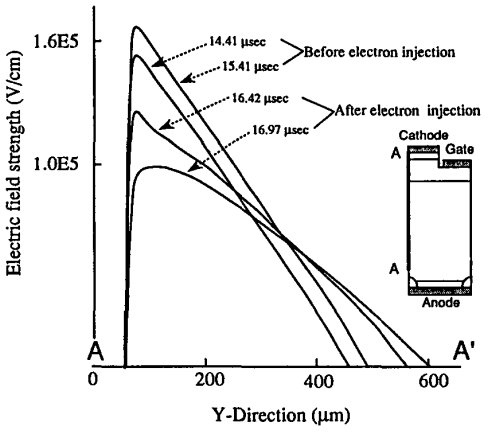


Fig. 10 Transition of y-direction electric field along the center line of the device.

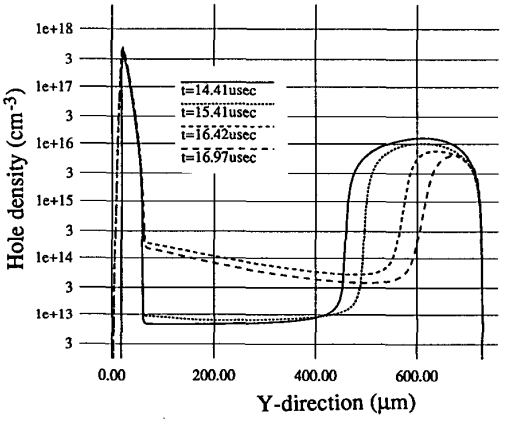


Fig. 11 Hole density along the center line of the device. The high electric field region swept out carriers which had been stored in the anode side of the N-base.

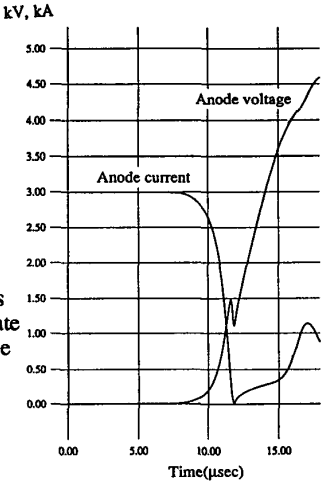


Fig. 12 Simulated waveforms for Cs = 3μF with keeping gate voltage at -56V throughout the tail time period.