IMPACT OF DIELECTRIC ISOLATION TECHNOLOGY ON POWER ICs

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Abstract

Dielectric isolation(DI) is superior method for integrating any kinds of devices in a single chip. The success of a high voltage telecommunication IC, called SLIC, advanced the technology of DI.

The next driving force will be high voltage and relatively large current power ICs, integrating a small power system unit into a single chip. This small scaled version of "system on chip" ICs will fully utilize advantages of the DI method, operated at a high temperature when installed inside such instruments as motors or lamps. This will realize simplified and small sized power systems or apparatus.

Research efforts for a low cost DI method will be led by SOI technology using several micron thick or less silicon layers. This will simplify the device isolation and even attain high voltages.

Introduction

VLSI technology has advanced so greatly that even 64Mbit DRAMs have become a reality. Power systems and the related circuits cannot be outside the influence of VLSI technology[1]. It would be quite strange for power systems alone to still continue to consume a large space while brains become smaller and smaller. Integration of power systems into a single silicon chip will be a reality within the next decade.

Early work on power integrated circuits was instigated by the needs for display drivers and high voltage telecommunication circuits.

Efforts to achieve high voltage lateral MOSFETs started in the early 70's and 800V lateral MOSFET[2], using RESURF concept and DMOS(DSA[3]) technology, was developed for display drivers in 1976, before the RESURF concept was fully established[4].

The development of high voltage SLICs advanced the dielectric isolation technique[5-7] because it required electrically floating bidirectional switches, which were difficult to be realized by the conventional junction isolation technique.

In this paper, impacts and advantages of dielectric isolation will be discussed, and an attempt will be made to highlight the directions of DI research.

Impact of DI

The dielectric isolation has many advantages[8,9] over junction isolation techniques in regard to points wherein:

1)Virtually all integrated components can be treated as if they were discrete devices, so that circuit design becomes easy.
2)Bipolar devices, including thyristors can be integrated without any difficulties.
3)Coupling between two devices can be minimized, thus, attaining better IC performances: no latch-up, high speed, large noise immunity and ruggedness.
4)High temperature operation is feasible, because there are virtually no parasitics and leakage current is low.
5)Radiation hardness for space use.

Recently, the power MOSFET technology has been greatly improved. Especially, the success in the MOS bipolar composite devices such as IGBTs[10,11,12] and MCTs[13] made it possible to control a large current by the MOS gate. DMOSFETs have been frequently used as output devices in high side switches[14], leading to a vast application market in the automotive field[15], replacing mechanical relays and eliminating wire harness.

The large current handling capability by using the MOS gate has accelerated adopting MOS gated high voltage bipolar devices and even thyristors in power ICs[16].

In addition, a variety of dielectric isolation techniques have been invented, such as SOS[17] SIMOX[18,19], recrystallized polysilicon such as ZMR[20], Silicon wafer Direct-Bonding(SDB)[21], oxidizing porous silicon[22] etc. along with improvements in the conventional DI technique(soot bonding[23] and MSSD[24]). All this background has matured enough to start application of DI in larger areas of power ICs.

The author assumes that the merits of DI have not been fully utilized as yet and that there is still a large potential for realizing ultimate targets:
1) A higher voltage larger current multi-output power ICs (including source followers), fully integrating an entire power system.
2) High temperature operated power ICs to be installed inside instruments.

Thus, for the next decade, most DI research will be directed toward
1)Large monolithic device integration including a plural number of high voltage high current devices, aiming at system on chip power ICs.
2)ICs allowing high temperature operation and ruggedness.
3)Low cost DI process development.
4)High current high speed MOS controlled lateral output devices operated at a high temperature with self-protection functions.

The near future objectives are motor control ICs, especially, small intelligent motors equipped with one chip inverter ICs, light and small plug-in fluorescent lamps, and on-board one chip DC-DC converters.

These power ICs need to operate safely in a high temperature atmosphere in order to be installed inside the motors or lamps etc., which are no low temperature heat sinks but heat generators instead, contributing to increased reliability and reducing system sizes.

Special interest will be directed to thin silicon layer on silicon dioxide SOI structures. This is because thin silicon layers are easy to isolate devices and still retain possibilities for handling very high voltage and even higher current, in spite of their layer thinness. Several micron thick or even less SOI will realize a high device integration density, low cost isolation and even a large diameter wafer enough to utilize VLSI processes and fabrication lines, thus, reducing chip cost.

According to the thus stated reasons, emphasis will be applied, in this paper, to high voltage power ICs with a plural number of large current devices.

Dielectric isolation technology using thick siliconlayers

The first success in DI application involved high voltage telecommunication ICs, called SLICs., which require electrically floating high voltage

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bidirctional switches. Thus, DI was the only solution for successfully achieving such ICs.
In the early developed SLICs, double injection devices with current control gates such as gated diodes and GTOs were used for such switches[6,25]. Recently, new version telecommunication ICs have adopted lateral IGBTs[26] or MOS gated thyristors[27] because of the ease of gate drive. All the commercialized SLICs, so far, adopted the conventional DI method [28].

The requirement for and the resultant research on SLIC have advanced DI methods and fabrication processes. The success in SLIC was supported by the fact that monolithic integration and added function deserved expensive DI.

Conventional DI substrates must have become cheaper because of mass-production, following the well-known learning curve. This will give a trigger for wider application of DI to other power ICs.

The author assume that one of the next good research target of DI is motor control inverter ICs. Required and desired targeted power handling capability is 1kW. This specification will realize small intelligent motors, washing machines, refrigerators and many.

Dielectric isolation methods based on conventional EPIC and recently introduced silicon wafer direct-bonding(SDB) are both promising candidates for such power ICs. The reasons are that thick silicon islands, which are required for handling high current, can easily be fabricated.

Figures 1 and 2 compare two IC structures. The SDB method has both merits and demerits over EPIC.

The merits are:

1)High thermal conductivity of single crystalline silicon substrate, suited for high power.

2)Ease for large diameter wafers for reducing chip cost.

The demerits are:

3)Relatively large isolation regions due to V grooves and only a small number of output devices can be implemented.

4)Bipolar logics are difficult to implement because a large number of low voltage logics should be fabricated on a single silicon island.

Item 3) does not actually restrict the application of the SDB method, because most of the high current power ICs have a relatively small number of output devices.

Power IC chips can be fabricated at reasonable cost if all the integrated devices are formed only by diffusions without buried layers. This is easily realized if all the analog functions are designed using only CMOS processes and if high speed output devices are realized without introducing lifetime killers. It was reported[29] that CMOS can operate at a high temperature(350°C), so this approach will also lead to high temperature operating power ICs.

Analog functions have now been frquently designed using only CMOS processes. High speed lateral IGBTs, fabricated only by diffusion, have also already been developed by introducing additional N^+ diffusion in the P-drain([30], see Figs.3 and 4[31]). This LIGBT attained 0.2μs fall-time without any lifetime killers. The alternative techniques are schottky[32] or emitter-short. Even the high speed diode can be fabricated by adopting the same method as shown in Fig.5 or by using a lightly doped P-emitter[33,34,35].

Although CMOS analog circuits have become popular, circuit designers are sometimes still conservative. They claim bipolar logic functions. Figure 6 shows a cross-sectional view of newly developed power ICs, capable of implementing junction isolated bipolar logics in a single DI island. Since the conventional junction isolated low voltage BiCMOS logics can be fabricated in a single DI island, well matured analog logic libraries can be simply utilized.

Figure 6 shows the fabrication process sequence for such dielectrically isolated substrate wafers. After forming a P^+ diffusion layer and a silicon dioxide film, a P^- wafer is bonded to another substrate and then the P^- layer thickness is adjusted. The N^+ buried diffusion layers are formed, before an N type high resistivity layer is epitaxially grown. The V groove isolation and the surface finish are, then, subsequently carried out so that the epitaxial layer remains.

A 250V 1A 3 phase inverter IC has already been developed using conventional DI[36].

A 500V 1A inverter IC chip has also been developed recently, using a SDB substrate shown in Fig.6, integrating six 500V LIGBTs, diodes, protection circuits and even a PWM circuit, which operates at a 16kHz carrier frequency (see Fig.7).

These research efforts will surely lead to system on chip power ICs.

DI utilizing thin silicon layers

If a silicon layer on a silicon dioxide film is thin enough, device isolation is easily done by trenches or even by LOCOS.

Attempts to utilize thin silicon layers for power ICs started after the invention of SIMOX, SOS and recrystallized SOI methods, etc. 180V and 1100V lateral MOSFETs on recrystallized SOI[37] or SOS[38] were developed in 1987 and 1979, respectively.

The ZMR method has also been utilized to dielectrically isolate logics from vertical high current devices[39].

There are two big issues associated with high voltage devices on SOI. One is how to realize a high voltage under the influence of substrate ground potential. The other is how to attain a low on-resistance with a thin silicon layer.

In the conventional DI, the wrap-around N^+ region(see Fig.1) is used in the DI island to prevent the influence of substrate potential[40] on the device breakdown voltage.

However, for thin silicon layers, this method cannot be used. The bottom silicon dioxide layer simply works as an undoped layer as far as Poisson equation is concerned. Thus, a SOI layer on a grounded silicon substrate structure behaves similarly to the structure of a doped N type thin silicon layer/undoped silicon layer (corresponding to silicon dioxide)/grounded P^+ silicon substrate. In this repect, the SOI layer works similarly to a resurf layer.

Attaining a high breakdown voltage for a thin silicon layer device will be a hot issue for the next several years. One possible method[41] is to share a large part of the applied voltage to the silicon dioxide film, where even a high electric field does not cause oxide film breakdown. Two normal components $E_t(Si)$,$E_t(I)$ of the electric fields to the interface of the silicon and the bottom insulator layers have the relation:

$$\epsilon(Si)E_t(Si)=\epsilon(I)E_t(I),$$

where $\epsilon(Si)$,$\epsilon(I)$ denote dielectric constants for silicon and silicon dioxide, respectively.

Using an insulator film with a lower dielectric constant will increase device breakdown voltage because the insulator layer shares a larger voltage.

The device breakdown voltage naturally depends on the thickness of the bottom insulator layer, as shown in Fig.8, where a 20μm thick silicon layer structure (see Fig.9) is assumed.

Figure 10 shows experimentally obtained 600V breakdown voltage, using a 20μm silicon layer and 3μm silicon dioxide structure shown in Fig.9.

Another method is to completely shield the influence of the substrate potential. A method inserting polysilicon field plate between the device and the substrate, as shown in Fig.11, was proposed[42] in 1989.

Highest breakdown voltage will be obtained, if a method is found so that the electric field component normal to the silicon and insulator interface is

reduced and only the component parallel to the interface is dominant in the thin silicon layers. One possible method for this is to use a SIPOS film as a field shielding layer and insert it between the silicon and the oxide interface as shown in Fig.12. Figure 13 shows the calculated lateral diode potential distribution, where an ideal breakdown voltage can be realized.

It was found that the device layout also affects the breakdown voltage for thin layer devices[41]. The drain N^+ layer should be surrounded by the source P^+ layer. If the layout is reversed, a part of the silicon dioxide film under the drain layer sustains all the drain voltage. This induces a high electric field near the drain, as shown in Fig.14.

Figure 15 shows calculated dependence of LIGBT on-resistance on the silicon layer thickness. It is quite astonishing that the on-resistance does not significantly increase even if the silicon layer thickness decreases to 1μm (carrier lifetime is assumed as high as 5μs). This result is quite favorable for thin SOI power ICs.

Application of thin SOI to power ICs has just started. By adjusting the thickness of the SOI layer, this technology will have faily large application fields.

DI for vertical high current devices

DI can be applied to power ICs with a high current vertical output device. Various DI processes have already been proposed for this kind of power ICs, including the methods based on conventional DI called VLCS(see Fig.16[43]), SDB(see Fig.17[44]) and thin SOI(see Fig.18[39]). The most largest market is in automotive applications. The PN junction isolation is a competing candidate for low voltage high side switches. A large number of high side switches have been developed, adopting the JI methods.

DI high side switches will be used in cost-effective areas, where high temperature operation or ruggedness are required.

DI will also be used for power ICs with high voltage large current vertical output devices. The reason is that monolithic integration of gate circuits has a potential wherein:

1)5V gate drive voltage can be used instead of conventional 15V.

2)Negative gate bias will not be required during the off-state.

This will greatly simplify the system and will gain advantage over hybrid approach.

Conclusion

High voltage and large current intelligent power ICs, aiming at the system on chip, will probably be realized only by the DI method. It will realize simplified and small sized systems, as well as increased reliability.

Key technologies accelerating this trend will be:

1)Simplified isolation and large diameter wafer, reducing chip cost.

2)All diffusion CMOS logics and output devices.

3)High temperature operation.

4)High voltage large current high speed MOS gate output devices.

System on chip power ICs will provide cost-effective added values. Such Power ICs will be key components for simplified systems, just like MPUs for personal computers. This will trigger wider application of DI methods.

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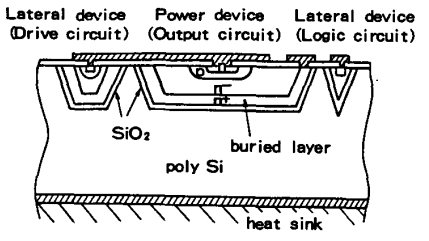

Fig.1 Conventional DI method(after[7])

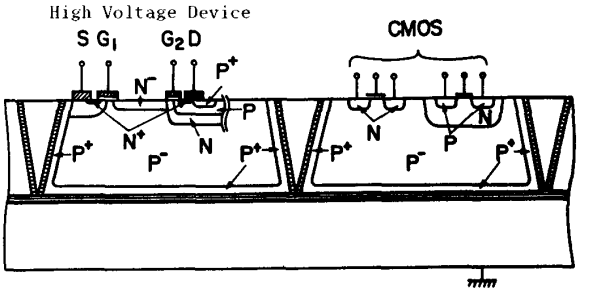

Fig.2 Dielectric Isolation by Silicon wafer Direct-Bonding(DISDB)(after[45])

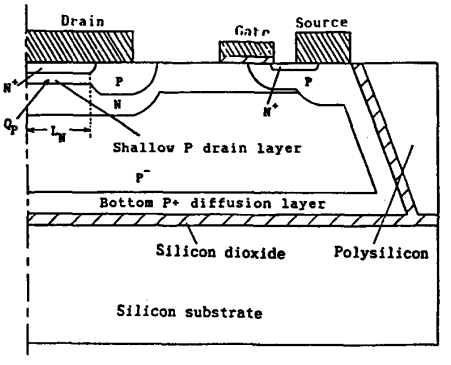

Fig.3 New high speed LIGBT structure with N-diffusion layer in P-drain(after[30,31])

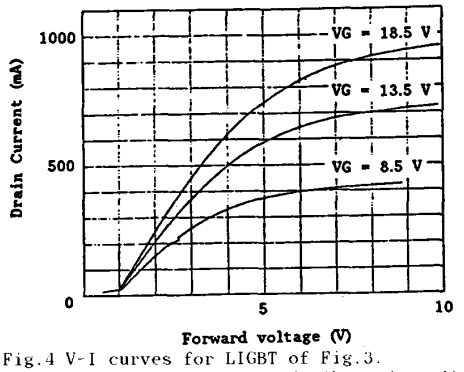

Fig.4 V-I curves for LIGBT of Fig.3. High speed is attained wihout degrading forward voltage for low current level. (after [31])

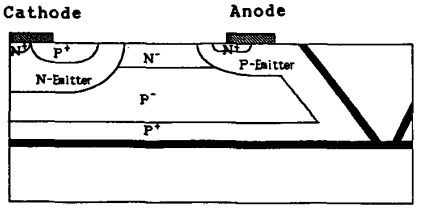

Fig.5 New high speed diode structure.

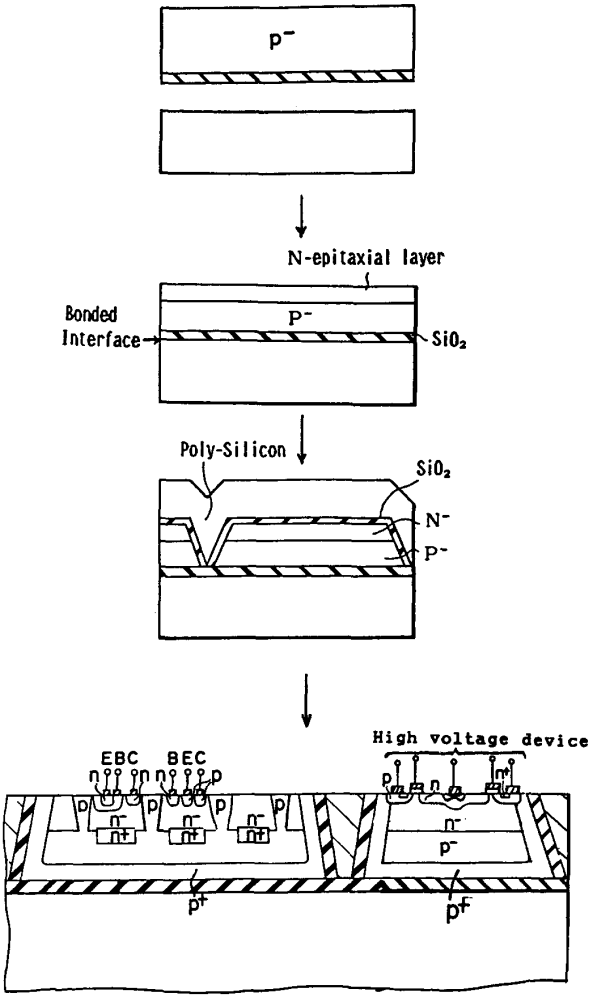

Fig.6 New DISDB substrate, merging DI and JI, and its fabrication processes. Logics are isolated by conventional JI in single DI island.

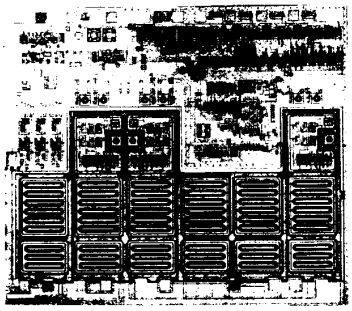

Fig.7 Developed 500V 1A 3-phase inverter IC chip.

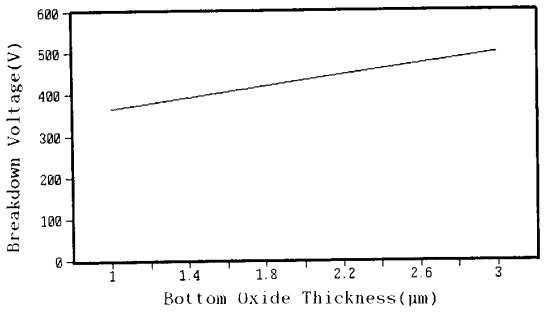

Fig.8 Breakdown voltage of 20μm thick lateral diode as a function of bottom oxide thickness.

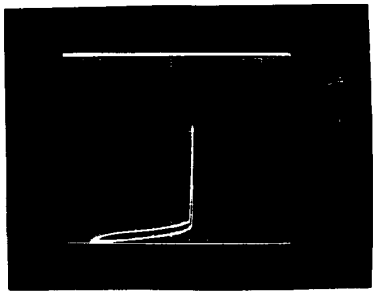

Fig.10 600V breakdown voltage was obtained for the fully depleted diode of Fig.9

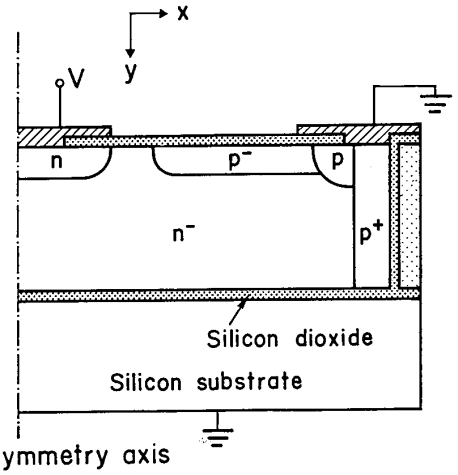

Fig.9 High voltage fully depleted diode on 20μm thick SOI(after [41]).

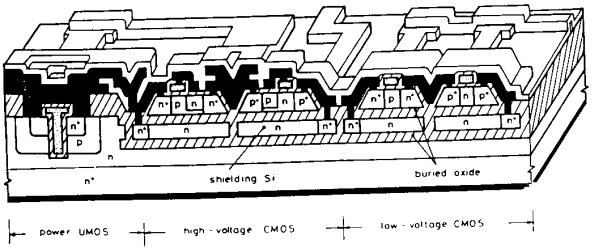

Fig.11 High voltage SOI based on SIMOX(after [42]).

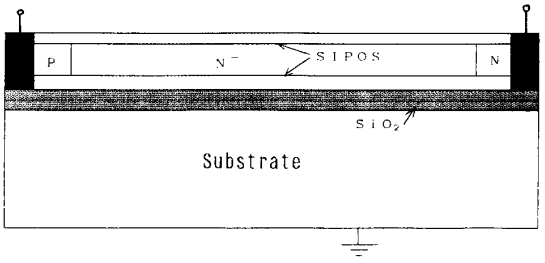

Fig.12 Proposed high voltage SOI structure using SIPOS shielding layer.

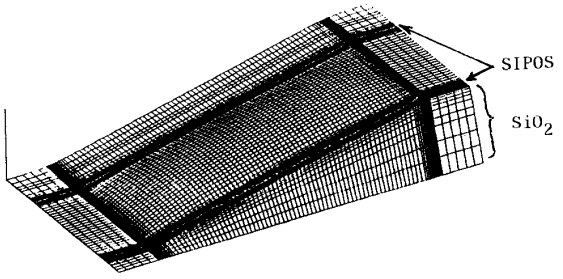

Fig.13 Calculated electric potential for the structure of Fig.12
SIPOS layer completely shield effect of substrate potential.

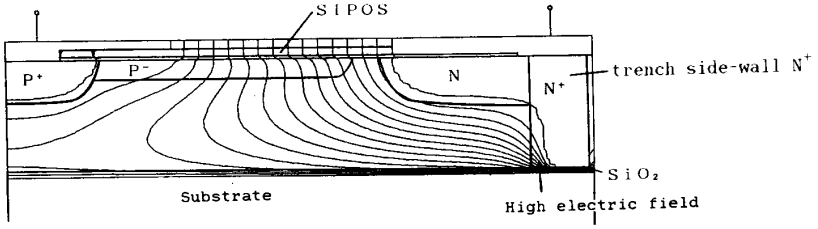

Fig.14 Calculated electric potential distribution for a LIGBT with a source surrounded by drain N^+ layer(trench side-wall N^+ diffision). High electric field appears at the portion where the arrow indicates.

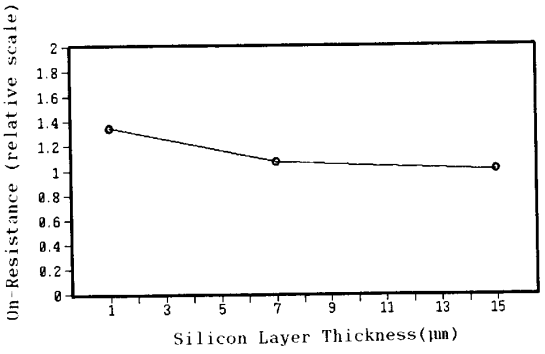

Fig.15 Calculated on-resistance of LIGBT vs. Silicon Layer Thickness(μm)

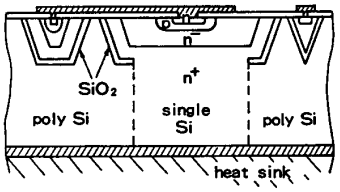

Fig.16 DI method(VLCS) for a vertical device with a contact on the back of chip (after [43])

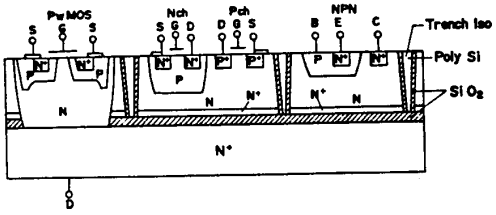

Fig.17 DI method(DISDB) for a vertical device with a contact on the back of chip (after [44])

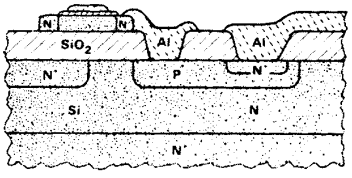

Fig.18 DI method(ZMR) for a vertical device with a contact on the back of chip (after [39])