Proceedings of 1990 International Symposium on Power Semiconductor Devices & ICs, Tokyo, pp.97-101

NEW 500V OUTPUT DEVICE STRUCTURES FOR THIN SILICON LAYER ON SILICON DIOXIDE FILM

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Abstract

Studies into a 20 μm deep trench technique for dielectric isolation and a high voltage lateral device structure for thin silicon layers have been carried out. These techniques can be applied to high voltage power ICs with high density packing. These proposed structures are characterized by a very shallow N-type diffusion layer on a bottom film of relatively thick silicon dioxide. Breakdown simulation was carried out by means of the two-dimensional device simulator TONADDEIIB. It was shown that a breakdown voltage of more than 500 V can be obtained with a 20 μm thick silicon layer structure.

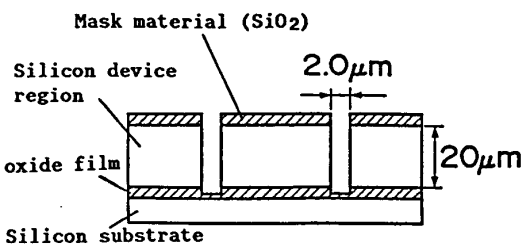
1. Introduction

Dielectric isolation is a reliable technique for high voltage power ICs, especially for ICs with a breakdown voltage above 500 V. Several techniques have already been proposed for such dielectric isolation[1,2]. Key requirements for optimum dielectric isolation are the ability to pack devices at high density and the suitability of the technique for large diameter wafer handling. Trenches are a very attractive means of device isolation, but trench depth is limited by the lack of a good mask material for selective RIE and by difficulties in filling deep trenches.

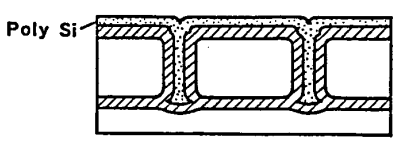
This paper reports a 20 μm deep trench technique as well as a high voltage device structure on thin silicon layer/silicon dioxide. It is shown that combination of these two techniques has the potential for ideal dielectric isolation, leading to future high voltage large current power ICs.

An important issue is how to ensure a high breakdown voltage, when a high voltage device is isolated from a substrate at earth potential only by means of a thin oxide film. The substrate potential has a major influence on the device breakdown voltage through the thin oxide film when the silicon layer is completely depleted. This effect was not observed in high voltage devices on conventional SOS (silicon on sapphire) layers, because the insulating layer is very thick.

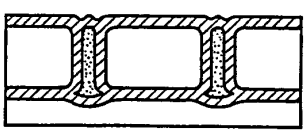
This paper describes appropriate structures for 500 V high voltage IC output devices on a 20 μm deep silicon layer over a thin oxide film. The work is based on numerical simulations.



(1)Forming 20 μm deep trenches



(2)Thermal oxidation and polysilicon filling



(3)Polysilicon etch-back and thermal oxidation

Fig.1 Process flow chart for deep trench isolation.

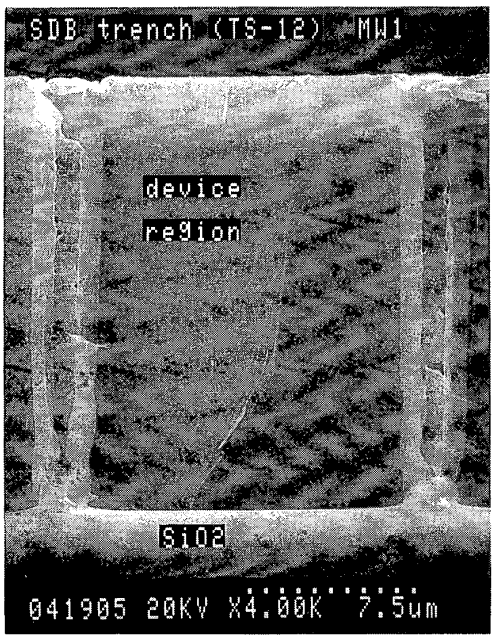


Fig.2 20 μm deep trench isolated silicon island.

2. Processing techniques for high voltage power ICs

Wafer direct-bonding[3] and deep trench techniques are a good combination for a high voltage, high density power IC structure. A relatively thick silicon layer is necessary to attain low on-resistance in high voltage devices, and a 20 μm deep trench technique has been developed for this purpose. The process flow chart for 5-inch diameter wafer fabrication is illustrated in Fig.1. Initially 20 μm deep trenches are formed, using a deposited SiO_2 film more than 2 μm thick as a selective etching mask. After N+ or P+ dopant deposition on the trench walls, thermal oxidation and polysilicon filling are carried out consecutively. The final smooth surface finish is attained by polysilicon etch-back and thermal oxidation. Figure 2 is a photograph of the resulting trench isolated silicon island.

Wafer direct-bonding is advantageous for utilizing a thick bottom film of silicon dioxide because wafer warpage problem is not so significant. Five-inch diameter wafers can be easily fabricated with a warpage of less than 20 μm.

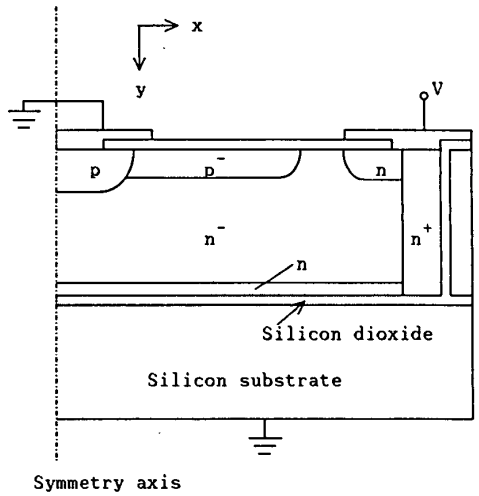


Fig.3A

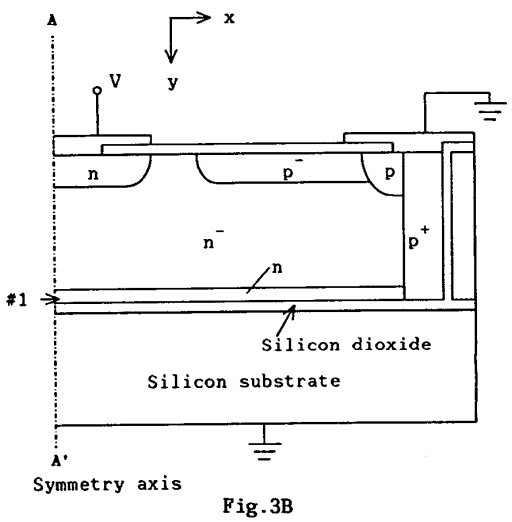


Fig.3B

Fig.3 Two proposed 500 V device structures for thin silicon layer/silicon dioxide/ silicon substrate structures.

3. Device structure optimization using breakdown voltage simulator TONADDEIIB

Figure 3 shows the two proposed output device structures, which are characterized by a thin silicon layer with a shallow N-type diffusion layer directly on a bottom film of silicon dioxide. The shallow diffusion layer is formed prior to wafer

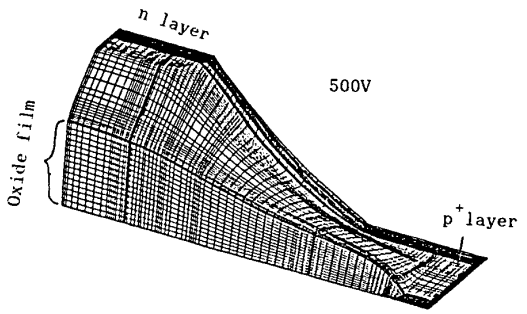


Fig.4 Calculated potential distribution for the structure in Fig.3B.
More than half of the applied voltage falls across the silicon dioxide film.

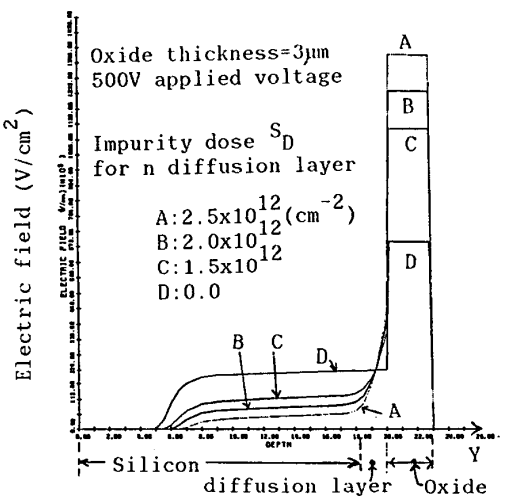


Fig.5 Electric field distribution along the symmetry axis. A high electric field is successfully applied in the oxide film.

direct-bonding. The source and drain electrode configurations are reversed in the two different structures.

For simplicity, lateral diode structures were adopted to optimize the device structure. The breakdown voltage was calculated by estimating the ionization integral[4] using TONADDEIIB[5].

If the device structure is optimized such that a large proportion of the applied voltage is carried by the bottom film of silicon dioxide, a breakdown voltage of more than 500 V is achieved even with a 20 μm silicon layer. Figure 4 shows an example: the 20 μm silicon layer is completely depleted and half of the applied voltage

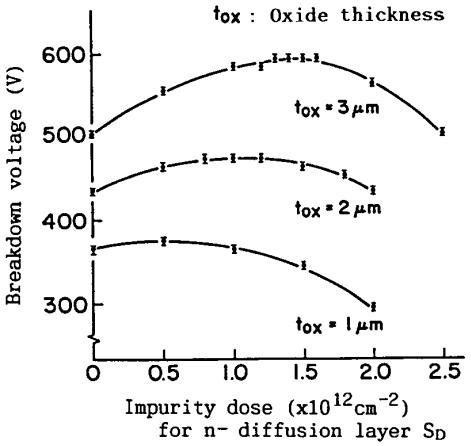


Fig.6 Breakdown voltage vs. impurity dose for shallow diffusion layer characteristics in the structure of Fig.3B.

falls across the silicon dioxide film when a 500 V reverse voltage is applied to the optimized device in Fig.3B.

An appropriate amount of the impurity dose in the bottom N-type shallow diffusion layer improves the breakdown voltage. The problem is how to apply a high electric field across the silicon dioxide film without increasing the field strength inside the bulk silicon layer. In this structure,the ionized shallow N-type diffusion layer acts as a shield for the high electric field within the silicon dioxide film. The impurity dose in the bottom diffusion layer and the layer depth are both key parameters, in addition to the oxide film thickness, which is naturally one of the factors having most influence.

Figure 5 shows the electric field distribution along the symmetry axis AA' of device B for various values of total impurity dose S_D in the bottom shallow N-type diffusion layer. It is seen that ionized donors in the shallow diffusion layer contribute to a rapid fall in electric field strength inside the silicon layer.

Figure 6 shows the dependence of breakdown voltage on the impurity dose S_D for various thicknesses of silicon dioxide film. Avalanche breakdown was always observed at the point marked by #1 in Fig.3B. A breakdown voltage of 580 V can be obtained with a 3 μm silicon dioxide film and on N-type bottom diffusion layer a few microns thick. The silicon dioxide film should be as thin as possible to reduce wafer-warping.

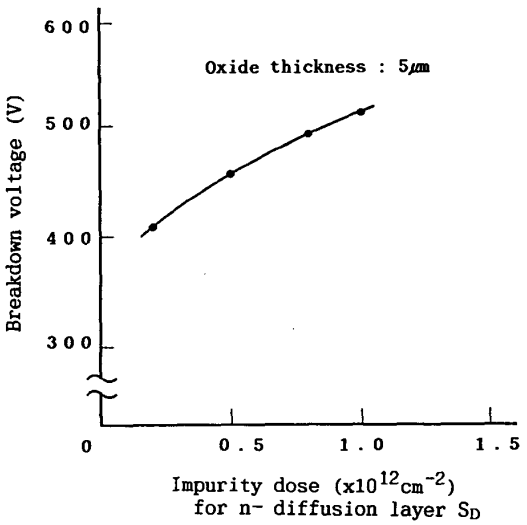


Fig.7 Breakdown voltage vs. impurity dose for shallow diffusion layer characteristics in the structure of Fig.3A.

Figure 7 shows a similar result for structure A. With this structure, a thicker silicon dioxide film of 5 μm is required to obtain a breakdown voltage greater than 500 V. Thus, in terms of breakdown voltage characteristics, structure B has the advantage.

The surface P- RESURF[6] layer has little influence over the device breakdown voltage, and can be removed if a SIPOS[7,8] resistive field plate is adopted.

The proposed structure can be applied to various high voltage lateral devices, including lateral IGBTs[9], and it makes dielectrically isolated power ICs a more promising prospect.

4. High-voltage power IC structure on a 20 μm thin silicon layer/ silicon dioxide substrate.

One possible future power IC structure is the one shown in Fig.8, in which the new high voltage technique is applied to lateral IGBTs. CMOS logic circuits will be fabricated on a single silicon island and each bipolar logic area and high voltage device will be isolated by trenches. If the high voltage structure B is simply adopted, both P+ and N+ trench wall diffusions will have to be carried out, but there may be some means to eliminate the P+ side-wall diffusion. One possibility, for example, is to adopt device structure A with a thicker bottom film of oxide as shown in Fig.9.

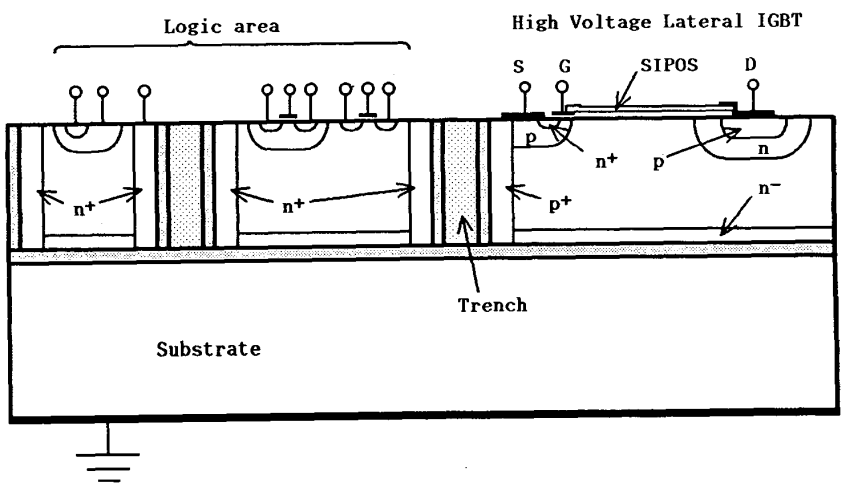


Fig.8 Deep trench isolated power IC with structure of Fig.3B.

5. Conclusion

Deep trench isolation combined with silicon wafer direct-bonding is a promising technique for future high density high voltage dielectrically isolated power ICs, utilizing more than 5 inch diameter wafers. A 20 μm deep trench technique has been developed as a step toward realization of such ICs.

It was shown numerically that a breakdown voltage of more than 500 V can be obtained by forming a shallow N-type diffusion layer with an appropriate impurity dose on the bottom of the lateral device.

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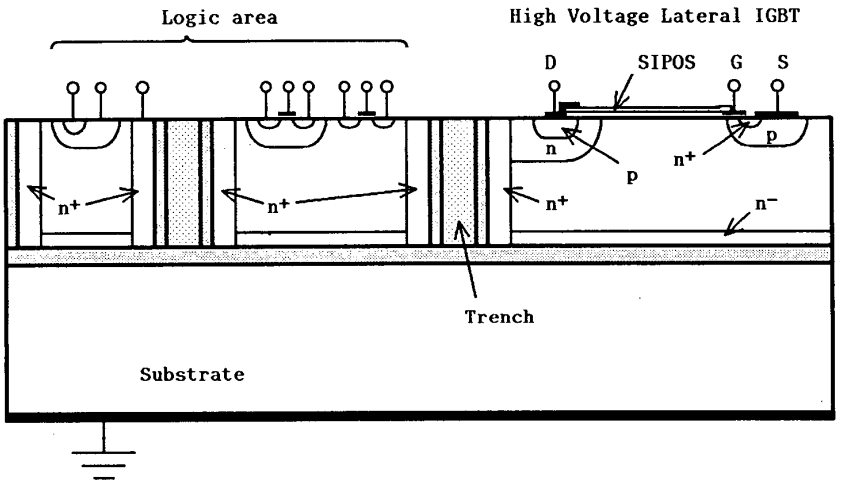

Fig.9 Deep trench isolated power IC with structure of Fig.3A.