Proceedings of 1990 International Symposium on Power Semiconductor Devices & ICs, Tokyo, pp.252-255 **6.2.5**

HIGH FREQUENCY 6000 V DOUBLE GATE GTOs WITH BURIED GATE STRUCTURE

T. Ogura, A. Nakagawa, M. Atsuta, Y. Kamei and K. Takigami

Research and Development Center, Toshiba Corp.,
1, Komukai Toshiba-cho, Saiwai-ku, Kawasaki-shi 210, Japan
Phone: 044-549-2138, Fax: 044-555-2074

ABSTRACT

A new double gate GTO with buried gate structure for a second gate has been proposed to realize high turn-off gain simultaneously with low turn-off switching loss. The double gate GTO has been combined with an n-buffer structure to realize 6000 V forward blocking voltage with a narrow n-base width, such as 550 μm. The high turn-off gain, such as 6, was obtained when the anode current was 500 A. It was found that the double gate GTOs with buried gate realize a very short tail time and a small tail current. The newly developed double gate GTOs decrease the turn-off loss to less than 1/10 of that for the conventional single gate GTOs.

INTRODUCTION

High power gate turn-off thyristors (GTOs) have been applied as key switching devices in inverters for industrial apparatus, such as motors and uninterruptable power supplies. 6000 V GTOs have already been developed for these applications [1]. However, it is desirable to develop higher frequency GTOs to realize highly efficient operation for these inverters. The main two problems in developing higher frequency GTOs are a large on-state voltage and large switching loss caused by a large n-base width to sustain a high forward blocking voltage.

An n-buffer structure is most suitable for high blocking voltage GTOs, because the n-base width for this structure is reduced to approximately 55 % of that for a reverse blocking structure, and to approximately 75 % of that for an anode short structure [1]. However, the maximum operational frequencies, even at the n-buffer GTOs, were limited to less than 1 kHz. The most difficult problem in realizing higher frequency operation for the n-buffer GTOs is large turn-off loss, caused by large amount of excess carriers in the n-base region.

A double gate GTO has already been proposed to attain high blocking voltage, such as 6000 V, simultaneously with low turn-off loss [2]. A second gate, fabricated on the n-base layer, sweeps away the excess carriers in the n-base at turn-off stage, thus reducing the turn-off loss. However, a large amount of the second gate current was required to decrease the turn-off loss considerably, because the turn-off gain for the second gate is low.

In this paper, a new buried gate structure for the double gate GTOs is proposed to realize high turn-off gain simultaneously with the low turn-off loss. The buried gate structure influence on the on-state voltage for the GTOs was investigated experimentally. Turn-off characteristics, such as turn-off gain for second gate, tail time and peak value for tail current, are discussed. Experimental results, comparing the turn-off loss for the double gate GTOs and conventional single gate GTOs, are presented.

DEVICE STRUCTURE

The device structure and the doping profile for the newly developed double gate GTO are shown in Figs. 1 and 2. A buried layer was fabricated in the n-buffer layer by a selective diffusion of high concentration n-type impurities. A low concentration n-type layer was fabricated on the n-buffer layer by an epitaxial growth process.

The n-buffer layer, with a fine meshed buried layer of high doping concentration, substantially reduce the lateral resistance for the n-buffer layer. A low concentration region in the n-buffer layer was fabricated through which the injected excess carriers from the p-emitter and n-emitter regions flow. The low doping concentration layer, fabricated between the n-buffer layer and a p-emitter layer, increase the breakdown voltage between the anode and second gate. A more than 200 V reverse blocking voltage was obtained by this structure, as shown in Fig. 3.

ELECTRICAL CHARACTERISTICS

The double gate GTOs with buried gate structure have been combined with the n-buffer structure, as indicated in Fig. 1, to realize 6000 V with a narrow n-base width. A 6000 V forward blocking voltage was realized by the n-buffer structure with only 550 μm n-base width, approximately 75% of the n-base width for anode short GTOs. The forward blocking voltage at a 1 mA leakage current dependences on junction temperature, for the double gate GTO and anode short GTO, are shown in Fig.4. This figure shows that the double gate GTOs sustain 6000 V forward blocking voltage at 150 °C junction temperature, 35 °C higher than that for the anode short GTOs. This is because the double gate GTOs can suppress the hole injection from the p-emitter by shorting the second gate to the anode electrode at the forward blocking stage.

The pattern for the buried gate layer was determined by the on-state voltage dependence on the distance between the buried layers, because the high concentration layer for the buried gate increases the on-state voltage for the GTOs. The on-state voltage characteristics for the double gate GTOs with three different buried gate distances, are shown in Fig. 5. This figure also shows the on-state voltage characteristics for the device without the buried gate layer. It was found that the on-state voltage increases as the distance between the buried layers narrows. The on-state voltage increases rapidly, when the distance between the buried layers is 30 μm . This increase in on-state voltage was caused by the restriction against current passage in the on-state by the high concentration layers for the buried gate. It was concluded that a suitable value, for the distance between the buried layers, is less than 120 μm.

The newly developed double gate GTOs realize high turn-off gain at the second gate. Typical turn-off waveforms for the anode current, anode voltage, first gate current and second gate current are shown in Fig.6. This device can turn off 700 A anode current, when the first and second gate currents are approximately 130 A and 90 A, respectively, as shown in this figure. The excess carriers in the n-base region can be swept away by the small amount of second gate current. This high turn-off gain at the second gate was caused by the reduction in the internal resistance for the second gate and the increase in the breakdown voltage at the junction between second gate and p-emitter layers. Figure 7 shows the second gate turn-off gain dependence on the anode current. The turn-off gain increases in proportion to the anode current. The 6 turn-off gain can be obtained, when the anode current is 500 A. This confirms that the buried gate structure can realize high turn-off gain at the second gate.

It was also found that the newly developed double gate GTO can realize a very short tail time and small tail current, as shown in Fig. 6. The tail time and peak tail current dependences on the anode current are shown in Fig. 8. In contrast to conventional GTOs, the tail time decreases with increasing anode current. This tail time dependence is a distinctive advantage, obtained by the buried gate structure. The short tail time can reduce the turn-off loss at a large anode current region. The very short tail time, such as 2 μs, was obtained when the anode current was 500 A, as also shown in Fig.8. The peak tail current for this GTO increases with increasing the anode current, the same as that for the conventional GTOs. However, this peak value increases only approximately two times, with increasing the anode current from 100 A to 500 A. This peak tail current dependence is also a distinctive advantage at the buried gate GTOs. It is considered that these two advantages were obtained by the effect of sweeping away the excess carriers in the n-base during the storage period by the second gate.

The double gate GTOs can decrease the turn-off switching loss by the second gate operation. Figure 9 shows the turn-off loss dependence on the anode current, for the single gate GTO and the double gate GTO. The turn-off loss for the double gate GTO was reduced to less than 1/10 of that for the single gate GTO over a wide anode current range. This is because the tail time and the tail current were decreased by the second gate effect, as mentioned before. Therefore, the newly developed double gate GTO can realize low turn-off loss, simultaneously with 6000 V forward blocking voltage.

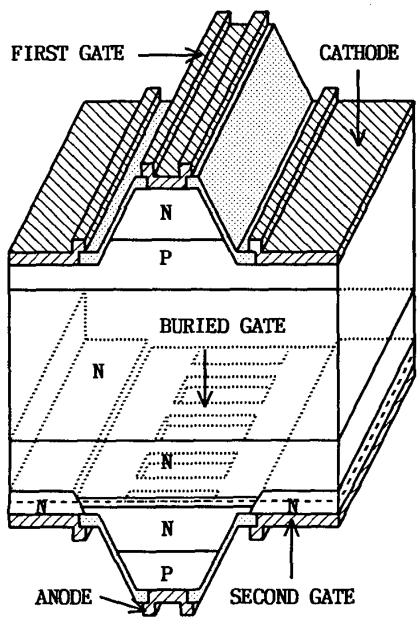
CONCLUSION

The on-state voltage and turn-off characteristics for the newly developed 6000 V double gate GTOs with buried gate have been investigated experimentally. The double gate GTOs with n-buffer structure sustain 6000 V forward blocking voltage, even at 150 °C junction temperature. The suitable value for the distance between buried layers is less than 120 μm to suppress the enormous increase in on-state voltage. The buried gate structure for the double gate GTOs realize high turn-off gain, such as 6, for the second gate operation. Also, the very short tail time and small tail current are realized by the second gate operation. This device reduces the turn-off loss to less than 1/10, compared with conventional single gate GTOs.

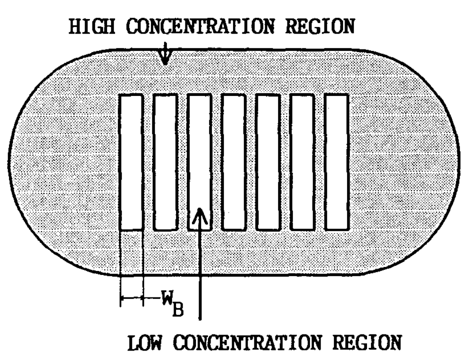
REFERENCES

[1] T.Ogura,et.al, "Low Switching Loss, High Power Gate Turn-off Thyristors (GTOs) with N-buffer and New Anode Short Structure", PESC'88 Record, pp.903-907, 1988.

[2] T.Ogura, et.al, "High Frequency 6000 V Double Gate GTOs", IEDM'88 Record, pp.610-613, 1988.



(a) Cross-sectional view of unit double gate GTO with buried gate structure.



(b) Buried structure top view.

Fig.1 Device structure for double gate GTO with buried gate structure.

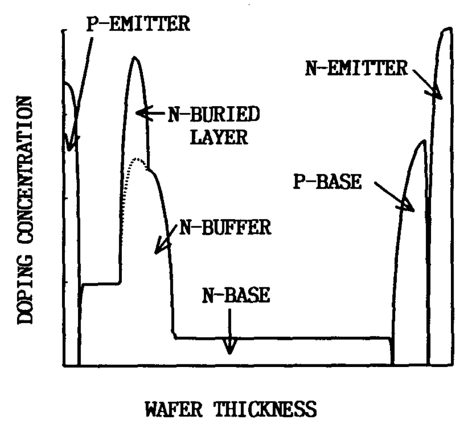


Fig.2 Doping profile for double gate GTO with buried gate structure.

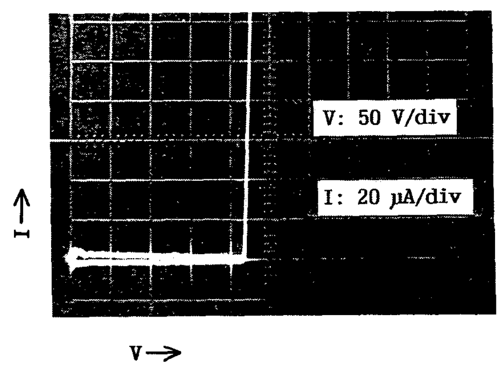


Fig.3 Reverse blocking characteristics for second gate of double gate GTO with buried gate.

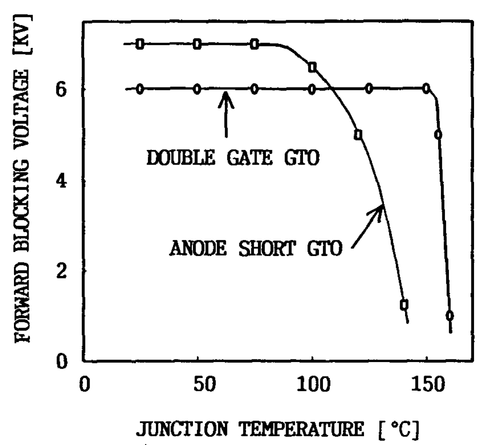


Fig.4 Forward blocking voltage dependence on junction temperature for double gate GTO and anode short GTO.

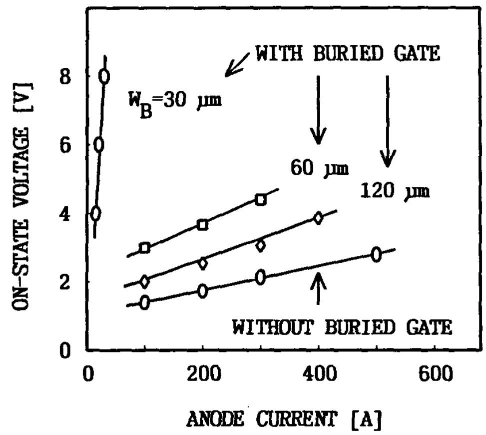


Fig.5 On-state voltage dependence on anode current for double gate GTOs with and without buried gate.

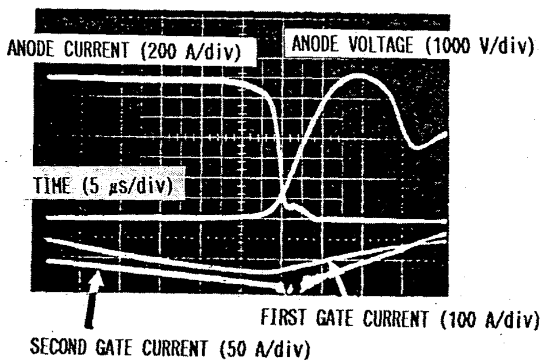


Fig.6 Turn-off waveforms for anode voltage, anode current, first gate and second gate currents for double gate GTO with buried gate.

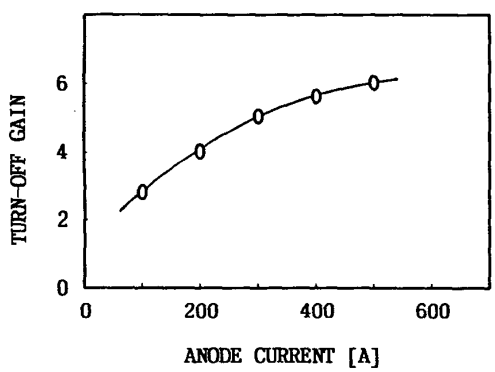


Fig.7 Second gate turn-off gain dependence on anode current for double gate GTO with buried gate.

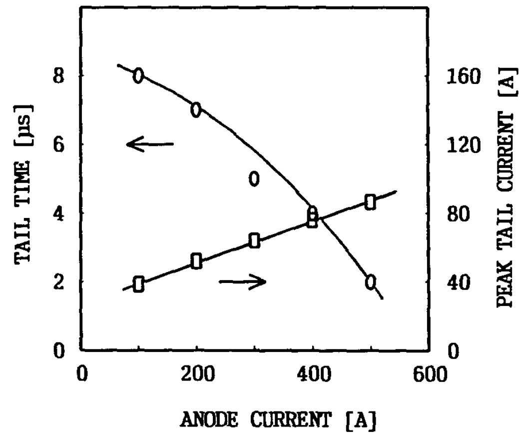


Fig.8 Tail time and peak tail current dependences on anode current for double gate GTO with buried gate.

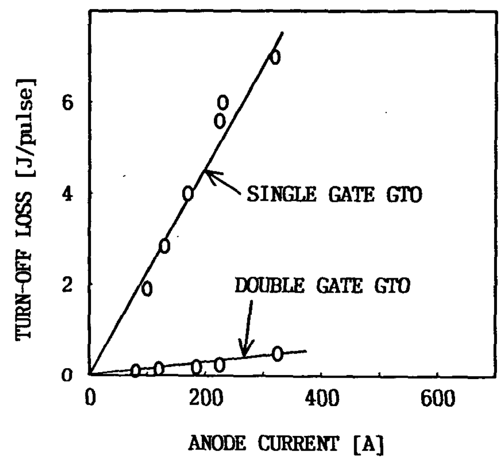


Fig.9 Turn-off losses dependence on anode current for double gate GTO and single gate GTO.