Proceedings of 1990 International Symposium on Power Semiconductor Devices & ICs, Tokyo, pp.180-185

SMALL WARPAGE DIELECTRICALLY ISOLATED WAFER FOR POWER ICs BY SILICON WAFER DIRECT-BONDING

K.Furukawa, A.Nakagawa, K.Tanzawa and N.Kawamura

Toshiba Research & Developement Center, Toshiba Corp.
1 Komukai Toshiba-cho, Saiwai-ku, Kawasaki, 210, Japan
Tel. 044-549-2138 / FAX 044-555-2074

Abstract

The warpage mechanism was investigated for dielectlically isolated wafers, fabricated by the direct bonding. Three factors affecting the warpage were revealed. They were elastic deformation, a phenomenon peculiar to the direct bonding and poly-Si deposition. The investigation on these factors reduce the warpage to a few microns for 3 inch diameter wafers. Six inch diameter wafers were directly bonded to obtain 5 inch diameter SOI wafers. The warpage for the SOI wafer was 13 to 34 μm. These results show that a 5 inch dielectlically isolated wafer can be applicable to power IC fabrications.

Introduction

DI (Dielectrical isolation), usually using an SOI (Silicon On Insulator) wafer, has attracted much attention for high voltage power ICs, as well as for high-speed and high-density VLSI devices. Many techniques, such as recrystallization, SIMOX, FIPOS etc., is being developed. Only EPIC (Epitaxial Passivated Integrated Circuit) [1] has been utilized for power ICs. However, large warpage, due to thick poly-Si deposition, limits the EPIC DI wafer diameter to no larger than 4 inches and prevents fine patterning.

Recently, an SDB (Silicon wafer Direct-Bonding) technique [2] has been successfully applied to DI devices, such as a photo-diode array [3] and a lateral IGBT [4]. The SDB technique has a potential to realize a thick and defect free single crystal large diameter SOI layer for high voltage power ICs.

In order to fabricate a large diameter DI wafer, large wafers must be bonded all over the surfaces. Although, small warpage is the advantage of SDB DI wafer[5], the warpage must still be decreased as wafer diameter increases. In this work, 6 inch wafers were directly bonded, and the mechanisms for SDB DI wafers were investigated.

Direct bonding and DI wafer process

A pair of 6 inch diameter wafers were directly bonded. Mirror surfaces for two wafers were contacted and the wafers adhered to each other at room temperature. High temperature annealing completed the bonding. The detailed bonding method was similar to that reported[2,5] for smaller wafer bonding. Bonding equipment and atmosphere cleanness were improved, in order to achieve voidless bonding. Figure 1 shows a infrared image for the bonded wafer. The entire wafer surface is bonded,

except for the rim of wafers, due to the rounded wafer edge shape.

Typical SDB DI wafers are fabricated in the manner shown in Fig.2. This figure shows DI wafer fabrication processes and cross-sectional photographs taken during the processes. First, a silicon wafer with an oxide layer on its surface, called an SOI wafer in this paper, is bonded to a substrate wafer, with or without an oxide layer. A thermally grown oxide layer is preferable, because a mirror surface is kept, even after oxidation.

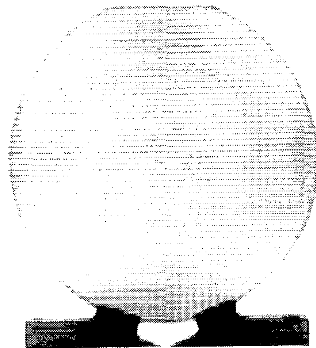


Fig. 1
Infrared image for directly bonded 6 inch diameter wafers.

The bonded wafer diameter is decreased by cutting off the rim to remove the unbonded part. For example, 6 inch wafers are bonded to obtain a 5 inch DI wafer.

The SOI layer thickness is reduced to a suitable thickness for the devices, which is fabricated later. V-shaped grooves are made by anisotropic etching. The silicon islands are electrically isolated by the oxide layer on the side-wall of the grooves. The grooves are filled with deposited poly-Si. Finally,

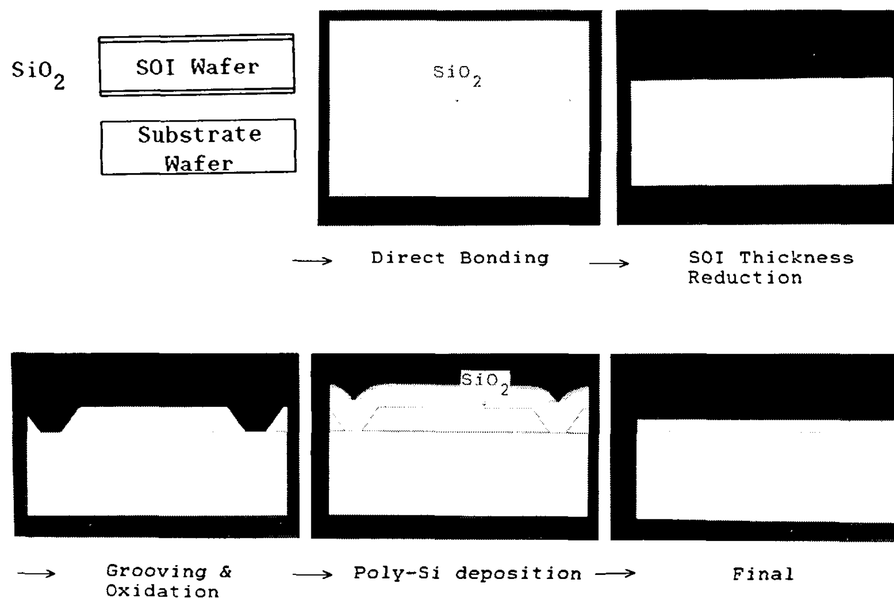
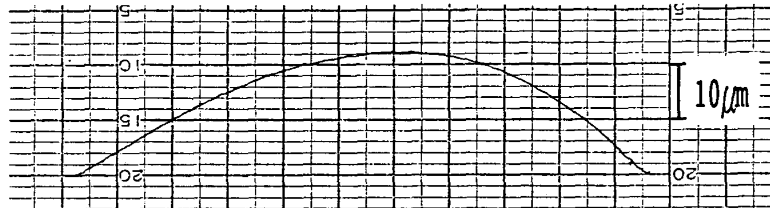


Fig. 2 Cross-sectional photographs for SDB DI wafer during typical wafer fabrication processes.

Fig. 3
Warpage for
5 inch diameter
SDB SOI wafer.



extra poly-Si is lapped out and the wafer surface is mirror polished.

The warpage for the 3 inch diameter SDB DI wafer was below 10 μm [6]. This value is small enough to allow fabricating a photodiode array and a lateral IGBT. However, the warpage increases, as the wafer diameter increases. Figure 3 shows the warpage for One of 5 inch SOI wafers. These wafers were obtained by the 6 inch wafer bonding. After the SOI thickness reduction, the warpage were 13 to 34 μm.

When more complicated devices or circuits are fabricated on a larger diameter DI wafer, the wafer warpage must be still further decreased. For example, Fig. 4 shows the wafer structure and fabrication processes for a power IC being developed[7]. Islands for 500 V IGBT and islands for low voltage logic devices are integrated. IGBT islands are P-type, because it was confirmed [8] that fall-time for an IGBT in a p-type Si island is smaller than that in an n-type Si island. Junction isolated n-type wells for bipolar transistors exist in the logic device islands. The wells are filled by epitaxial Si, simultaneously grown with poly-Si deposition. The well depth is adjusted by the final polishing. Small wafer warpage is necessary for accurate polishing.

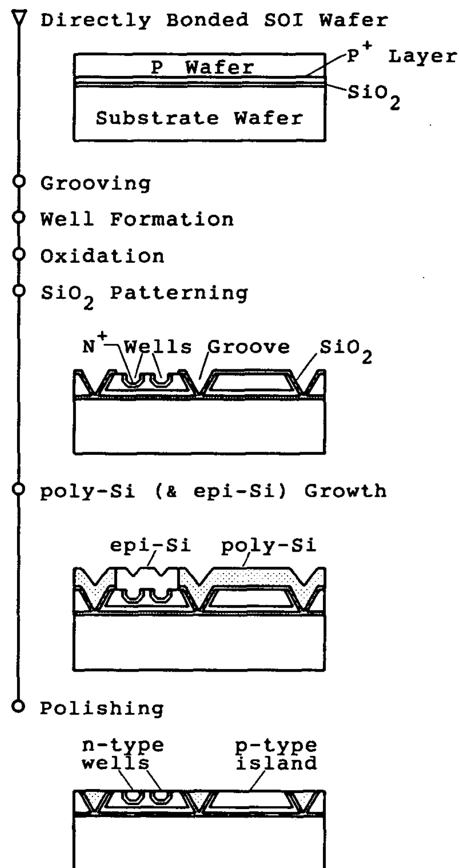


Fig. 4
Fabrication process and structure for SDB DI wafer for power IC.

Warpage for SDB DI wafer

The warpage for the SDB DI wafer was investigated. Figure 5 shows the warpage change during the SDB DI wafer fabrication processes shown in Fig. 1. Three factors affecting the warpage were revealed. They are elastic deformation, a phenomenon peculiar to the direct bonding and poly-Si deposition. The final warpage is a few microns for 3 inch diameter wafers. This small warpage value was achieved by the following investigation.

In Fig. 5, convex wafer warpage was observed, after SOI layer thickness was reduced. This warpage is elastic deformation. To investigate the elastic deformation, a pair of wafers with various oxide layer thicknesses were bonded. The warpage was measured after one of the bonded wafers was thinned. Figure 6 shows the relationship between the warpage and oxide thickness. The circles indicate the measured value. The warpage increases in proportion to the SiO_2 thickness, showing that the sandwiched SiO_2 is the warpage driving force.

The mechanism for this warpage is considered as follows. No stress exists in a bonded wafer during 1100°C anneal in the bonding process, because SiO_2 viscous flow occurs. As bonded wafer is cooled down, tensile and compressive stresses are generated in Si and SiO_2 layers, respectively. After the SOI layer is thinned, the compressively stressed SiO_2 moves from the symmetry center, and the SOI wafer is warped.

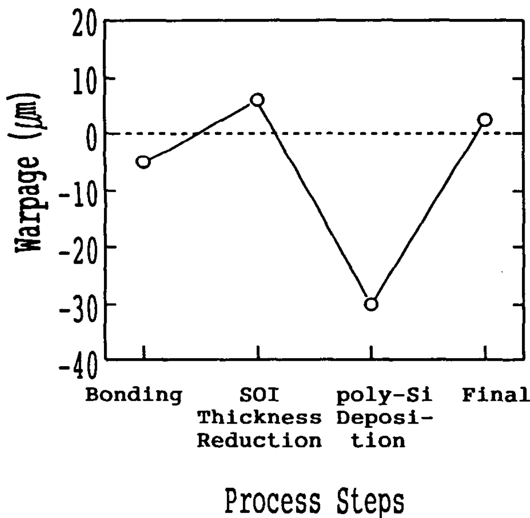


Fig. 5
Wafer warpage change during SDB DI wafer process described in Fig.2. Positive and negative values mean convex and concave warpage, respectively.
Wafer diameter is 3 inches.

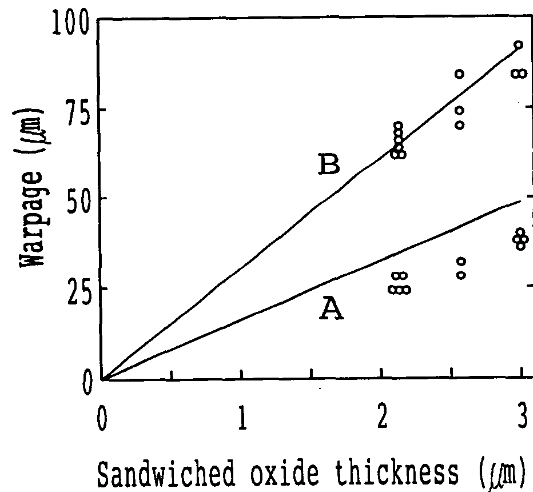


Fig. 6
Measured (circles) and calculated (lines) warpage for SDB SOI wafer after SOI thickness reduction.
Wafer diameter is 3 inches.
SOI layer thickness is 60µm.
Substrate wafer thicknesses are A: 525µm; B: 375µm.

The warpage was calculated, based on the above mentioned assumption, using a thin plate theory. The results are also shown in Fig. 6 by solid lines. The calculated value agrees with measured warpage, confirming that this warpage is attributed to the elastic deformation caused by thermal expansion difference between Si and SiO_2.

The elastic deformation is a dominant factor for the SDB DI wafer warpage. Therefore, the warpage is controllable by wafer design, such as sandwiched SiO_2 thickness or substrate wafer thickness. For the DI wafers in Fig. 5, SiO_2 thickness was designed to be 1μm, which is sufficient to isolate 500V devices. A 625μm thick substrate wafer was used. These wafer designs reduced the warpage to less than 10 μm, after the SOI layer thickness reduction, indicated in Fig. 5, from 20 to 90 μm as shown in Fig. 6.

When an oxidized wafer is bonded to a non-oxidized wafer, warpage peculiar to the direct bonding occurs. Figure 7 shows experimental processes and result for this bonding warpage. A pair of identical wafers, 4 inches in diameter and 400 μm in thickness, were bonded together. Only one wafer, the upper wafer in Fig. 7., had been oxidized. Just after the bonding, the bonded wafer has four layer structure, formed from surface oxide/ silicon/ sandwiched oxide/ silicon, as is shown at the middle the figure. A slight concave warpage was observed. The surface oxide was etched off to make the wafer symmetrical, with respect to the sandwiched oxide, as is shown at the right-hand side in the figure. Acording to the above mentioned elastic deformation theory, no warpage must be observed for a symmetrical wafer. However, the wafers warped. The oxidized wafer side (upper side in the figure) was concave. This warpage was not observed, when two oxidized wafers were bonded together.

The detailed mechanism for this bonding warpage is not clear. It is assumed that the stress relaxation,

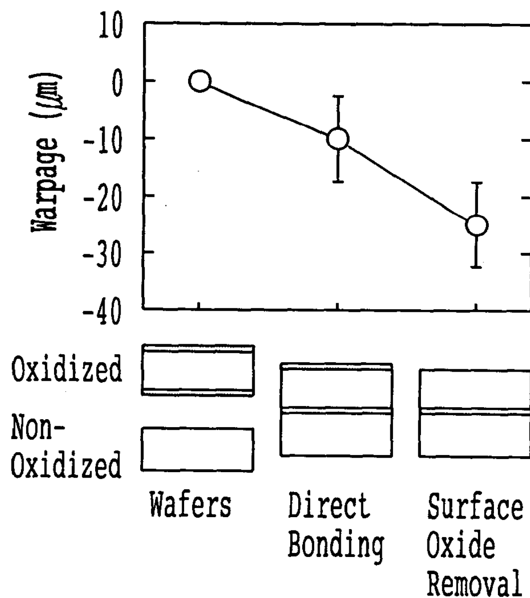


Fig. 7
Warpage change for bonded 4 inch diameter wafers, according to the experimental processes described at the lower part in the figure. Oxidized wafers are bonded to non-oxidized wafers. Oxidized wafer side is concave, when surface oxide layer is removed to make wafer structure symmetric.

during the bonding annealing generates the warpage. The stress relaxation occurs at the bonded Si/SiO_2 interface to reduce the tensile stress in the non-oxidized silicon wafer. On the other hand, the stress in the oxidized wafer is maintained, because no stress relaxation occurs at the oxidized Si/SiO_2 interface. The stress difference between the two wafers warps the bonded wafers.

For the SDB DI wafer processes in Fig. 5, the SOI wafers were oxidized and the substrate wafers were not. The concave warpage after bonding is the result of such wafer oxidation. The SOI wafer, in which devices are fabricated later, should be oxidized, because an oxidized Si/SiO_2 interface seems to be more stable than a bonded Si/SiO_2 interface. When only the SOI wafer is oxidized, the bonding warpage direction is opposite to the elastic deformation, so that the total warpage was reduced. This warpage reduction did not disappear, even after 1200°C heat treatment.

It is well known, in the EPIC wafer process[9], that a substrate is warped concave by the deposited poly-Si. This warpage is the weak point for an EPIC DI wafer. However, the warpage direction by poly-Si deposition is opposite to the elastic deformation for an SDB DI wafer. As is shown in Fig. 5, although the warpage by poly-Si deposition almost recovered after the wafer surface was polished and most poly-Si was removed, the SDB wafer warpage was reduced by optimized poly-Si deposition.

Conclusion

It has been revealed that three phenomena, elastic deformation, bonding warpage and poly-Si deposition, warp the SDB DI wafer. Because the elastic deformation caused by thermal expansion difference between Si and SiO_2 is dominant, the wafer warpage is controllable by sandwiched SiO_2 and/or substrate thickness. The other two phenomena can also reduce the warpage. A 3 inch diameter SDB DI wafer, with several micron warpage, was fabricated based on the investigation.

Six inch wafers were directly bonded all over the surfaces. A 5 inch SOI wafer was fabricated using the bonded 6 inch wafer. The warpage was sufficiently small, so that 5 inch diameter DI wafers can be applicable to power IC fabrications.

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