半導体アドバンスト講座　2013年10月3,4日

パワーデバイス

一般社団法人　半導体産業人協会

現職 中川コンサルティング事務所 コンサルタント
元職 東芝セミコンダクター社　首席技監
氏名 中川 明夫
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IGBTの発明実用化で、IEEE、大河内等表彰

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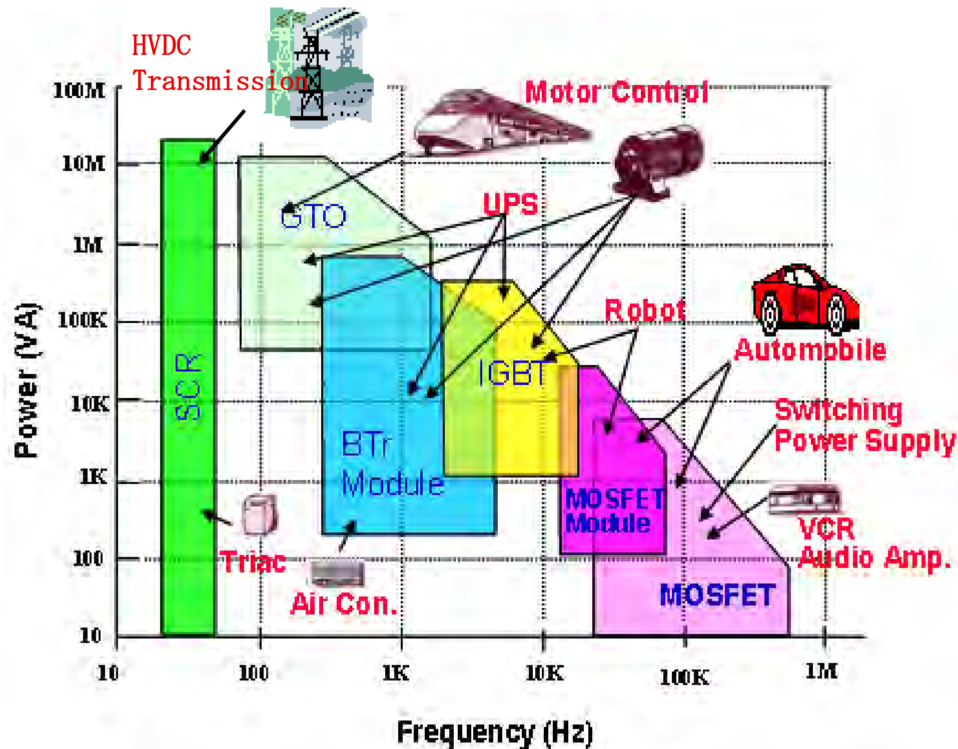
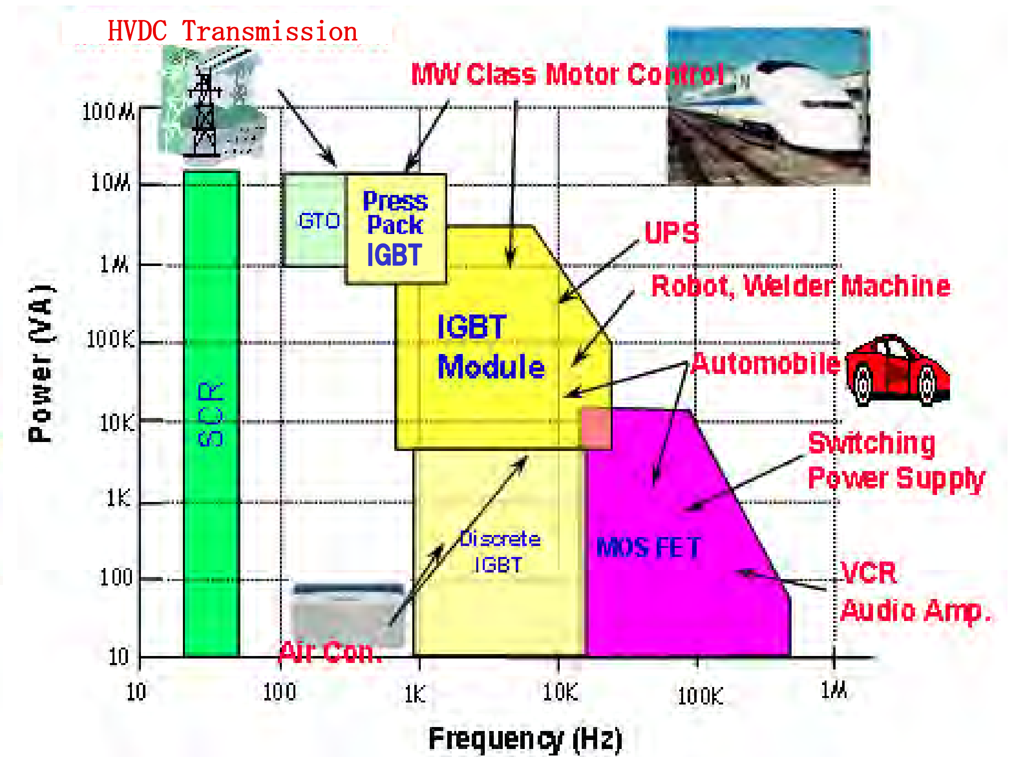
パワーデバイス応用分野の変遷

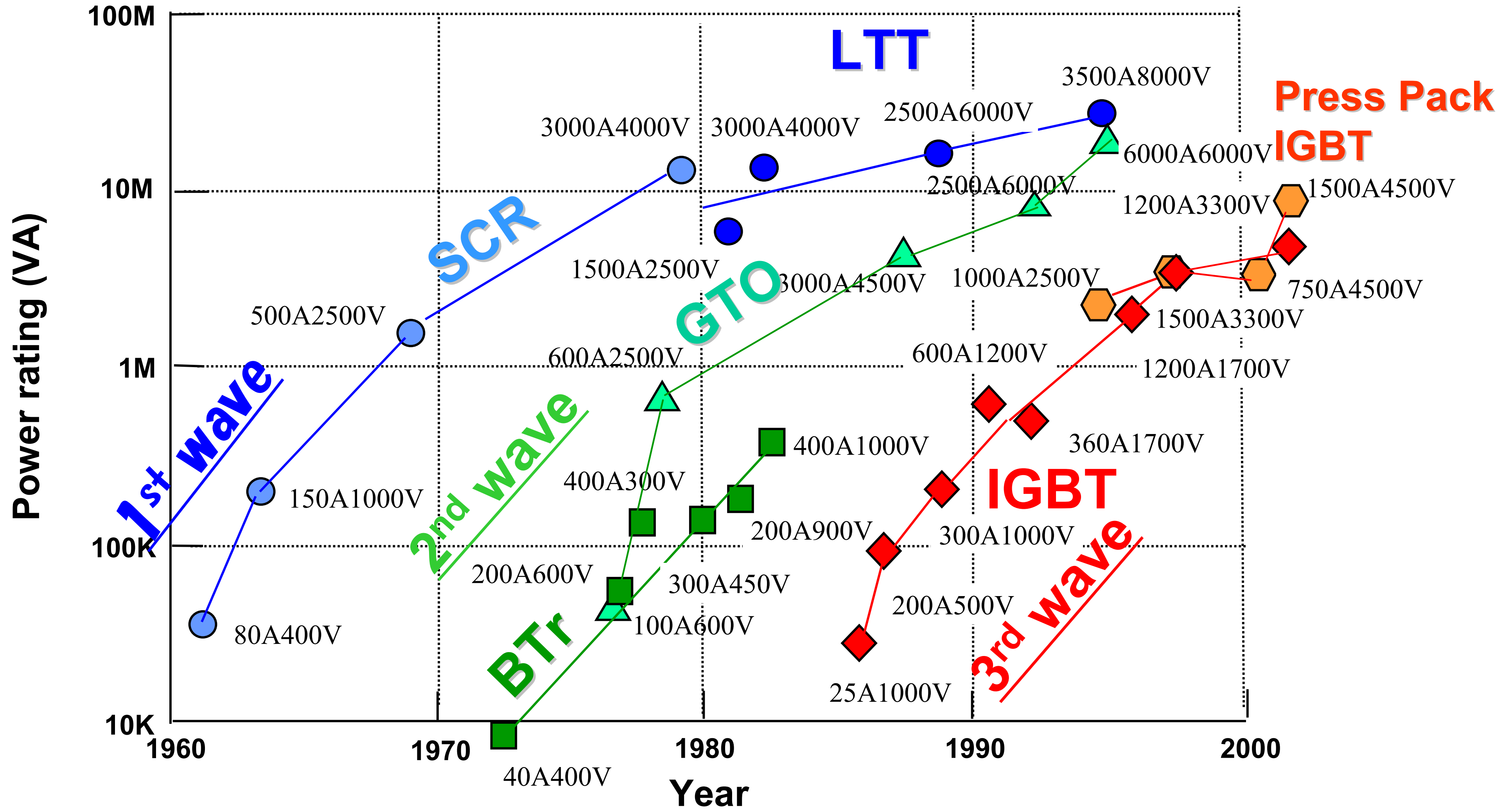
1997

2005





パワーデバイス発展の経緯（東芝の例）



GTOからIGBTに変わった新幹線のインバータ

インバータ駆動による高効率化

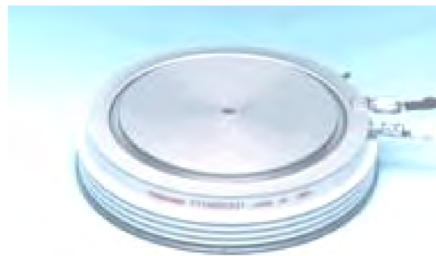
9 years

Model 300 (1990)

Model 700 (1999,2002)

GTO inverter

IGBT inverter



SG3000GXH24

ST1000EX21

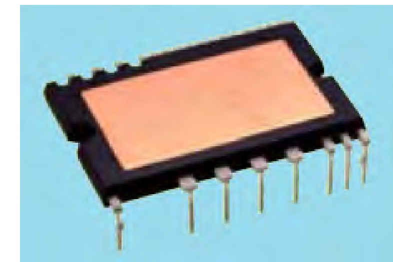
MG1200FXF1US53

IGBTの種類

Power Module

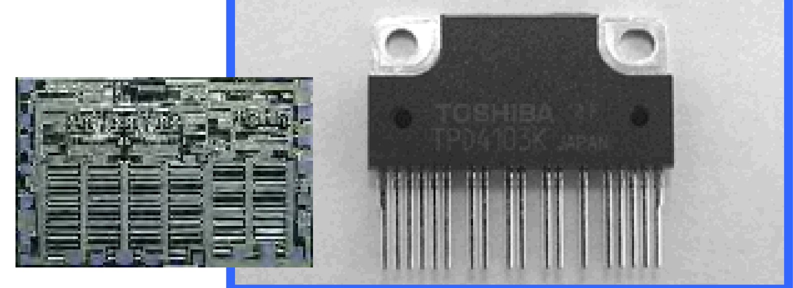
IPM

DIP-IPM

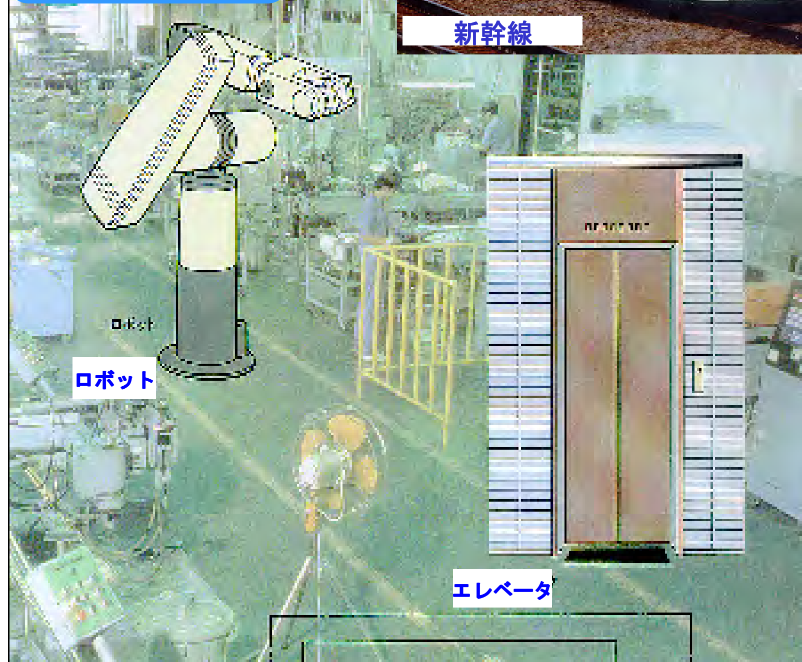


Press Pack IGBT

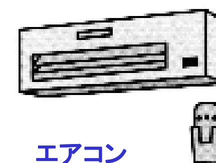
One Chip Inverter ICs

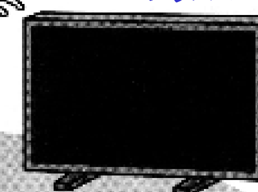


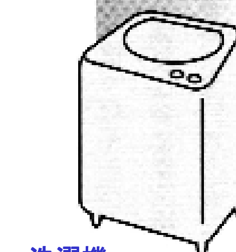
IGBTの応用



家電機器







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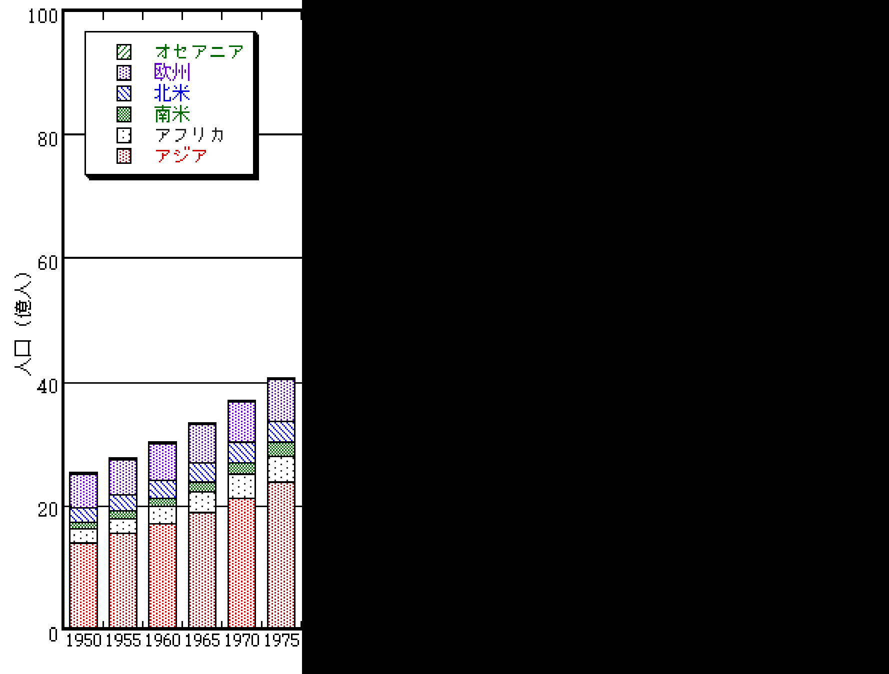
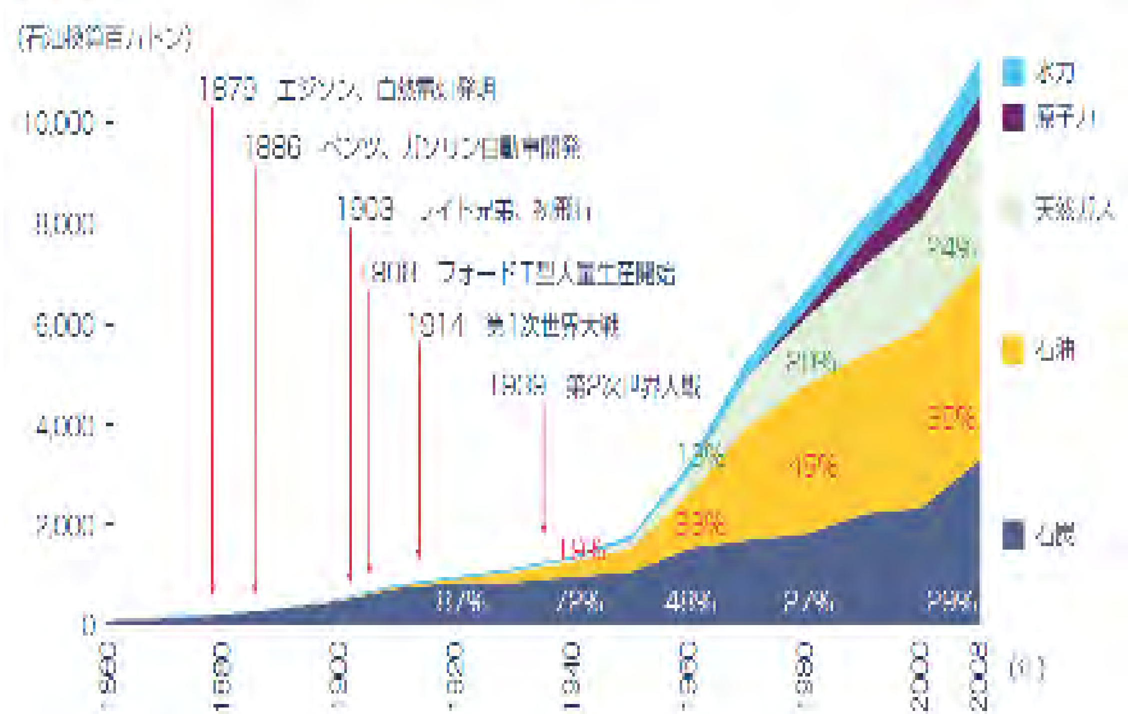
世界人口の推移とエネルギー消費

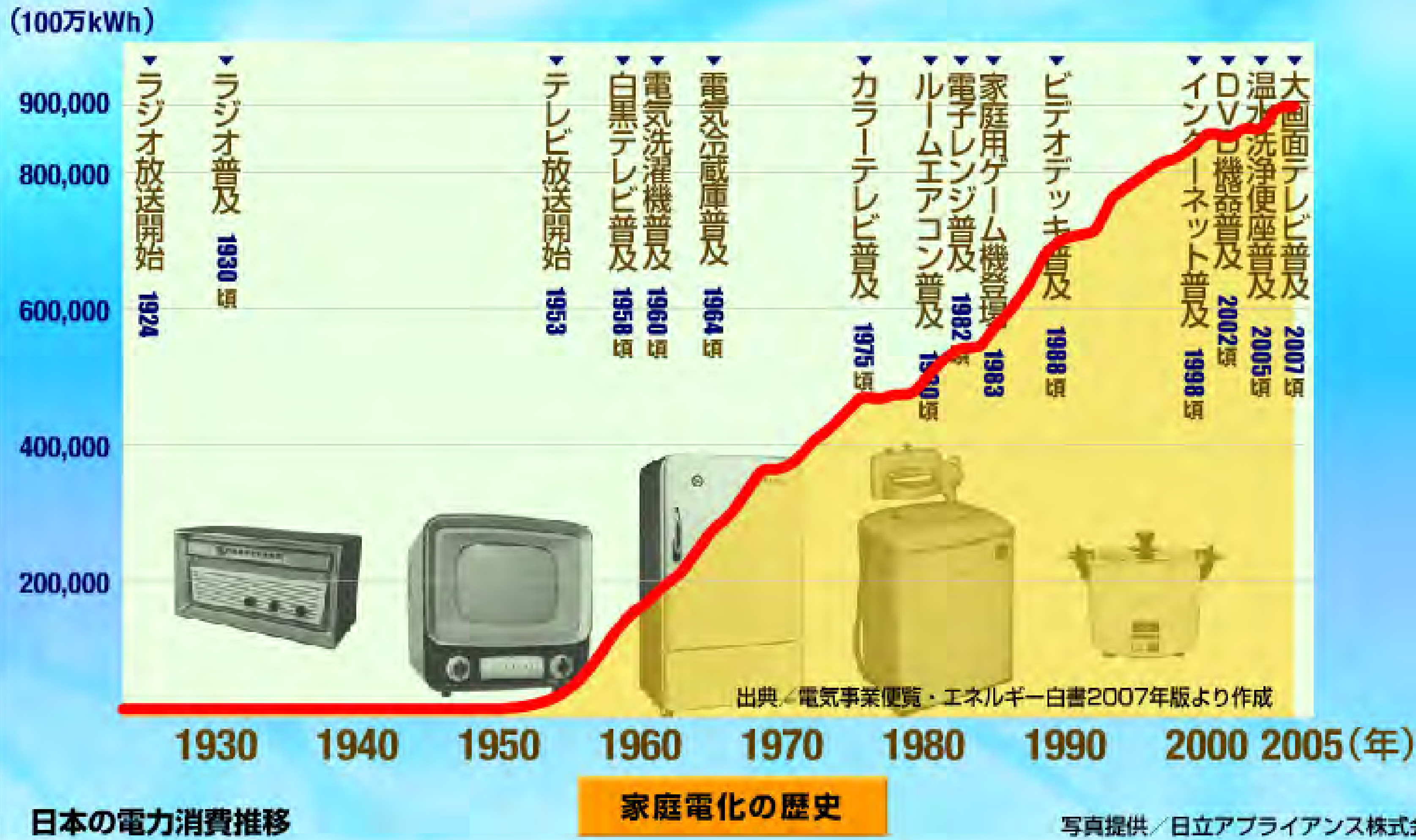


世界人口の推移と見通し

使用データ：総務省＞統計局ホームページ＞世界の統計　第2章 人口



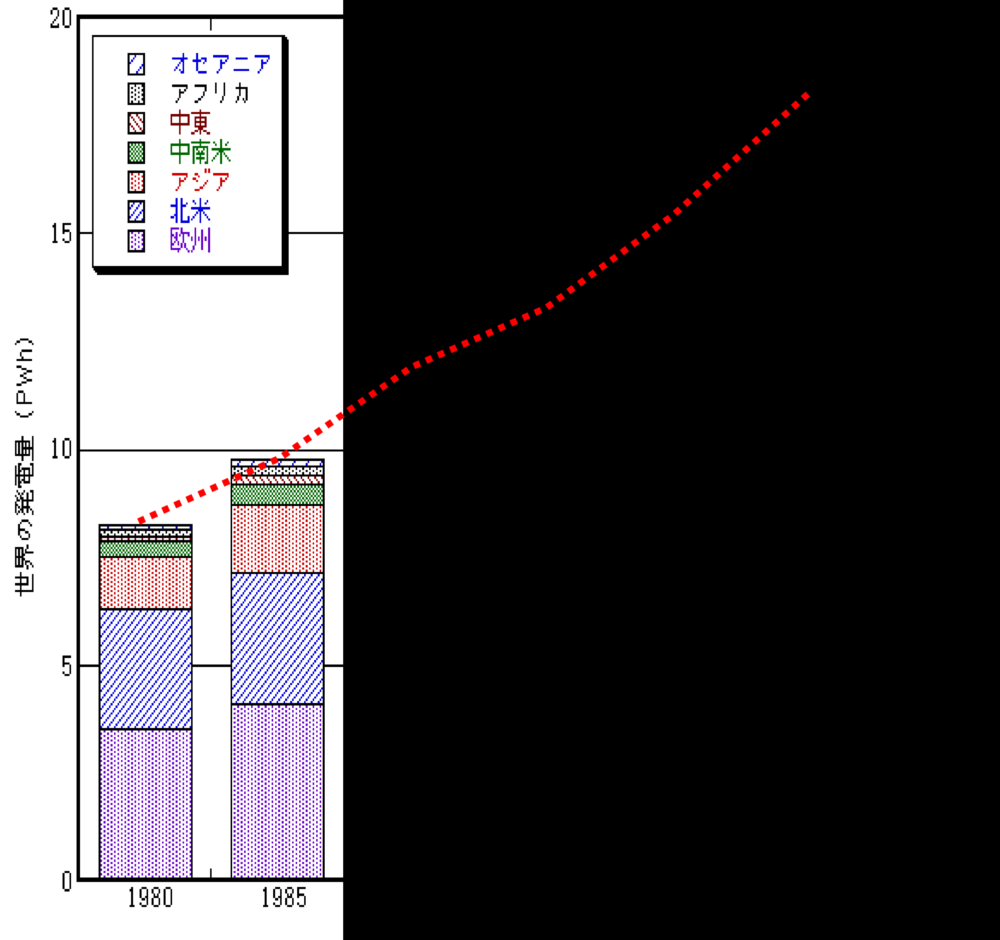
エネルギー白書2010



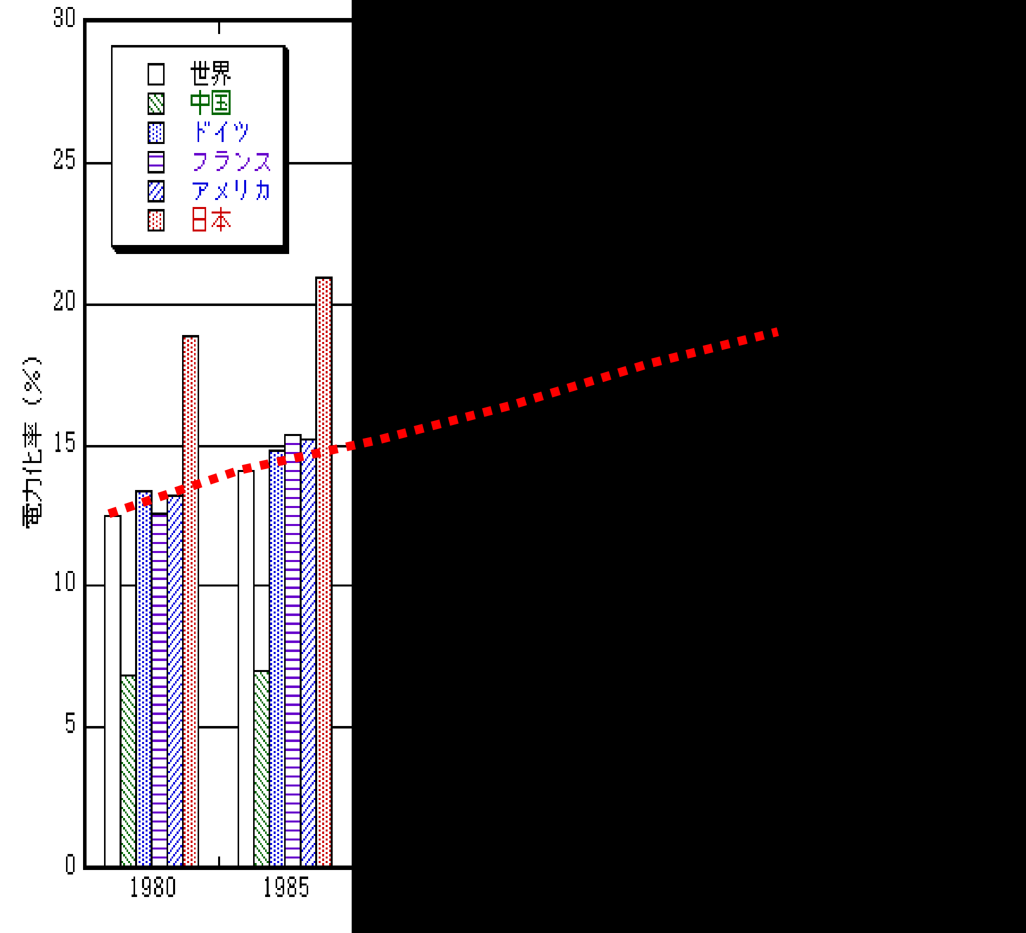
出所：科学技術振興機構 理科ネットワーク

世界の発電電力量

エネルギー消費に占める電力の比率 電力化率



使用データ：EDMC／エネルギー・経済統計要覧（2009年版）

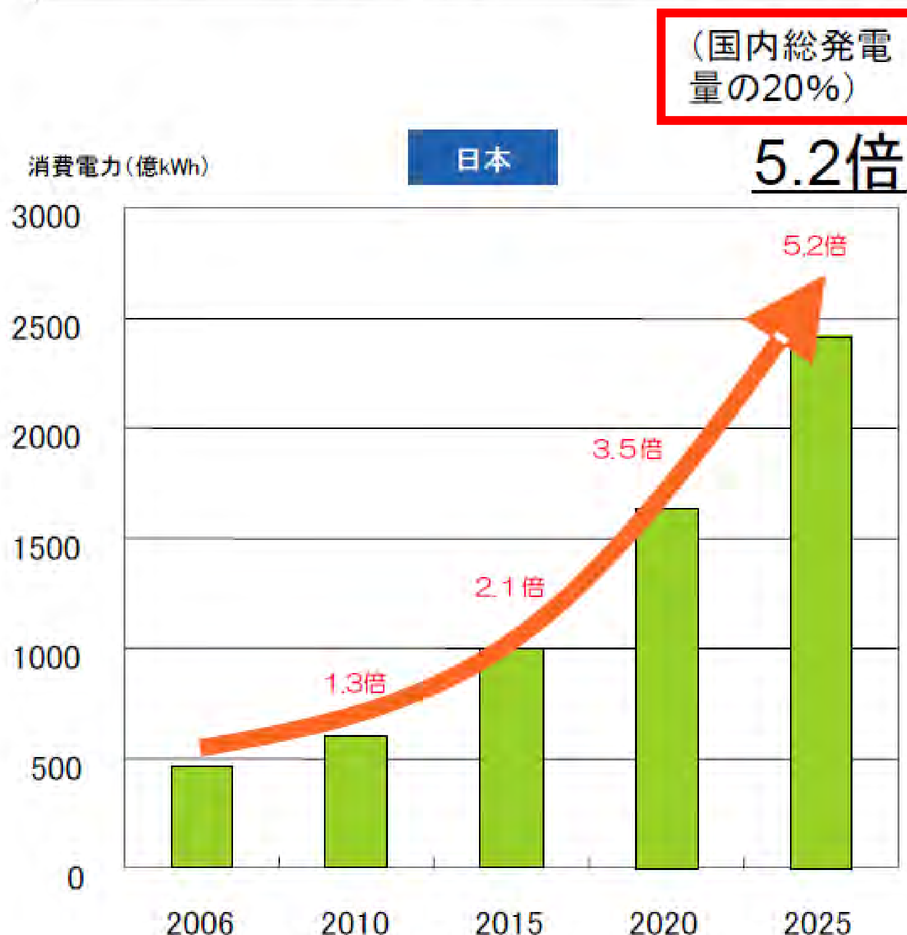


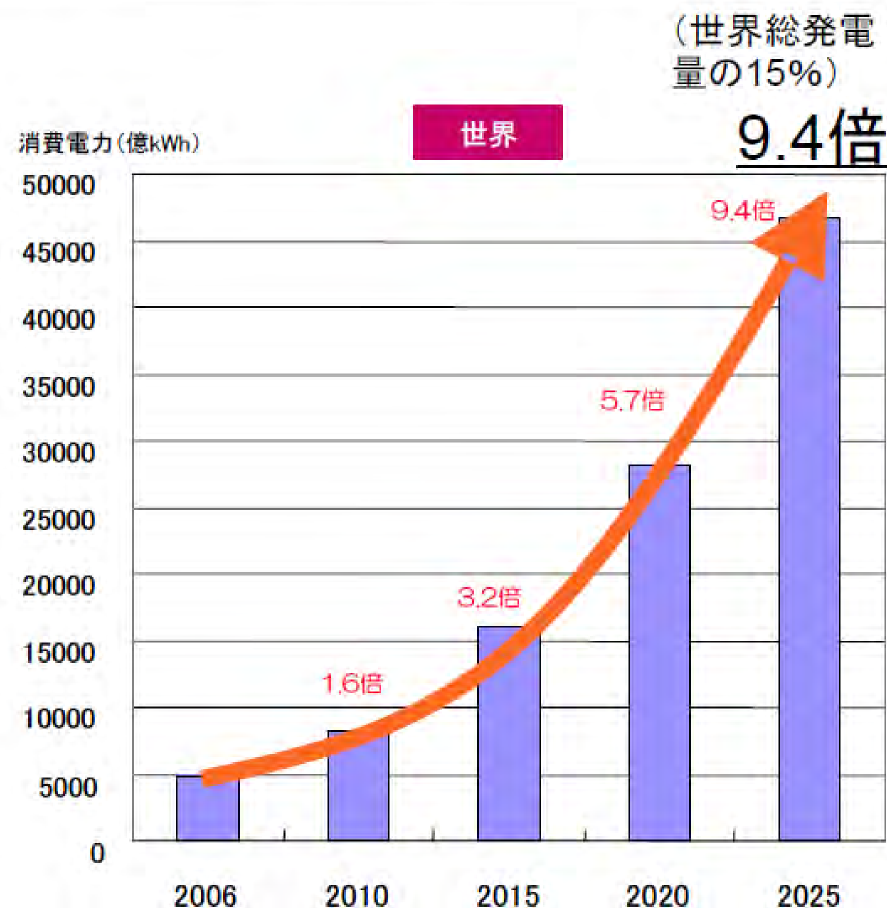
世界と各国の最終エネルギー消費に占める電力の比率（電力化率）
使用データ：EDMC／エネルギー・経済統計要覧（2009年版）

http://www.iae.or.jp/energyinfo/kaisetu.html

ＩＴ化でエネルギー消費増大

○ 情報化社会に伴うIT機器・システムの消費電力量の急増は、世界全体の課題。先進国に加えてBRICs等の発展により、世界のIT機器の普及は急増、**2025年には現在の9倍**（世界の総発電量の15%超、全エネルギー消費量の約6%）に達する恐れがある。

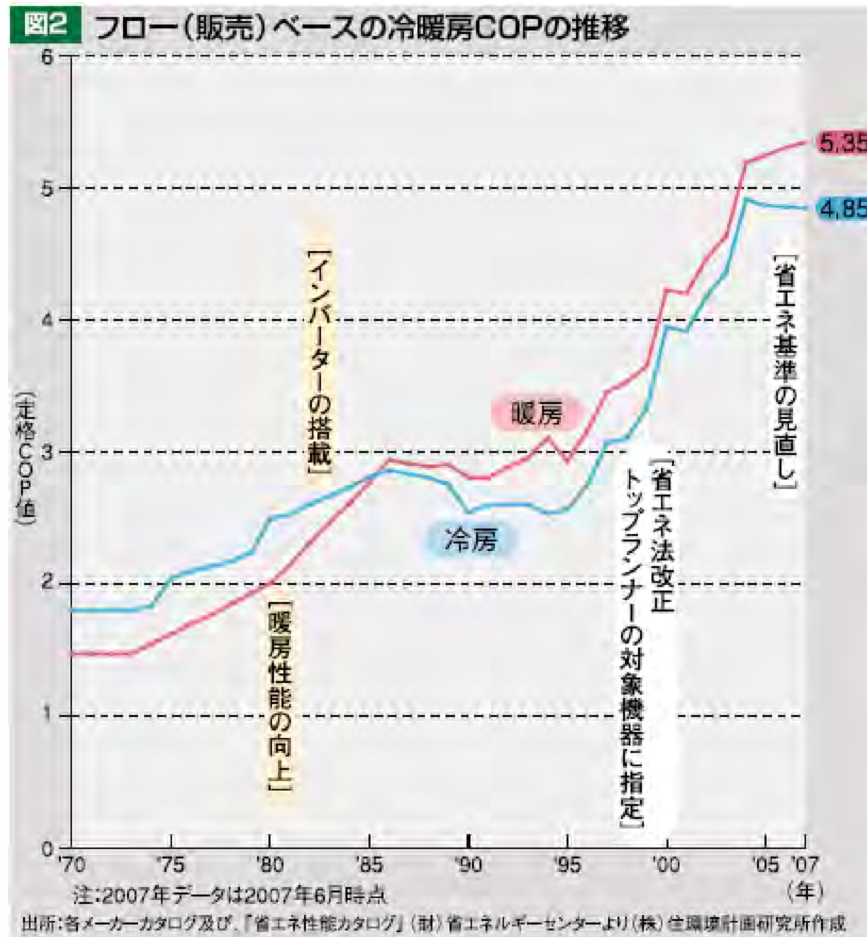


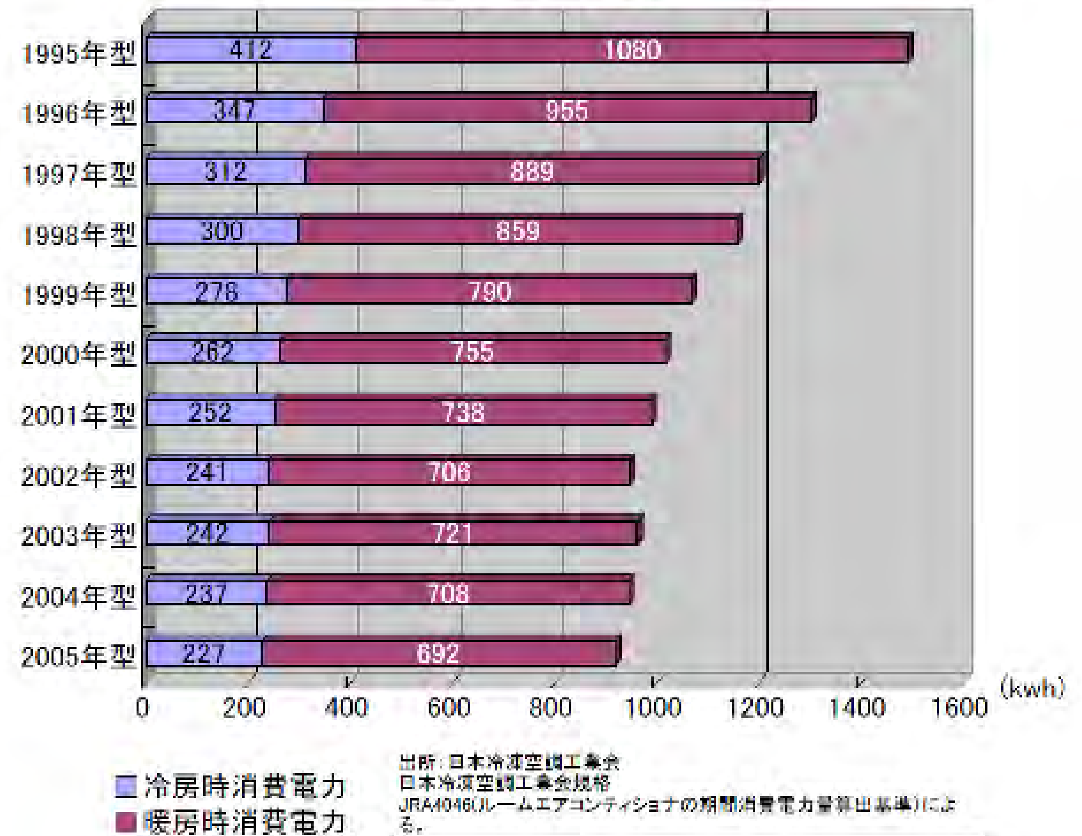


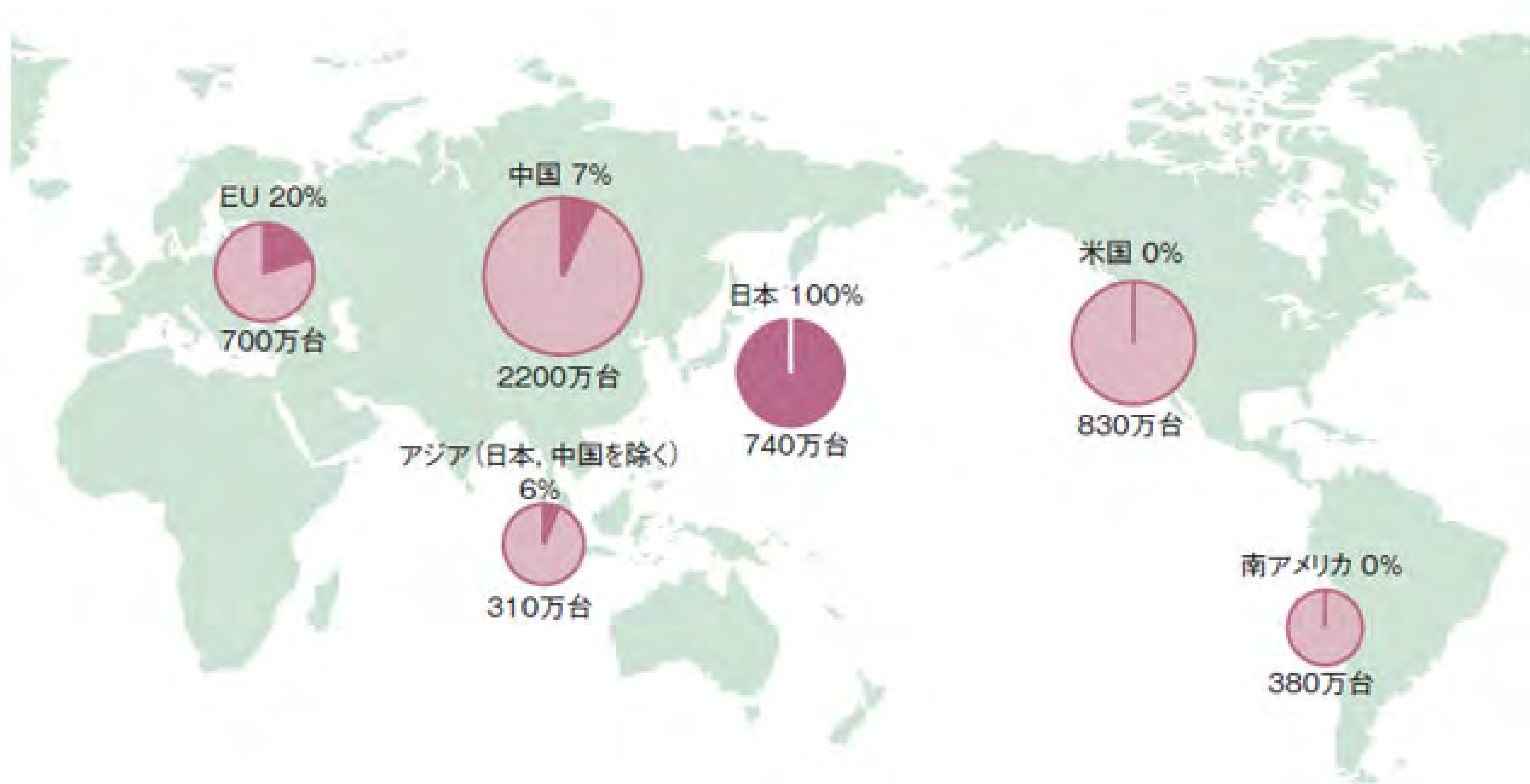
（出所）経済産業省/グリーンIT推進協議会試算(2008)

インバータは省エネルギーの主役

インバータエアコンの効率推移

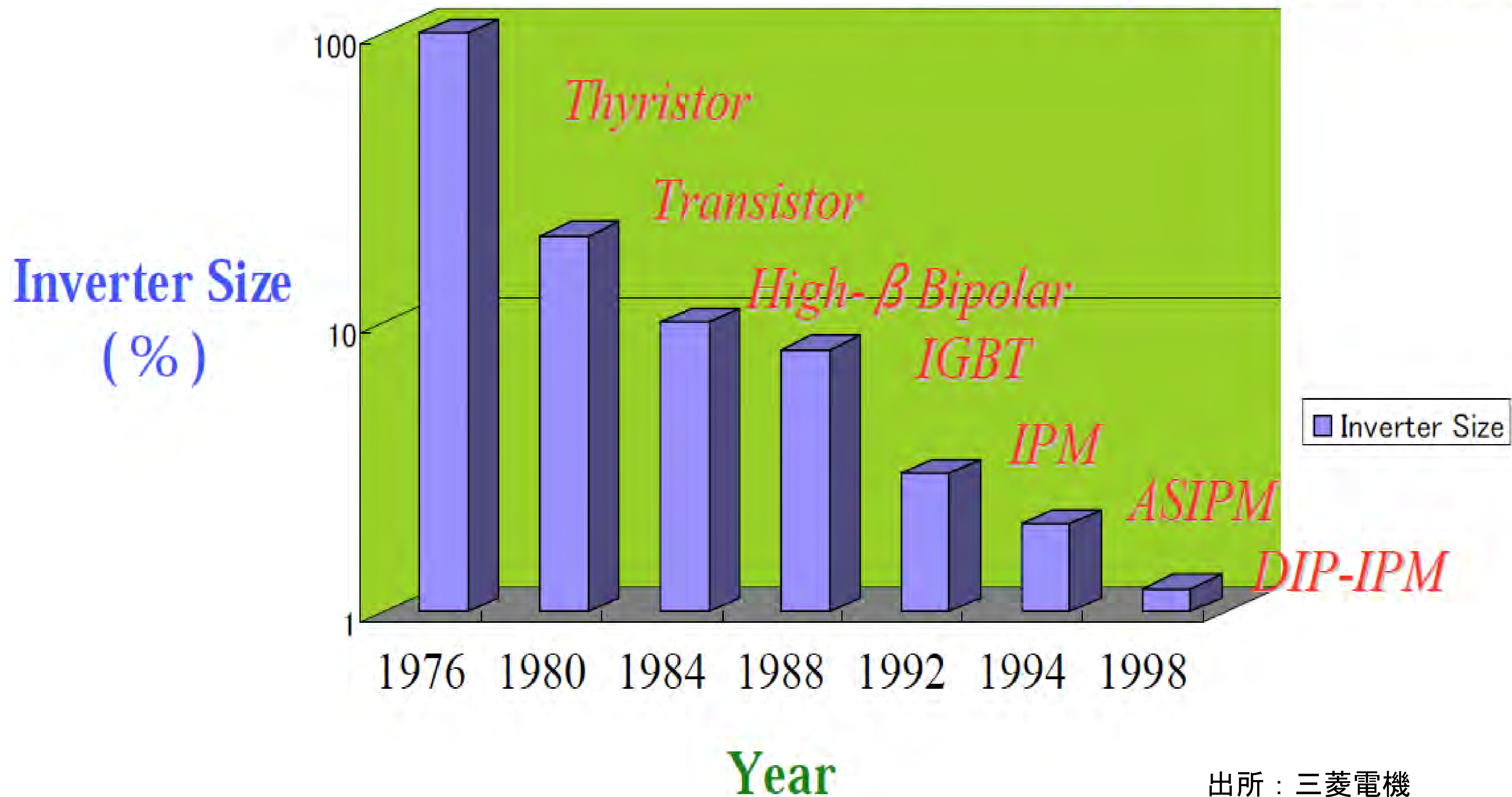






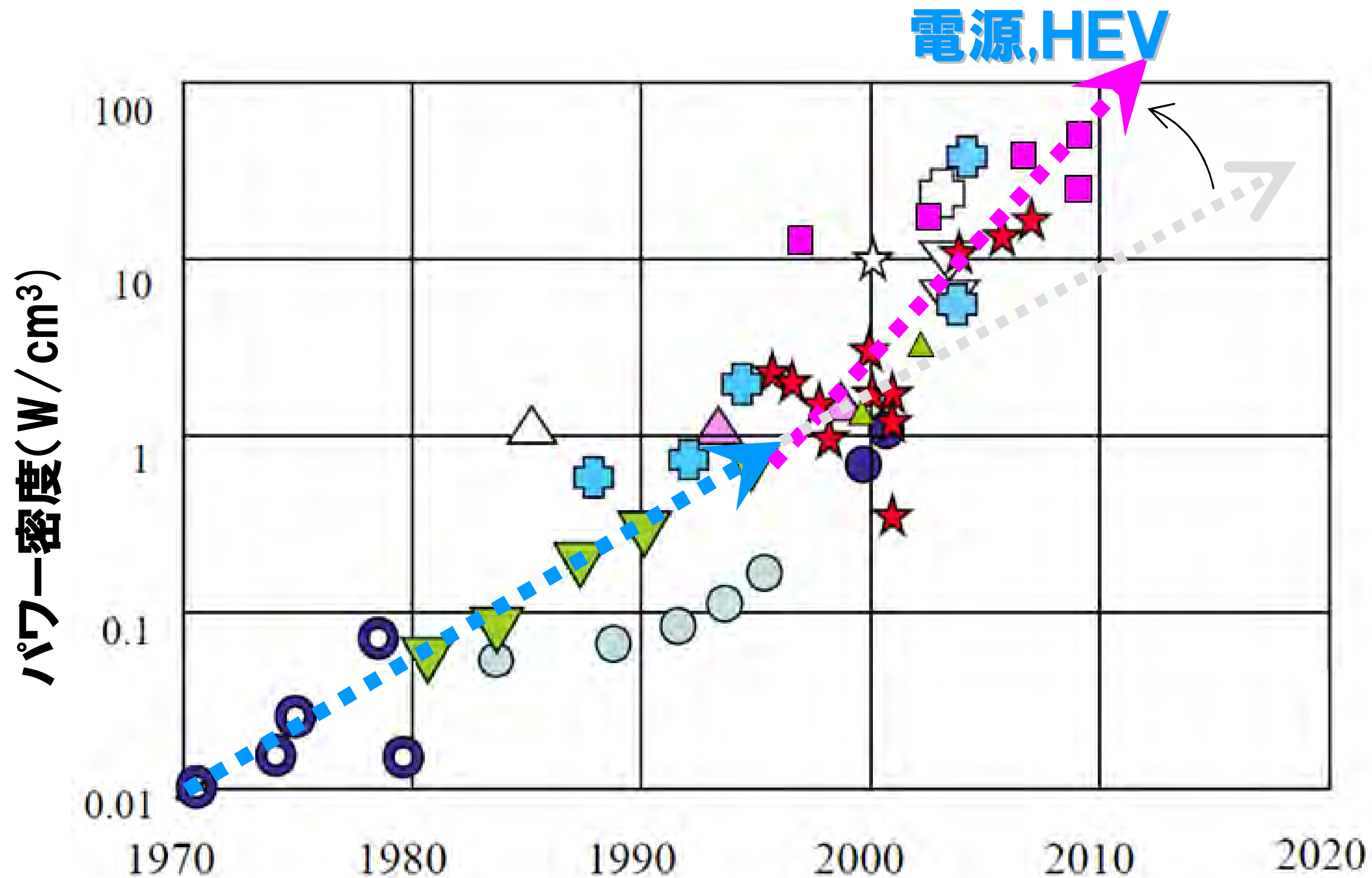
世界のエアコン消費台数とインバータ比率

出所：南川 明＝アイサプライ・ジャパン



出所：三菱電機

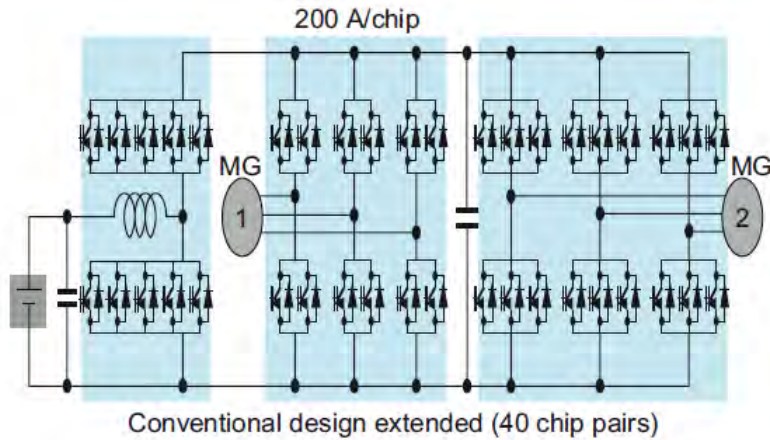
小型化・パワー密度向上が加速

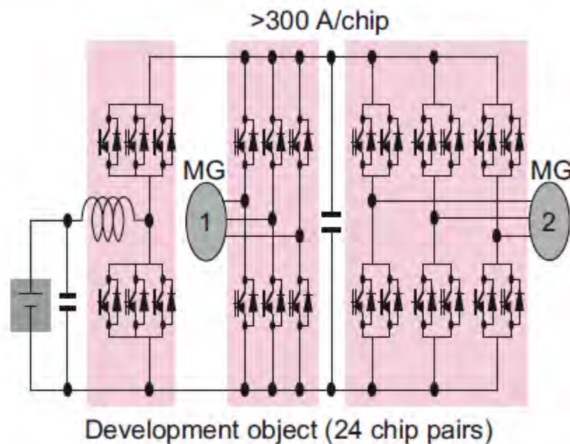


大橋 IEEJ Vol122 No.3 2002のデータを編集

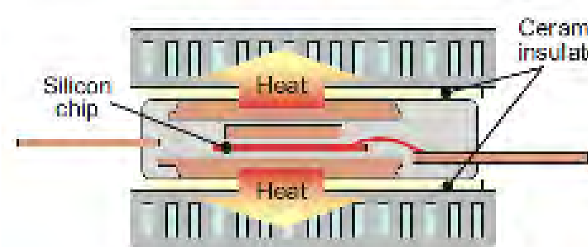
HEVパワーコントロールユニット大容量化

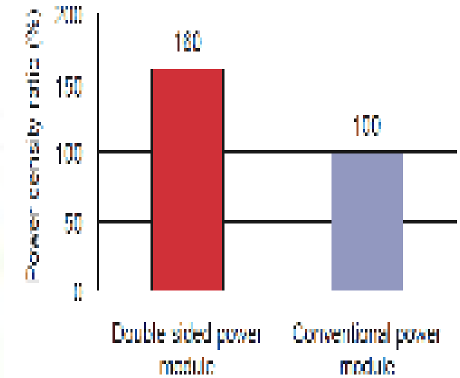
小型実装：両面冷却で高出力化

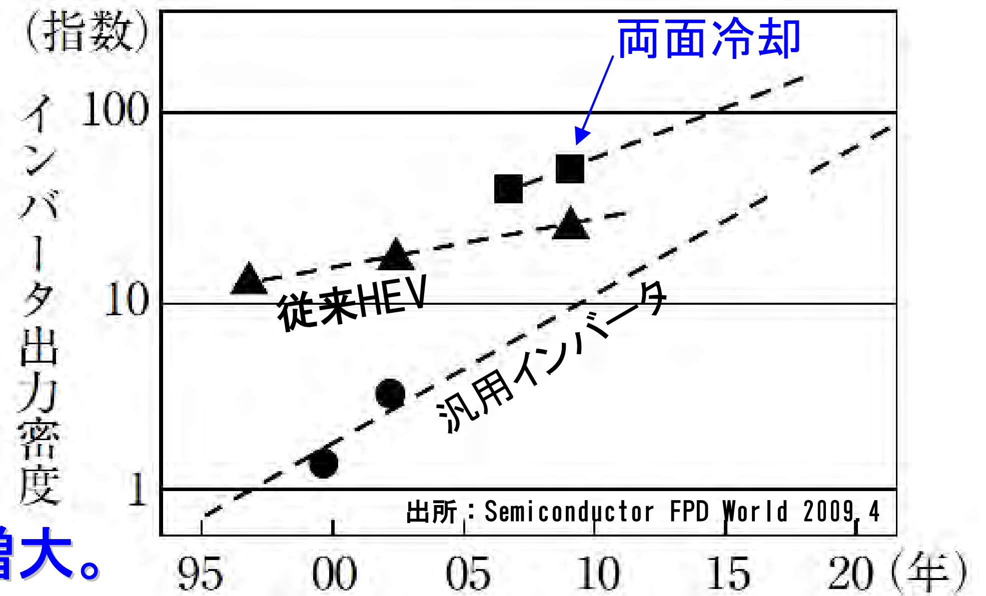




IGBT両面冷却



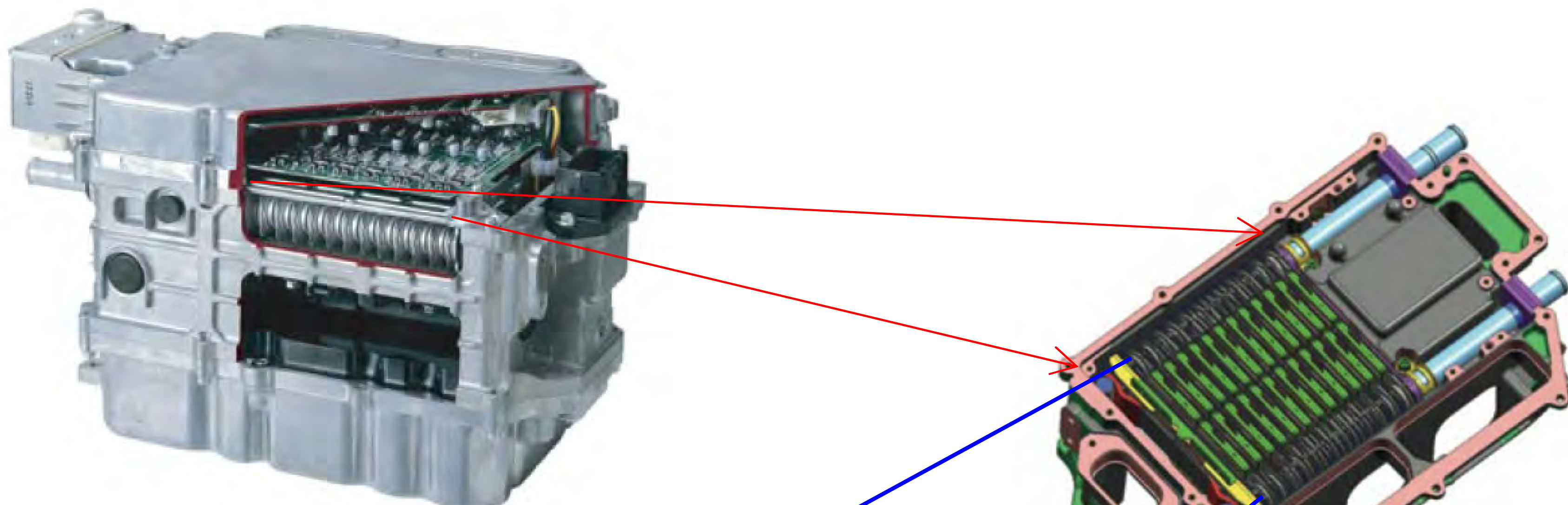




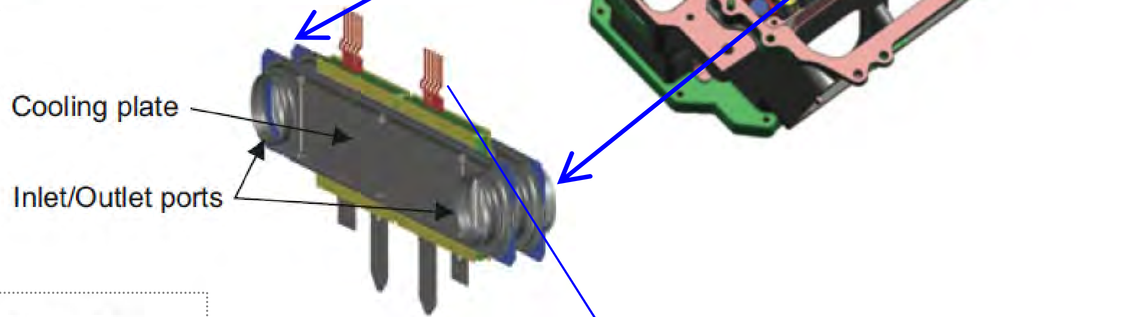
- 1Chip当たりの電流を200Aから300Aに増大。
- チップ数を増やさず大容量化。

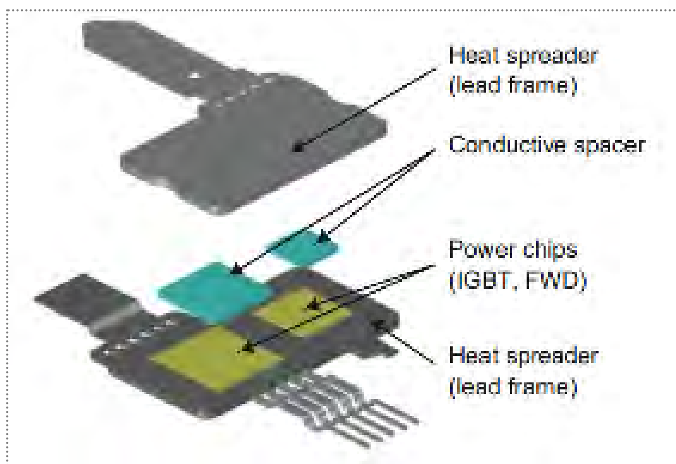
出典：デンソーテクニカルレビュー　Vol. 14　2009

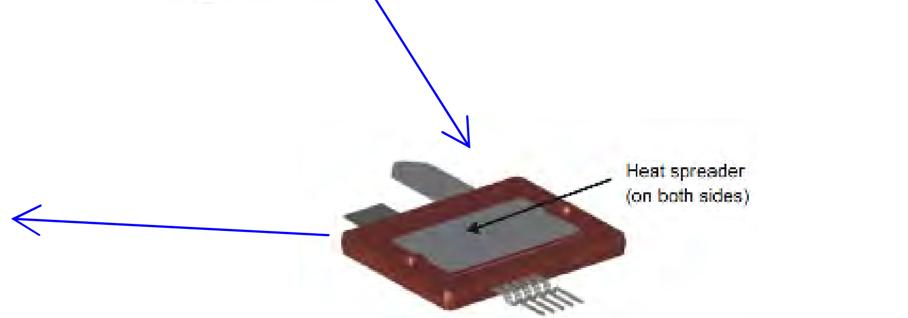
LS600h用PCU　パワー出力60％アップ



バッテリー同等サイズ

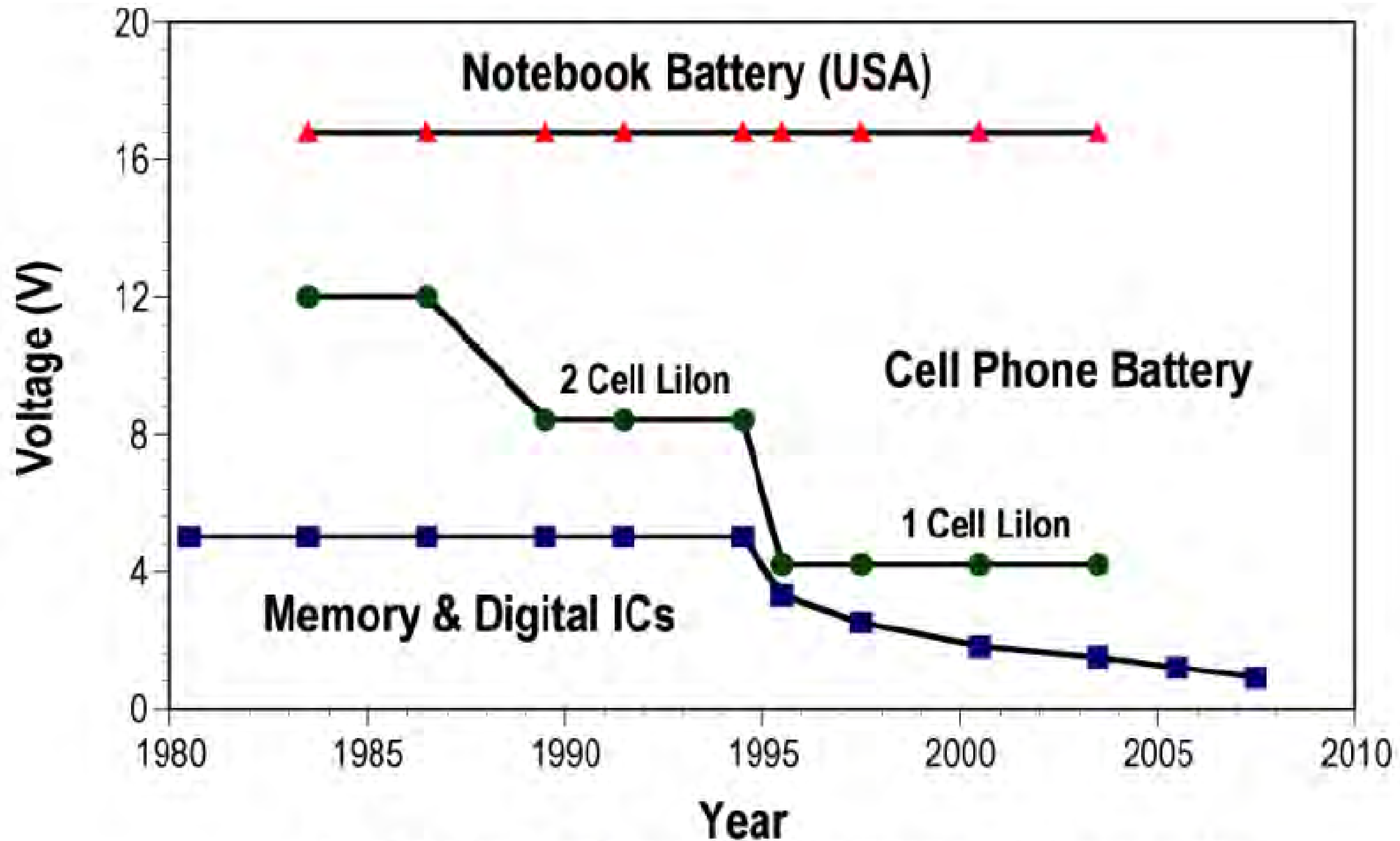






出典：デンソーテクニカルレビュー　Vol. 14　2009

微細LSIの課題

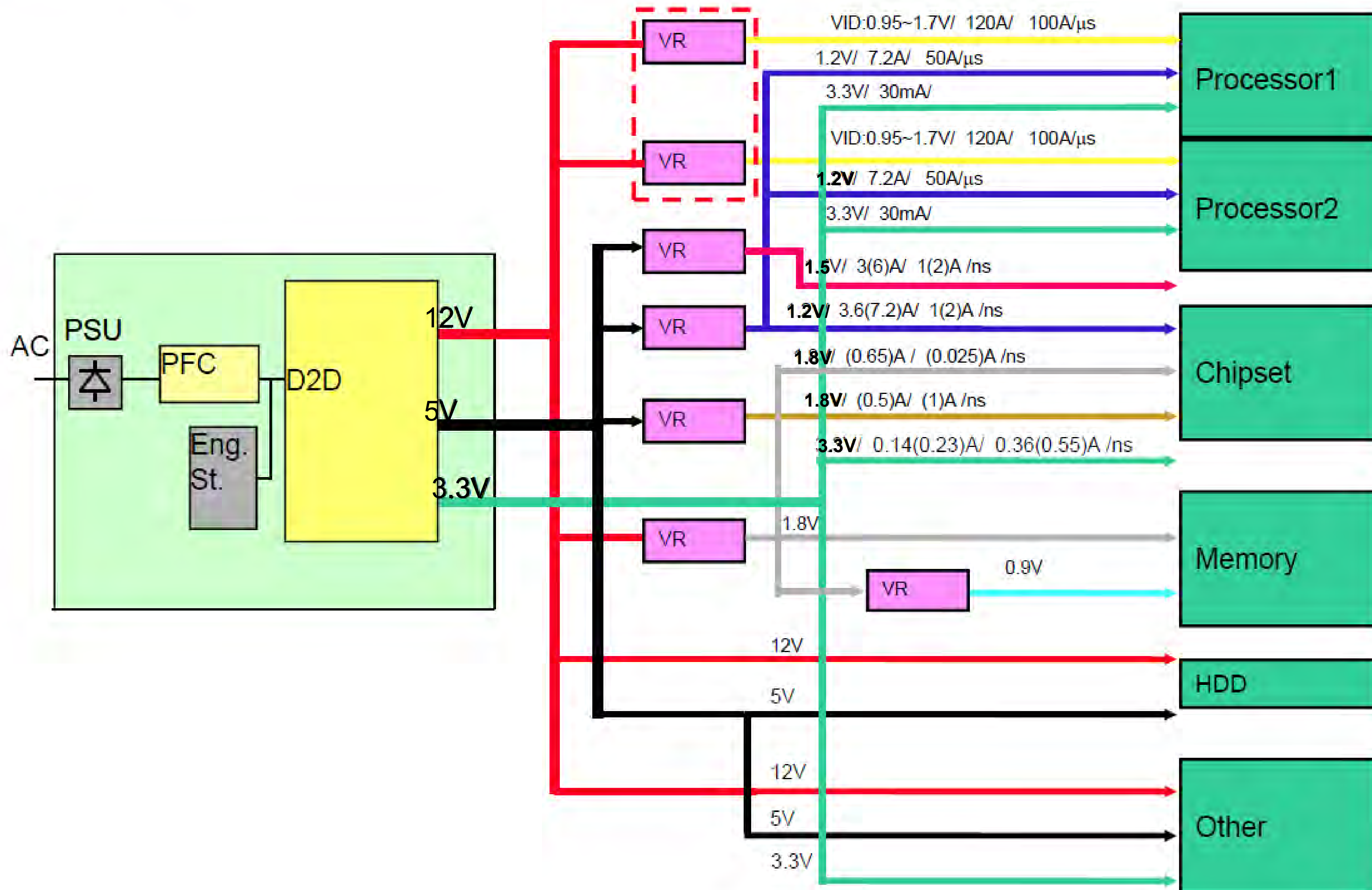


ISPSD' 2000, R. Williams, Advanced Analogic Technologies, Inc.

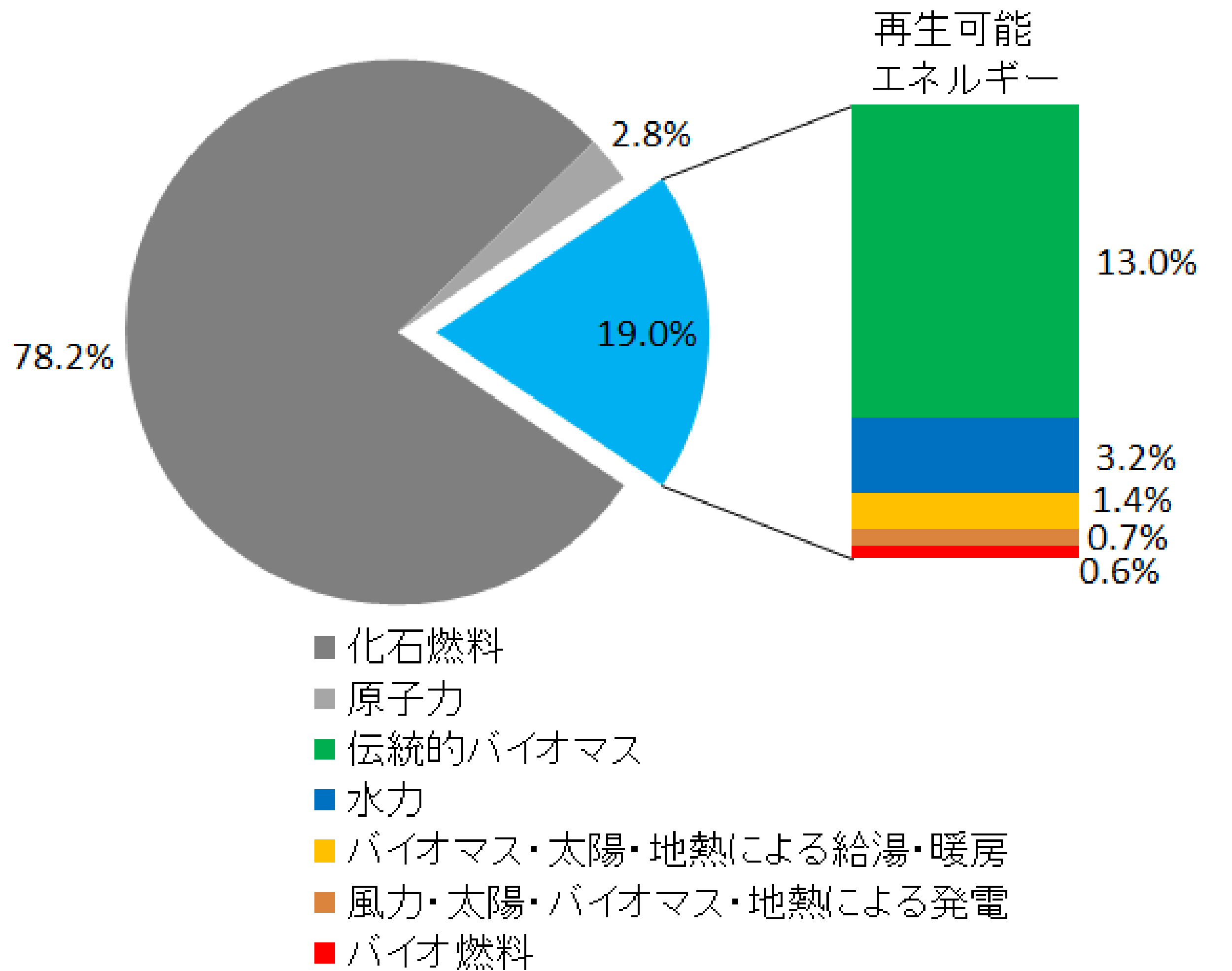
多種の電源電圧→電源の効率向上!!

Present Server Power Architecture

F. Lee PWRSoC' 08

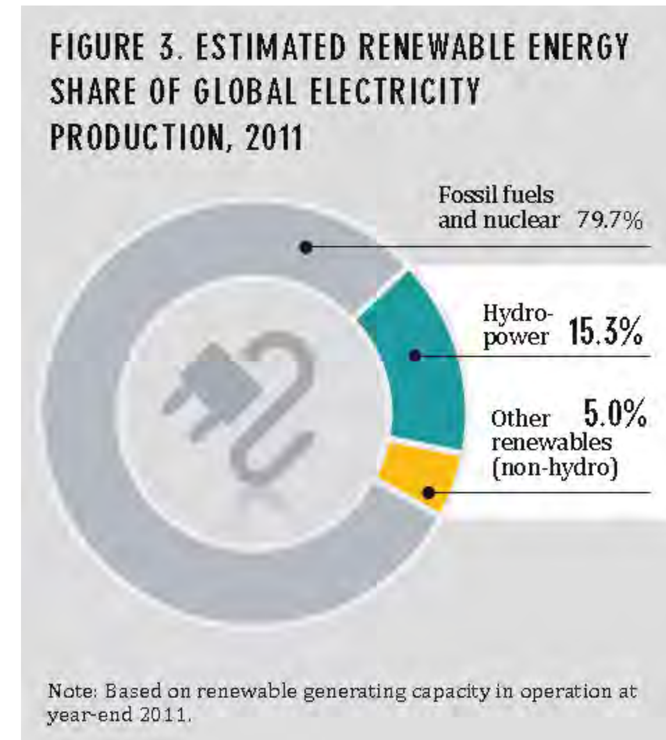


再生可能エネルギー



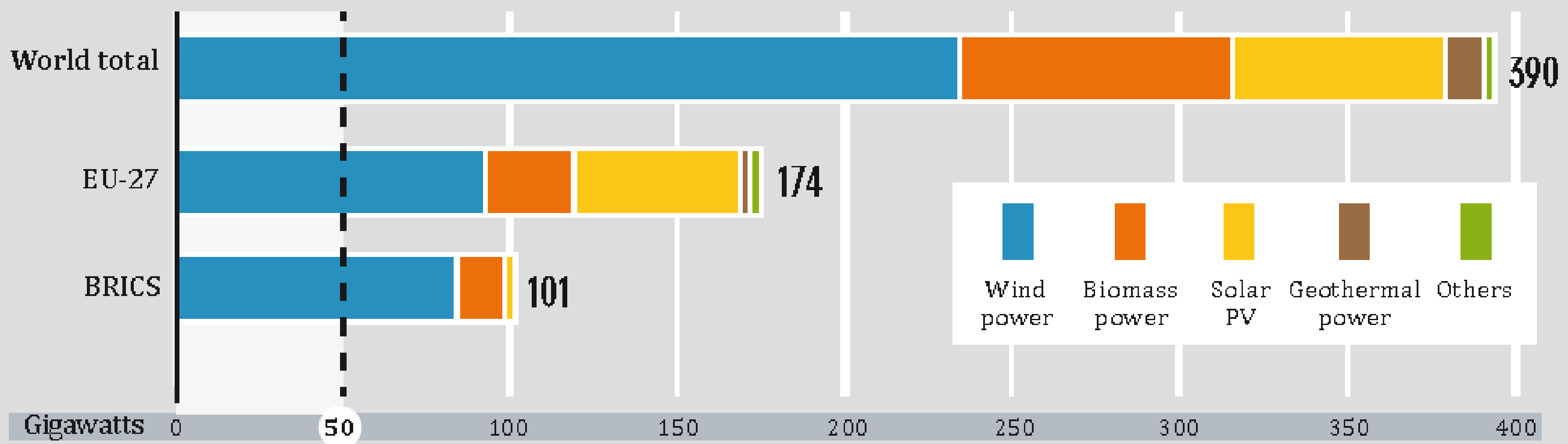
世界の最終エネルギー消費に占める再生可能エネルギーの割合(2008)

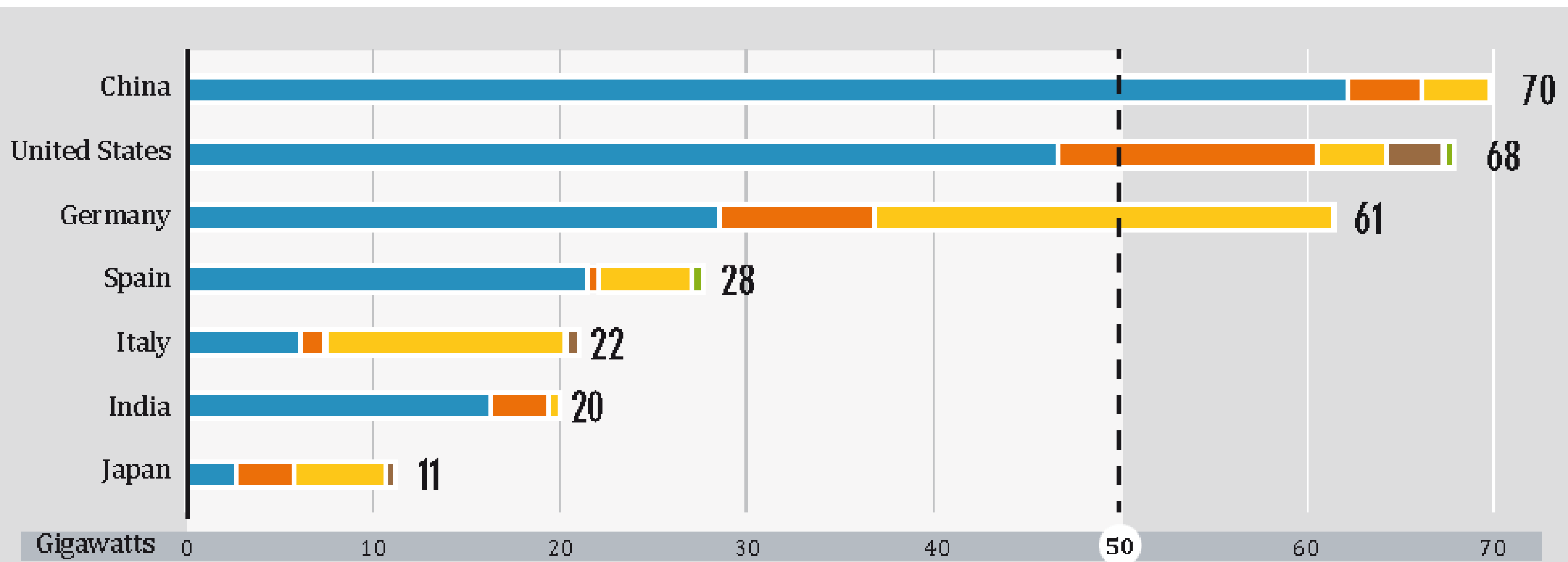
データ出典：REN21, Renewables 2010 Global Status Report



出所: REN21, RENEWABLES 2012 GLOBAL STATUS REPORT

FIGURE 4. RENEWABLE POWER CAPACITIES[1], EU 27, BRICS, AND TOP SEVEN COUNTRIES, 2011

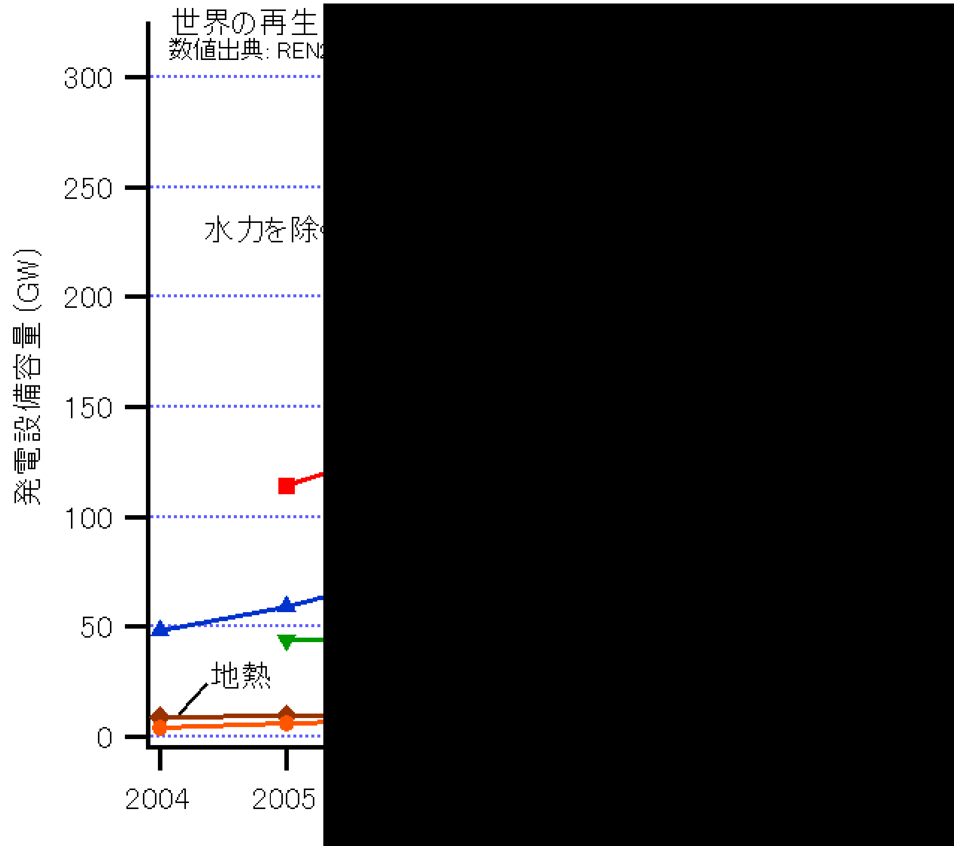


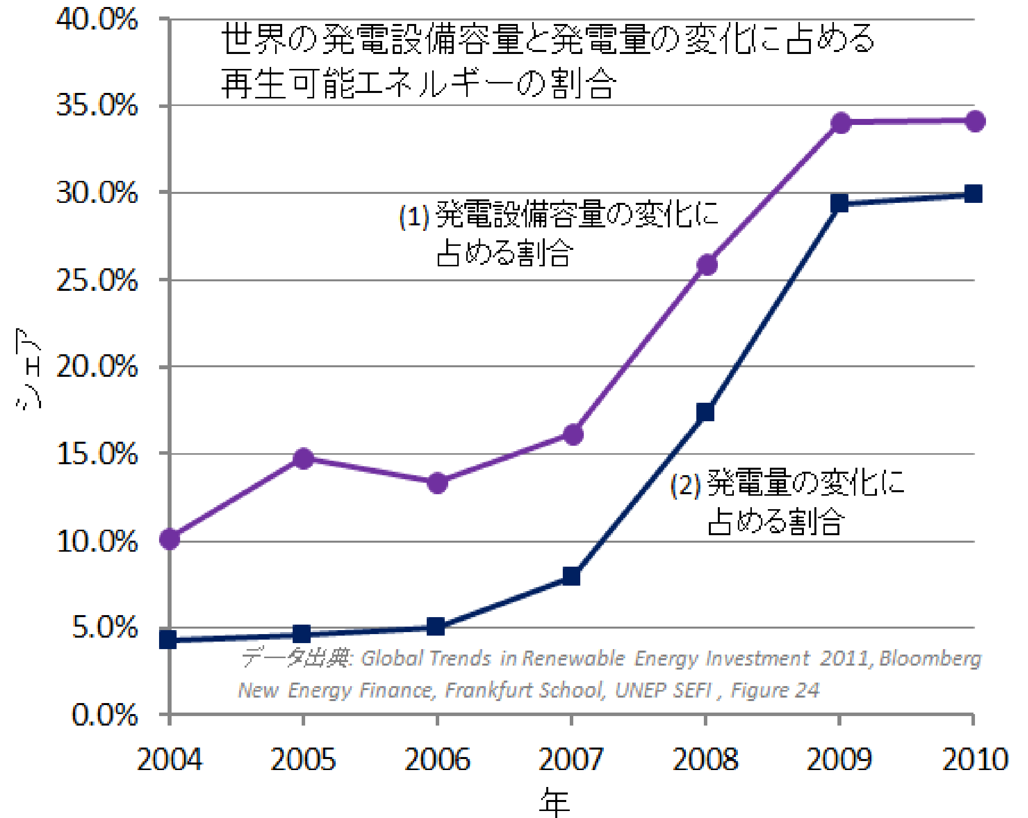


1 - excluding hydropower

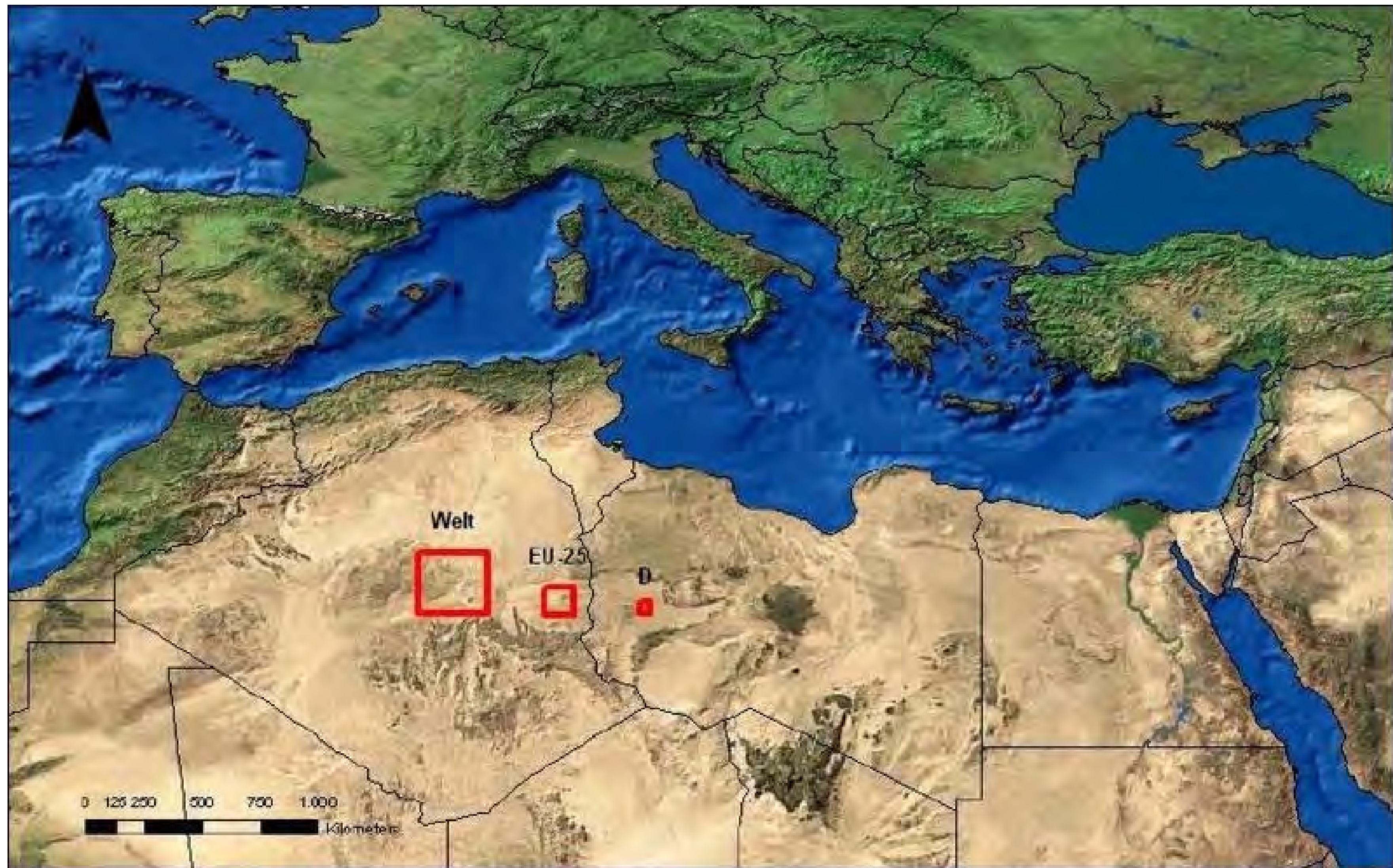
出所: REN21, RENEWABLES 2012 GLOBAL STATUS REPORT

増大する再生可能エネルギー



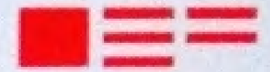


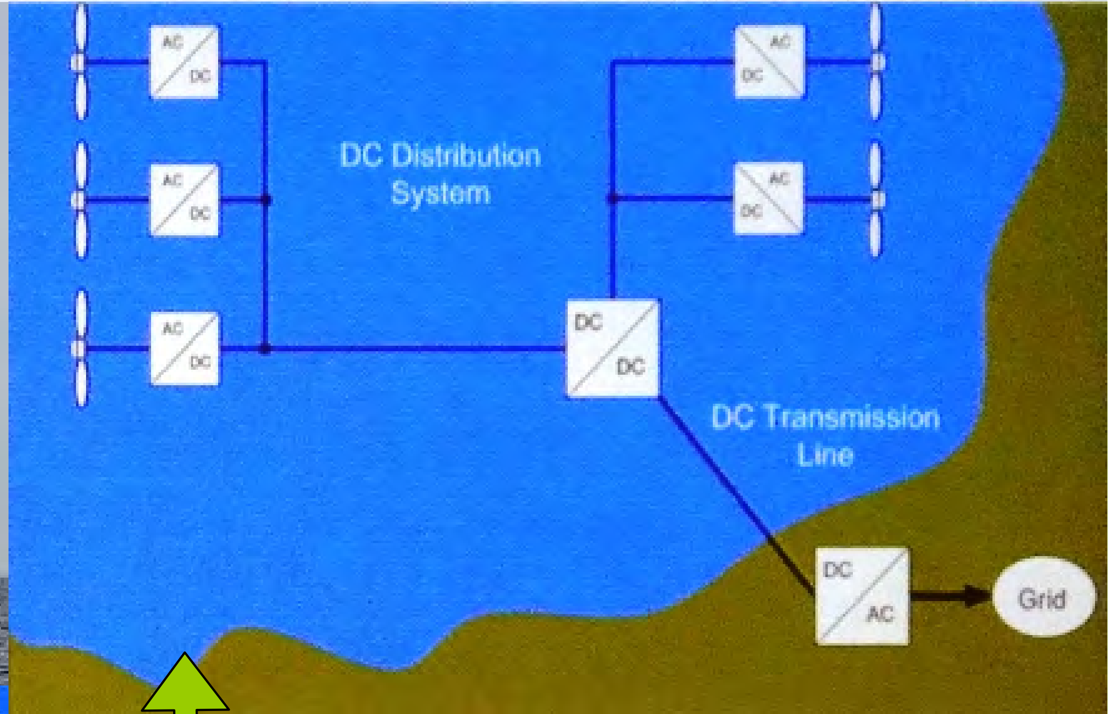
サハラ砂漠の6％の太陽光発電で全世界がまかなえる!!

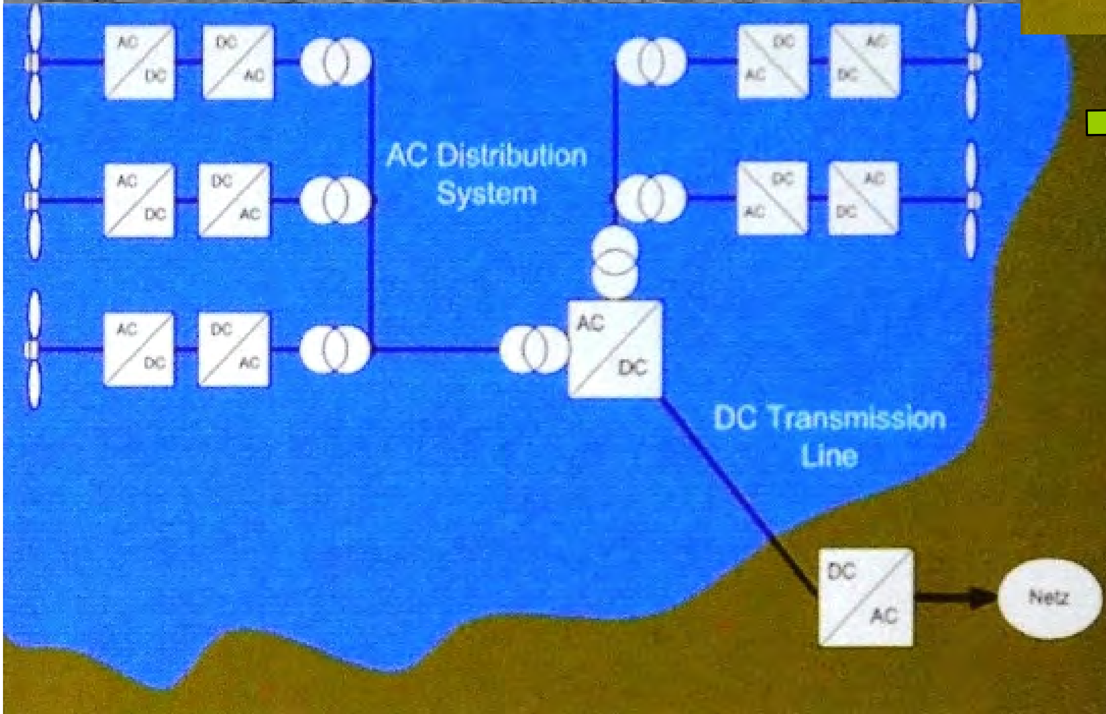


ドイツ、EU25カ国および全世界の需要と等しい電力を太陽エネルギーで発電するのに必要な面積

Grid Topologies for Offshore Wind Farms （Seatec）

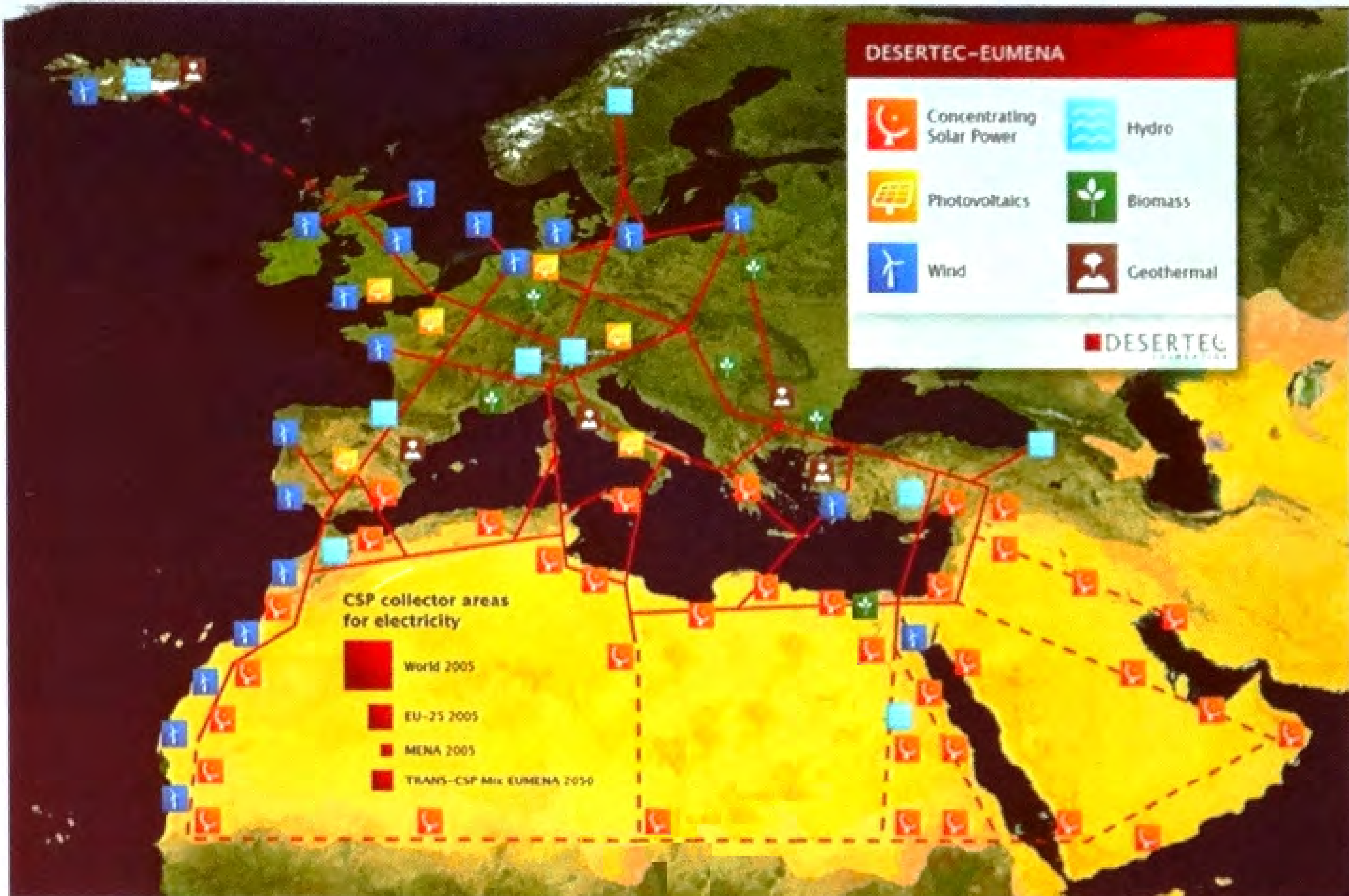






Desertec and Seatec Concept

E.ON Energy Research Center



Source: www.desertec.org

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パワーエレクトロニクスの誕生

1973年PESCでのWilliam E. Newell氏の基調講演

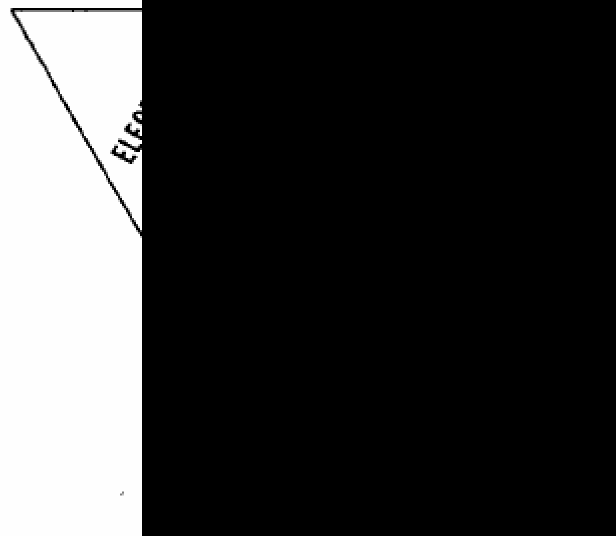
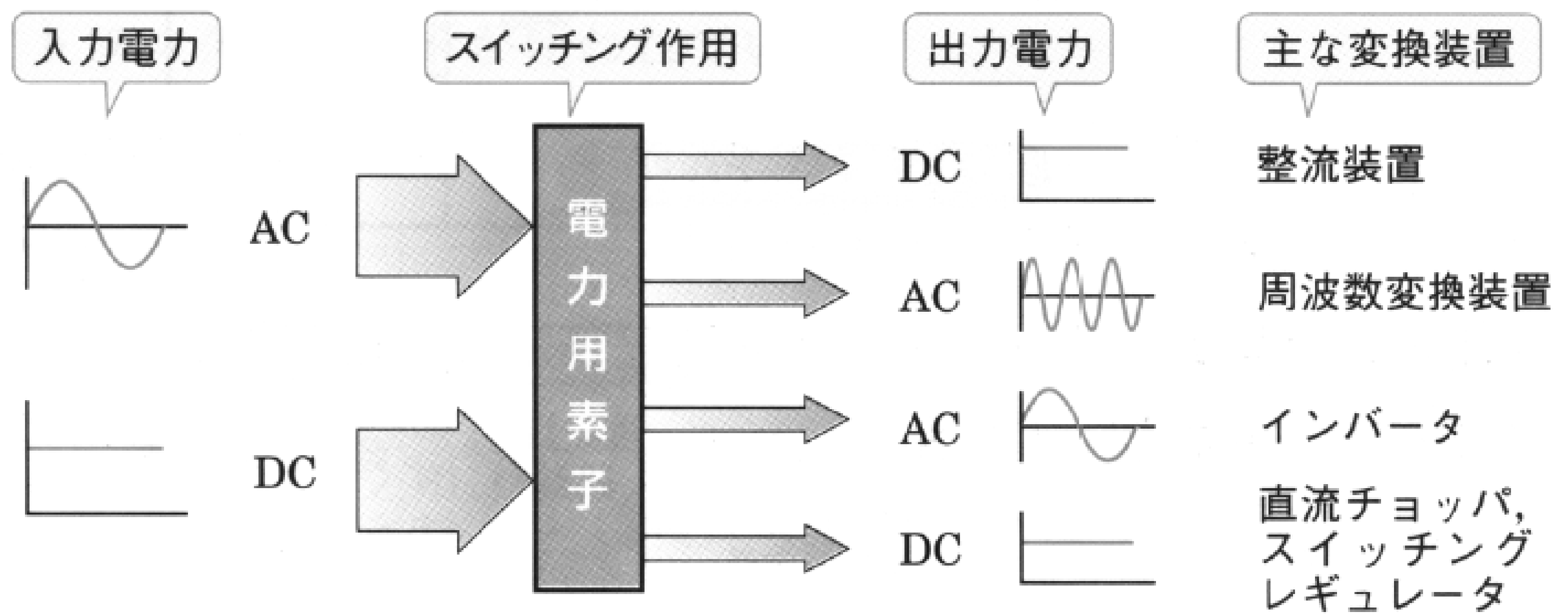


Fig. 1. Power electroni

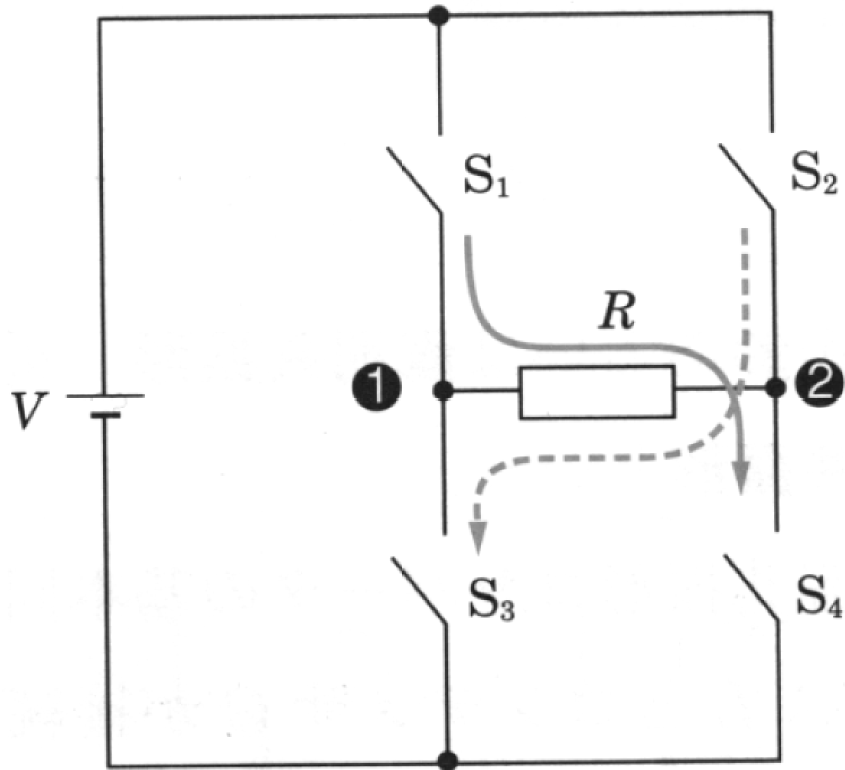
1. Systems and Contro
   1.00 General Syster
   1.10 Control Theor
   1.20 Sensing and G
   1.30 Motor Drives
      1.31 DC Drive
      1.32 AC Drive
      1.33 Brushles
   1.40 Heating and W
   1.50 HVDC and Ot
   1.60 Large Power S
   1.70 Low-Power an
   1.80 Miscellaneous
2. Solid-State Power D
   2.00 General Devic
      2.01 Material
      2.02 Power D
      2.03 Power T
      2.04 Turn-On
      2.05 Turn-Of
   2.10 Special Topics
      2.11 High-Vo
      2.12 High-Cu
      2.13 Surge an Analysis
      2.14 dv/dt Co Design
      2.15 Turn-On
      2.16 Turn-Of
      2.17 Series/P
      2.18 Second
3. Power Circuits and
   3.00 General Circui
   3.10 Power Compo
   3.20 Harmonics an
   3.30 Naturally Com
      3.31 AC/DC
      3.32 AC Swit
      3.33 Cycloco
      3.34 Varegul
      3.35 Pulse Ci
   3.40 Self-Commut Commutation
      3.41 DC Swit
      3.42 Inverter
      3.43 Frequen

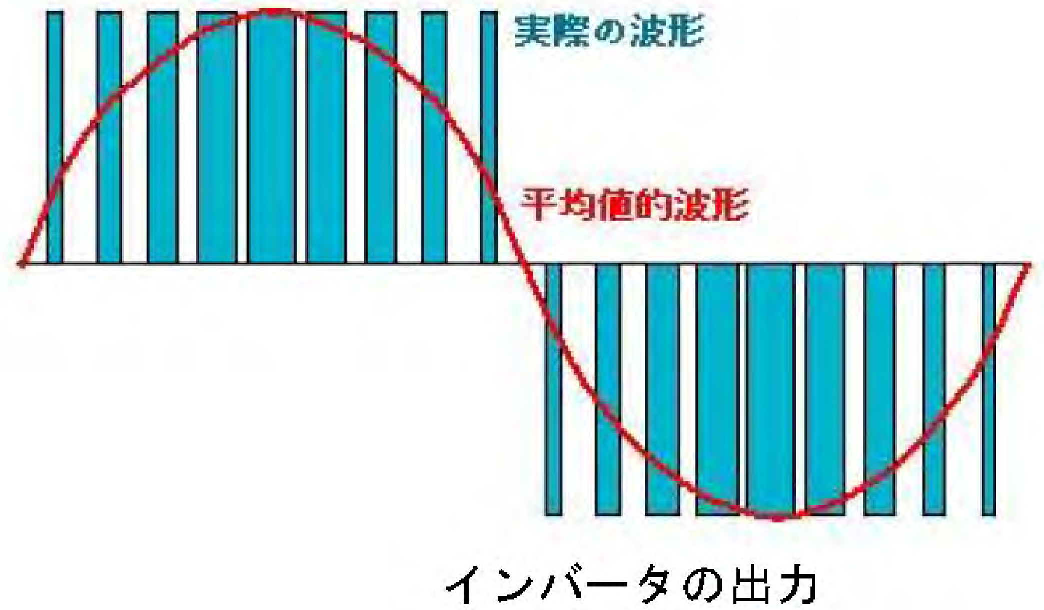
Fig. 2. Powe

電力変換



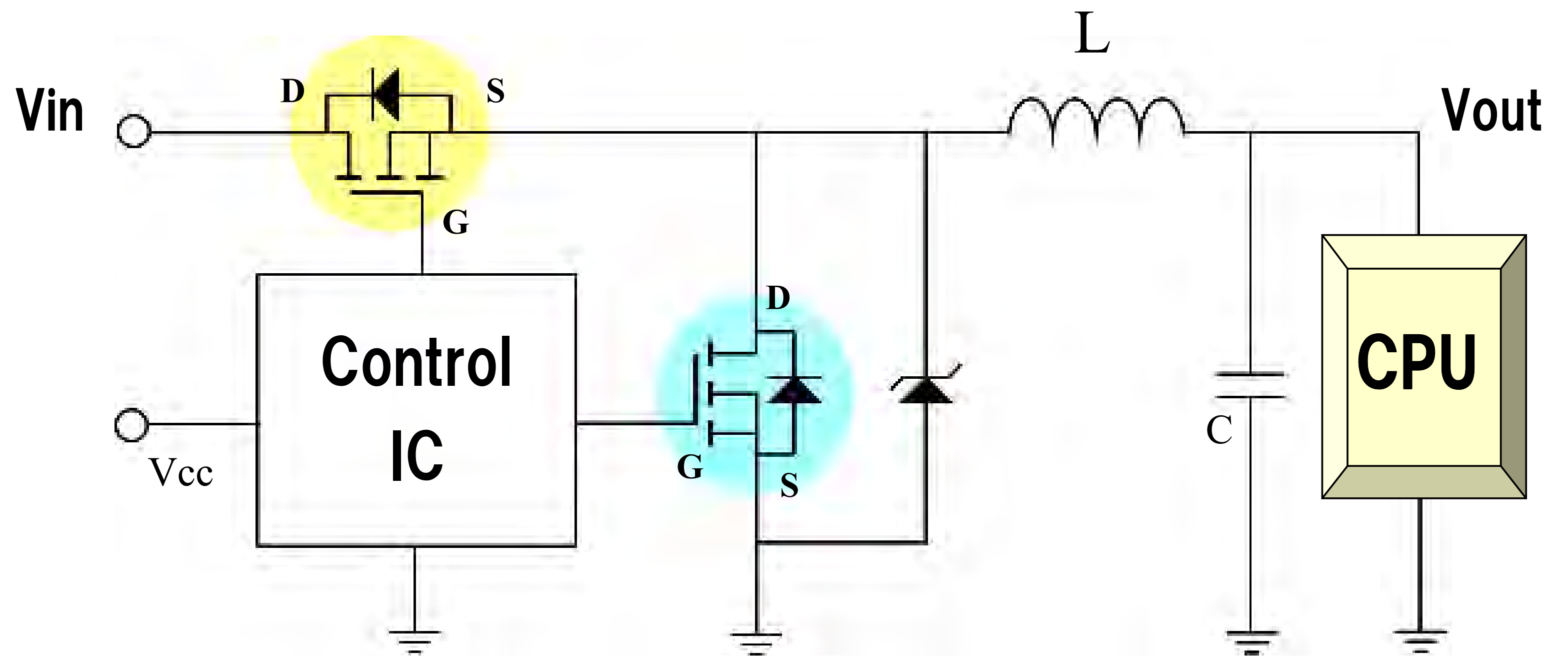
インバータの基本原理



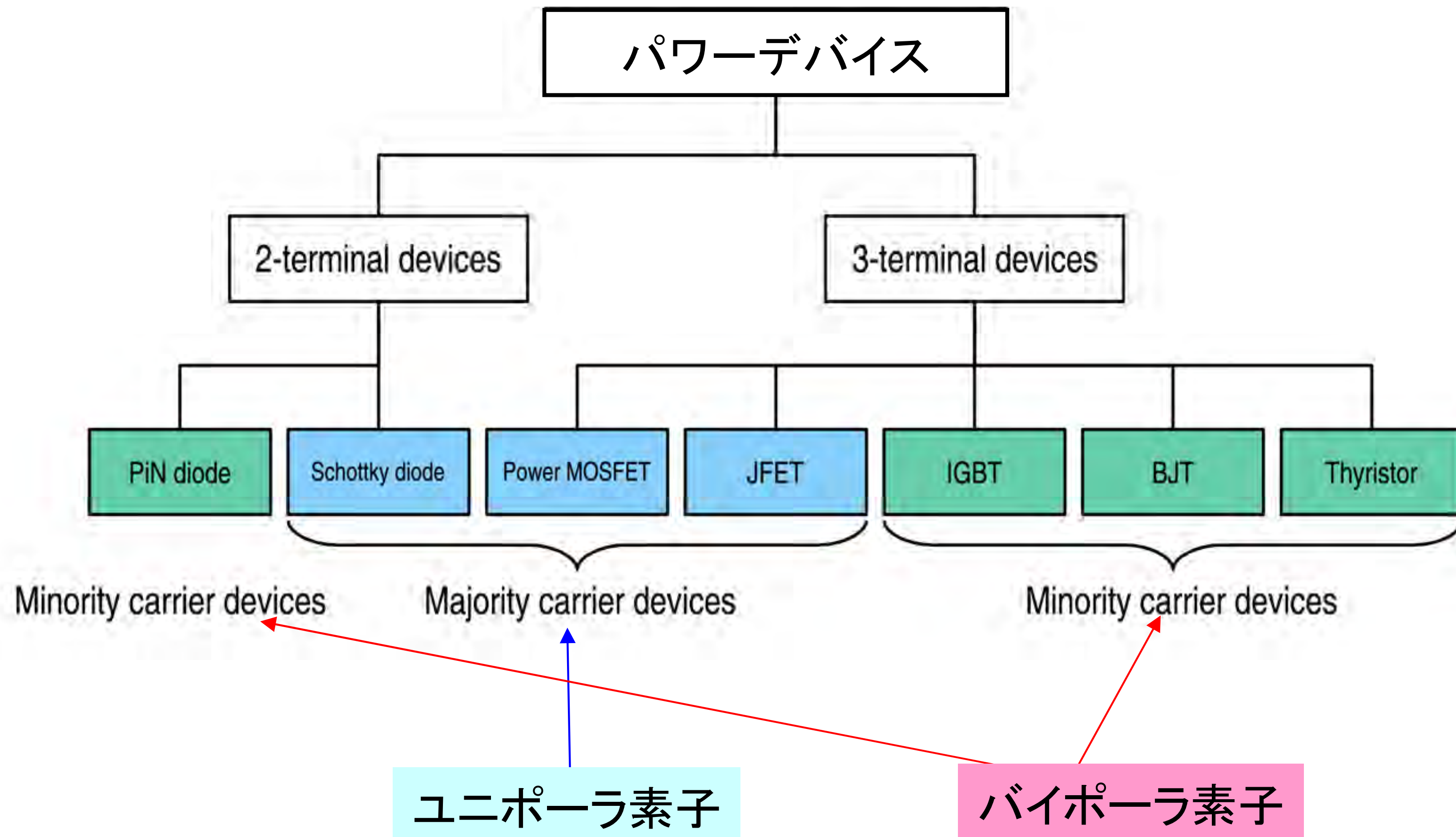


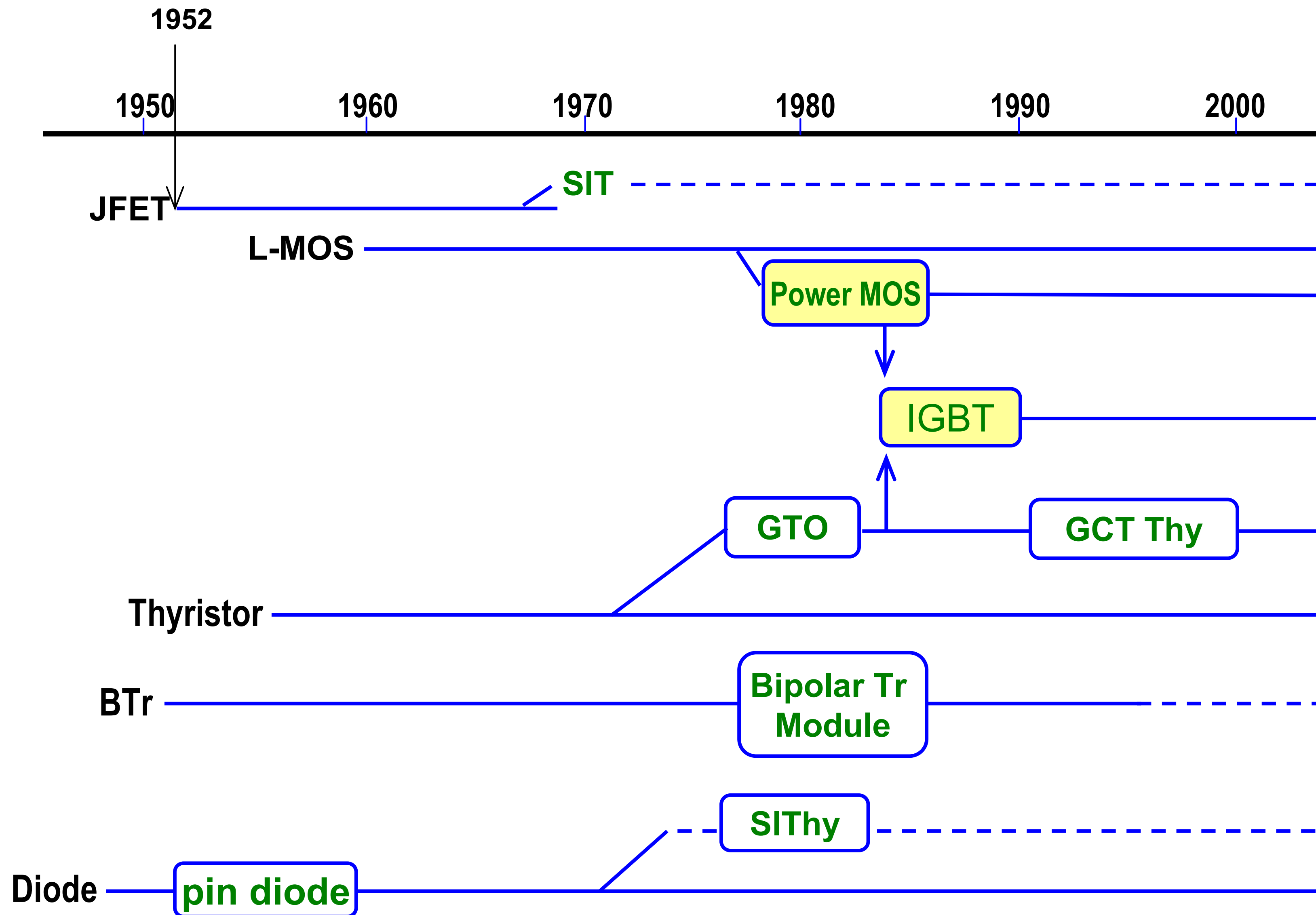
インバータの出力

DCDCコンバータ

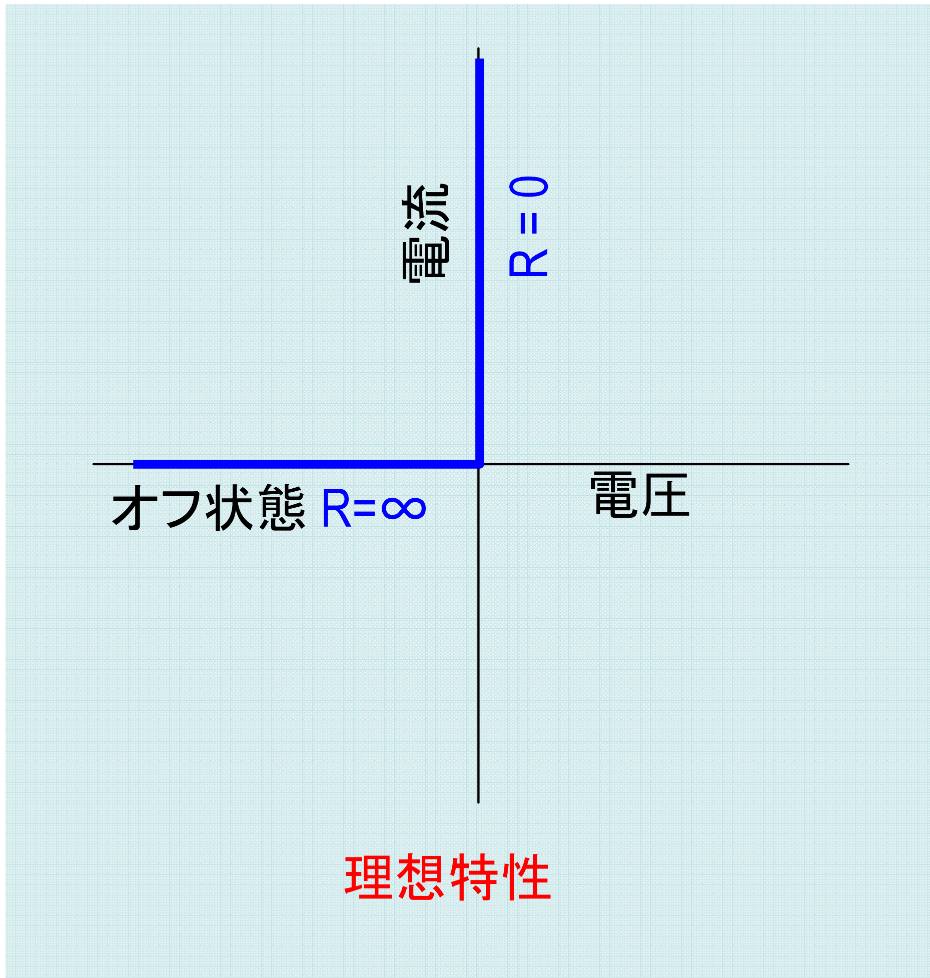


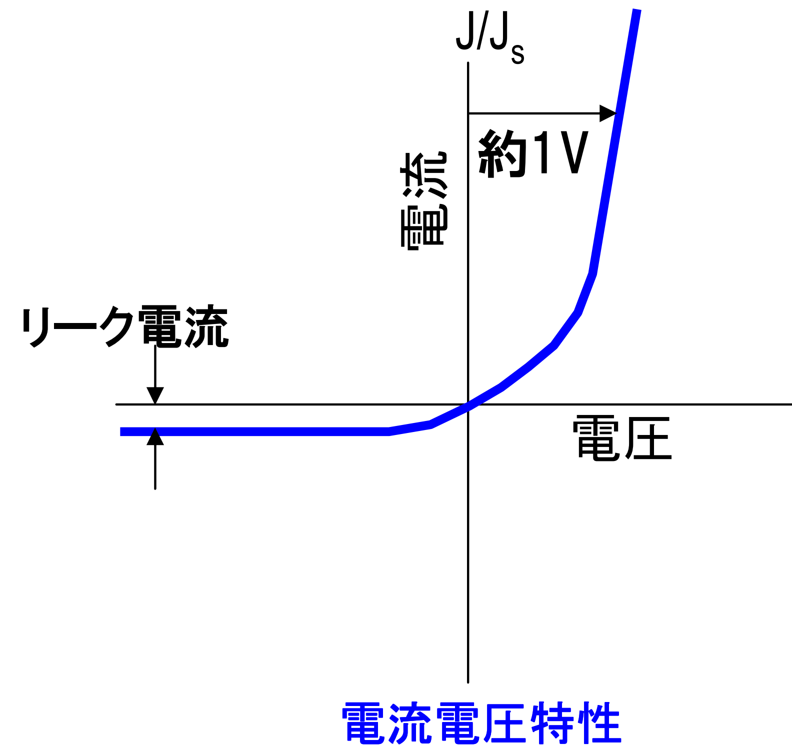
主たるパワー素子

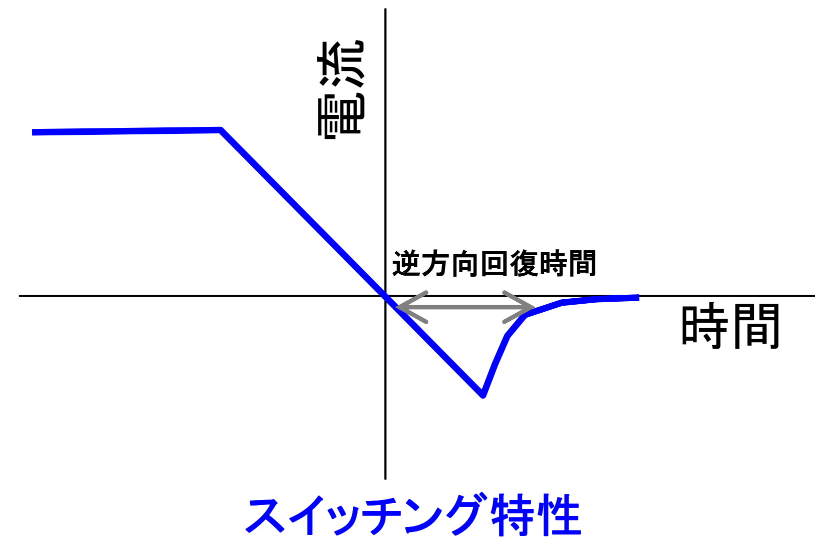



1952
1950
1960
1970
1980
1990
2000
JFET
SIT
L-MOS
Power MOS
IGBT
GTO
GCT Thy
Thyristor
BTr
Bipolar Tr
Module
SIThy
Diode
pin diode

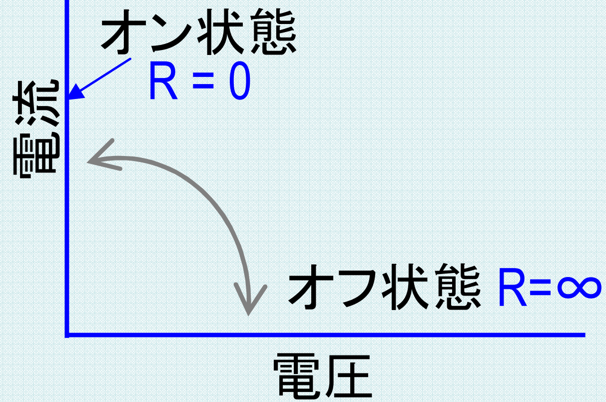
Diode特性

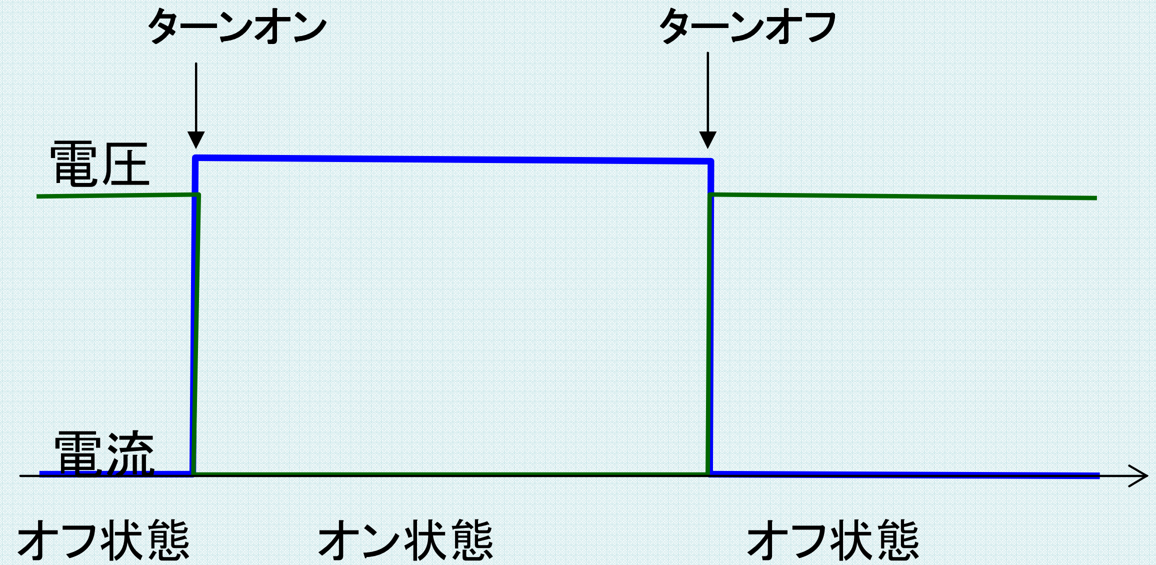


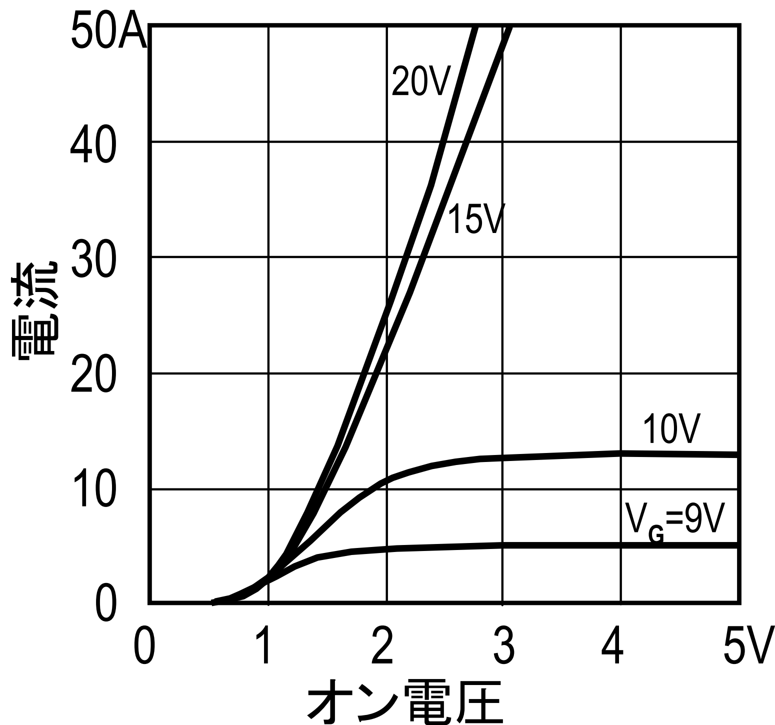


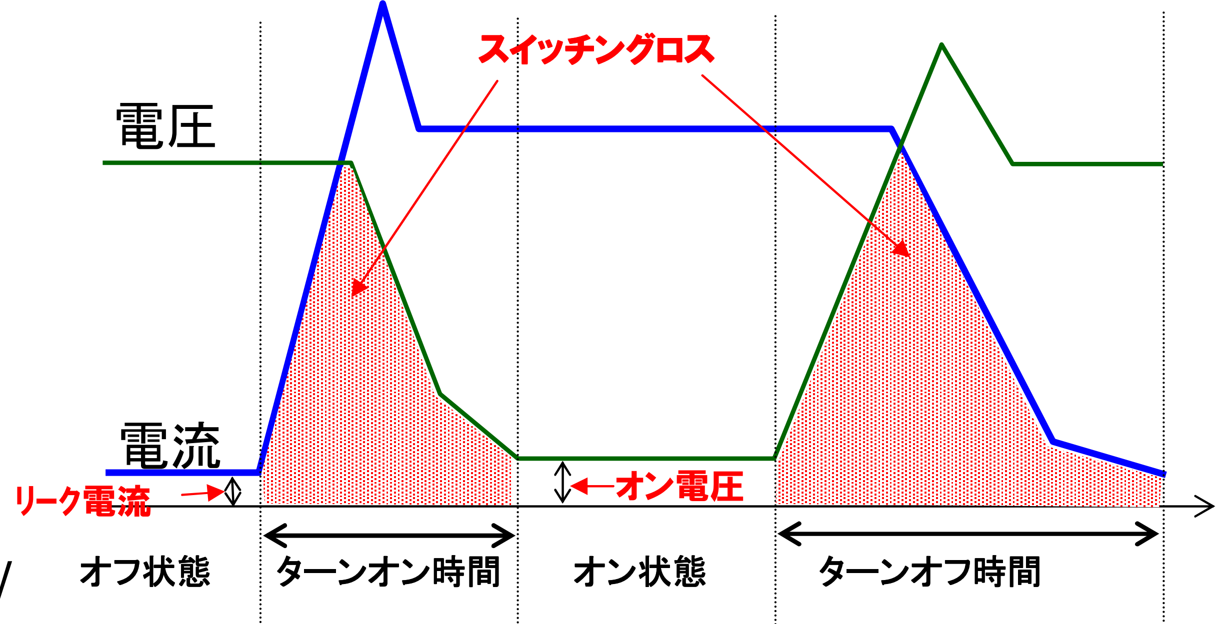


IGBT特性：スイッチ









パワー素子開発の歴史は理想スイッチに近づける。。。歴史

パワーデバイスの電力損失

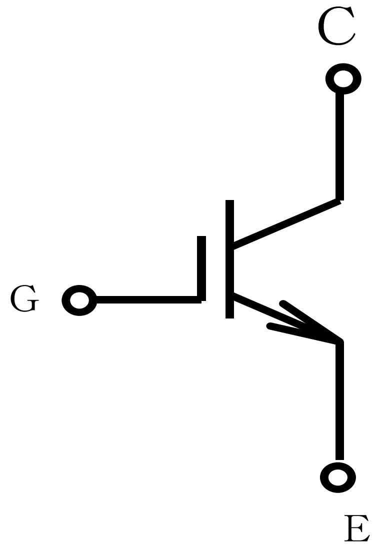
パワーデバイス部での電力損失 ＝ 導通損失 ＋ スイッチング損失

導通損失：オン時の抵抗値（オン電圧）が決定

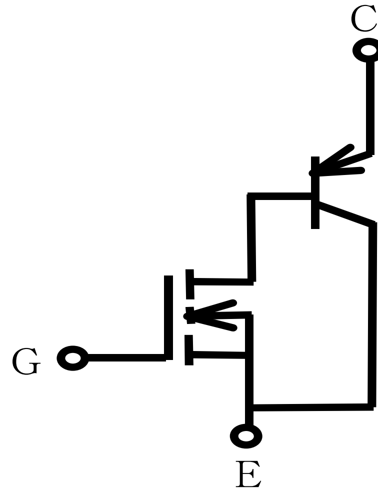
スイッチング損失：蓄積キャリアが強く影響

電力損失の低減には導通損失、スイッチング損失とも低減が必要

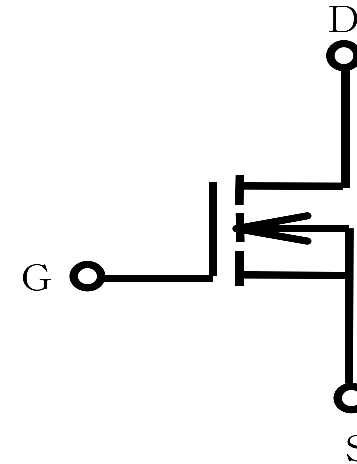
IGBT・MOSFETの記号



ＩＧＢＴ



ＩＧＢＴの等価回路



ＭＯＳＦＥＴ

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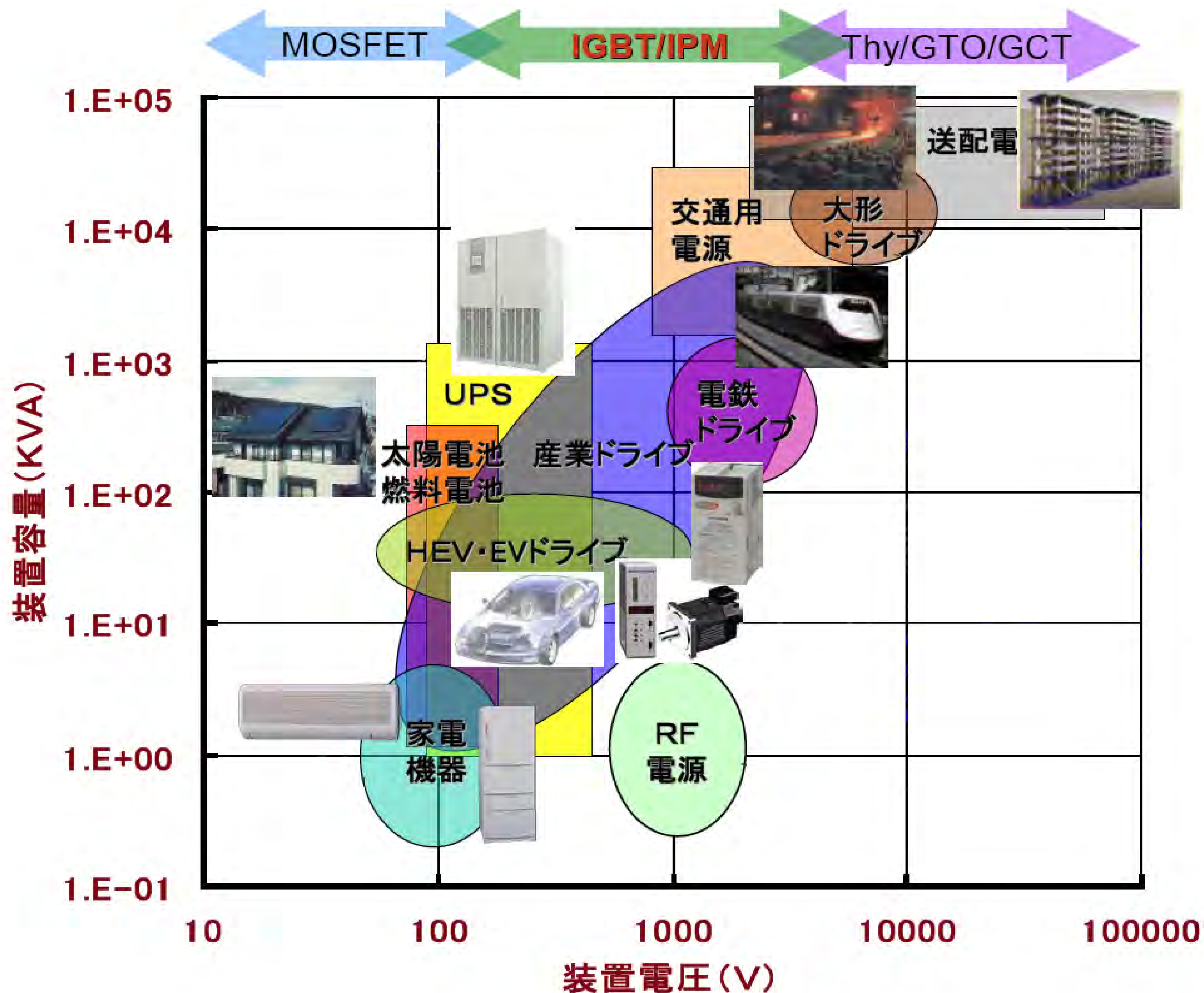
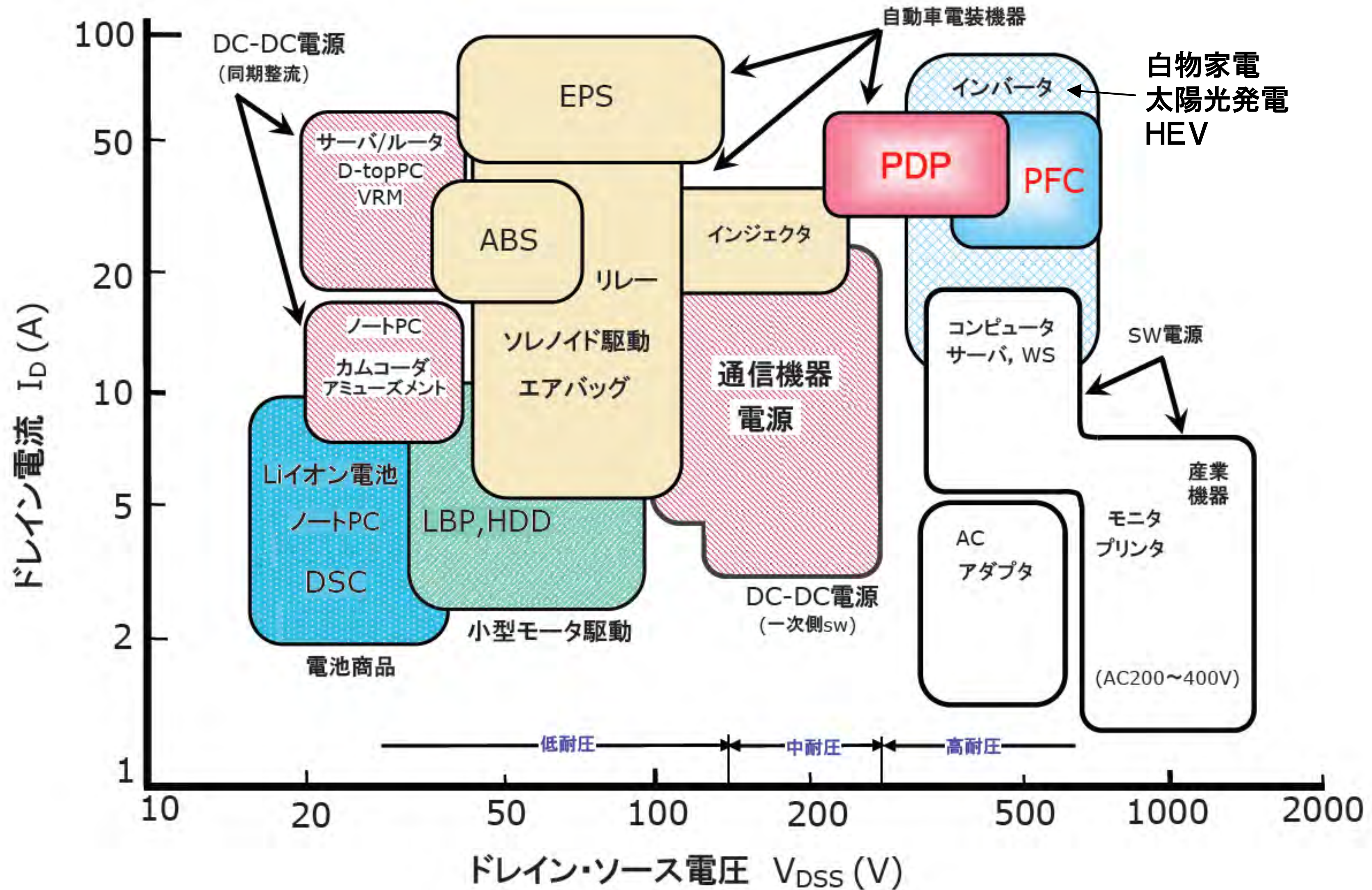
３．パワーエレクトロニクス
<u>４．パワーデバイスの市場</u>
５．IGBTとその発展の経緯
６．IGBTのシリコン限界に向けた今後の展開
７．パワーMOSFETの発展の経緯と
今後の可能性
８．新材料デバイス
９．製造プロセス
10．まとめ

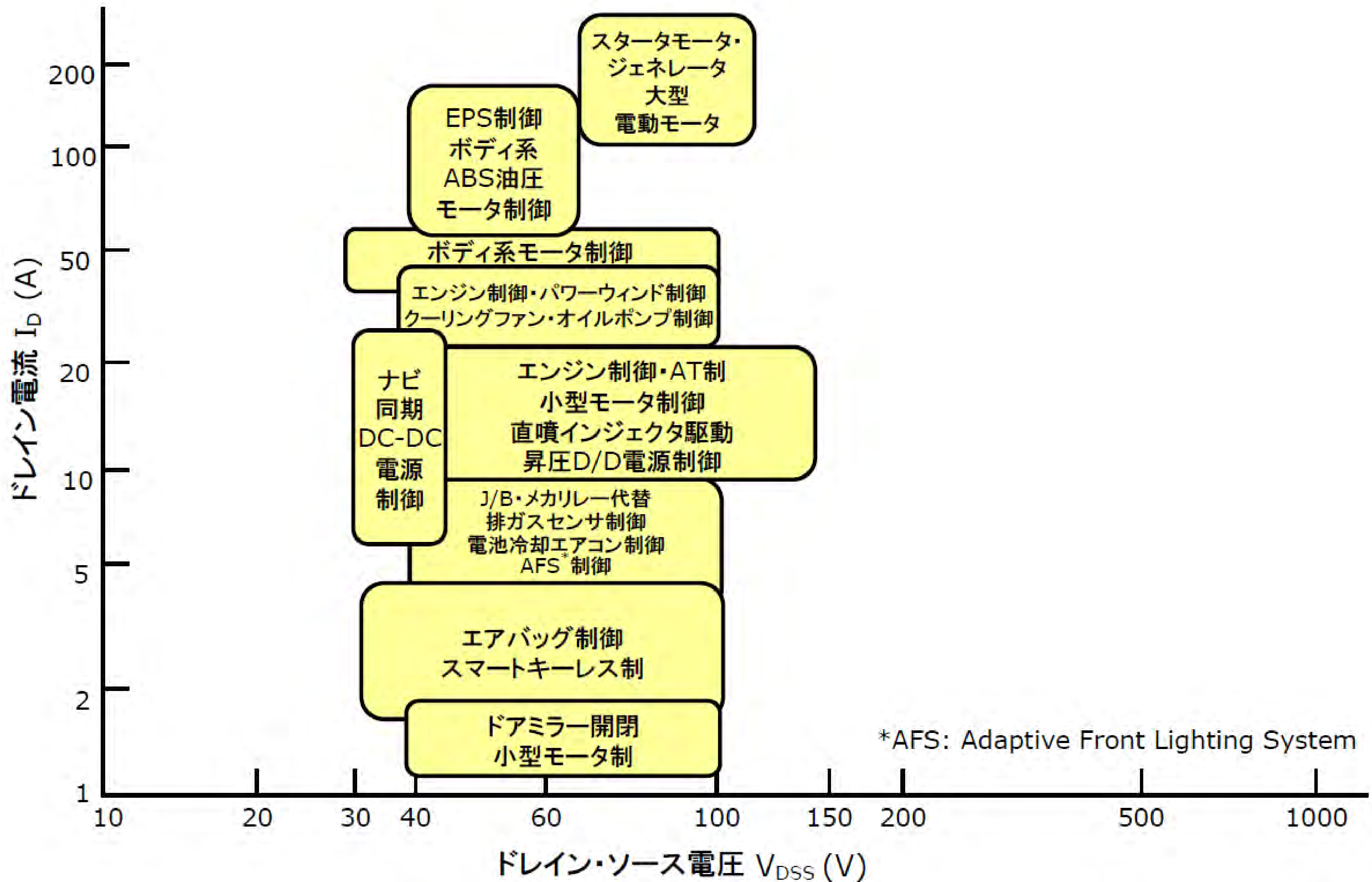
パワーデバイス応用分野(電流・電圧定格)



中小電力分野



自動車用パワーMOS FETアプリケーション



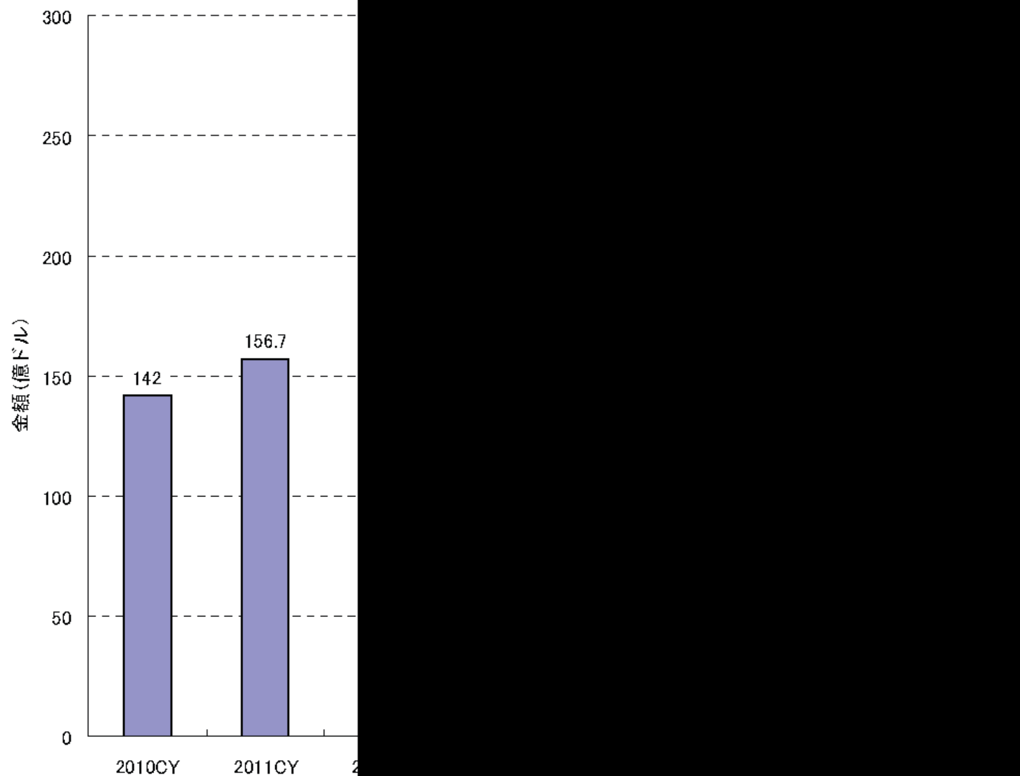
◆ 2011年のパワー半導体世界市場は，新興国向けの需要が拡大し,156億7,000万ドルに達する見込み

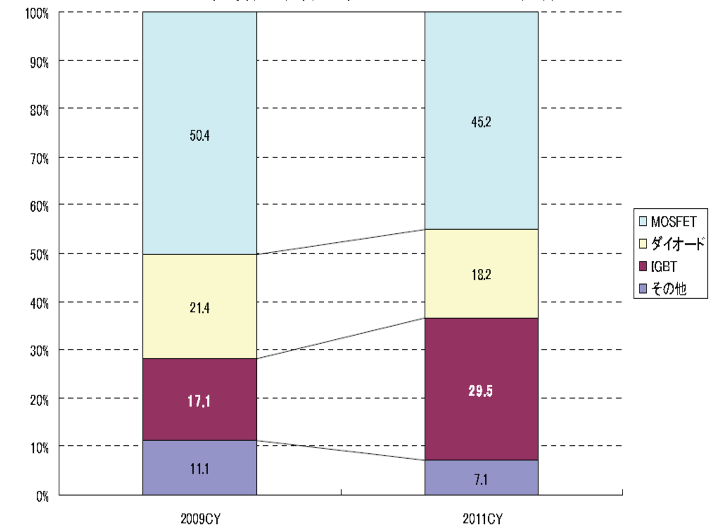
◆ 2011年のパワー半導体市場はIGBTが市場を牽引，2009年と比較して市場全体に占めるIGBTの割合は12.4%上昇

2011年の市場規模をデバイス別に分析すると、IGBTが市場全体の29.5%(46億2,000万ドル)を占めている。**新エネルギー、白物家電、次世代自動車**(HV/EV)向けのIGBTモジュールの需要拡大が進み、2009年の市場規模と比較すると、全体に占める割合は12.4%上昇する見通しである。

◆ 2017年におけるパワー半導体の世界市場は261億2,000万ドルと予測

2011年後半から太陽光発電向け投資の冷え込み、欧州の債務不安、中国における設備投資の低迷などが続いており、2012年前半のパワー半導体は厳しい市場環境となる。ただし、民生機器における在庫調整が一巡する2012年後半から緩やかな増加基調に戻る可能性が高い。中長期的には、中国におけるエアコンの省エネ基準の改定、欧州における洋上風力発電の進展、次世代自動車(HV/EV)の普及拡大など期待され、2017年のパワー半導体の世界市場は261億2,000万ドルになると予測する。





注1:メーカー出荷金額ベース
注2:2009年実績値、2011年見込値
注3:IGBTにパワーモジュール含む。その他にバイポーラトランジスタ、SiCデバイス含む。

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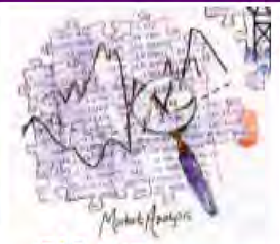
What TAM for SiC?

2006-2020 overall PE market size, split by device type



2006-2020 power device market size

MArket size (M$) / Annual Growth Rate (%)

$40 000M / $35 000M / $30 000M / $25 000M / $20 000M / $15 000M / $10 000M / $5 000M / $M

60% / 50% / 40% / 30% / 20% / 10% / 0% / -10% / -20%

	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Power IC															
Power Modules (M$)															
Discretes (M$)															
Growth rate (%)		7.7%	6.3%	-16.7%	28.0%	0.8%	4.0%	10.6%	8.1%	9.3%	7.9%	8.0%	7.6%	7.4%	7.4%

YOLE DEVELOPPEMENT

SiC can theoretically take market shares over these 2 segments

Source: Yole Développement

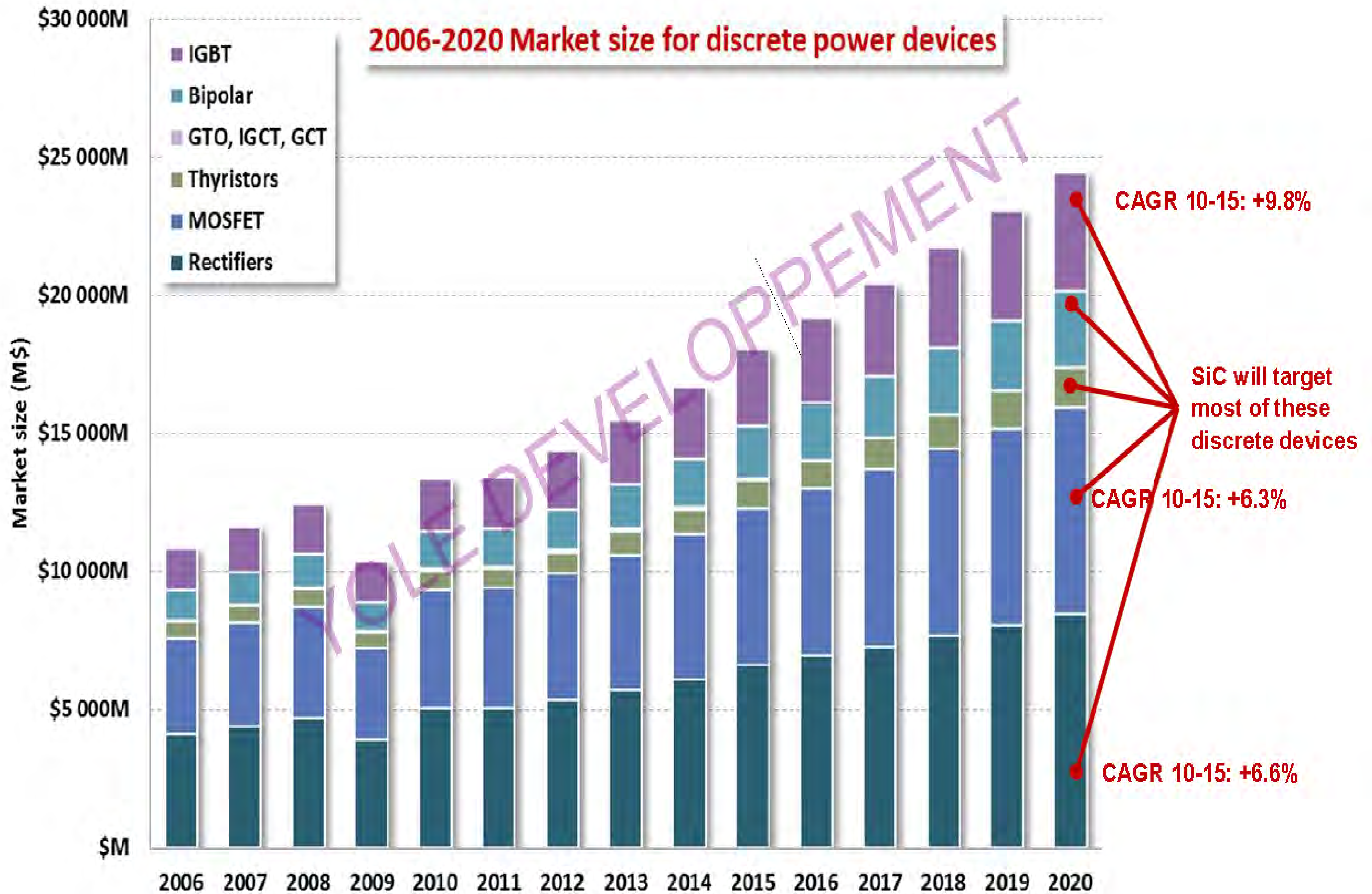
It includes:

- Power discretes: MOSFET, rectifier, IGBT, Bipolar….
- Power modules: IGBT, diode or MOSFET modules, IPM
- Power IC: power management IC: mainly voltage regulators (POL) and drivers

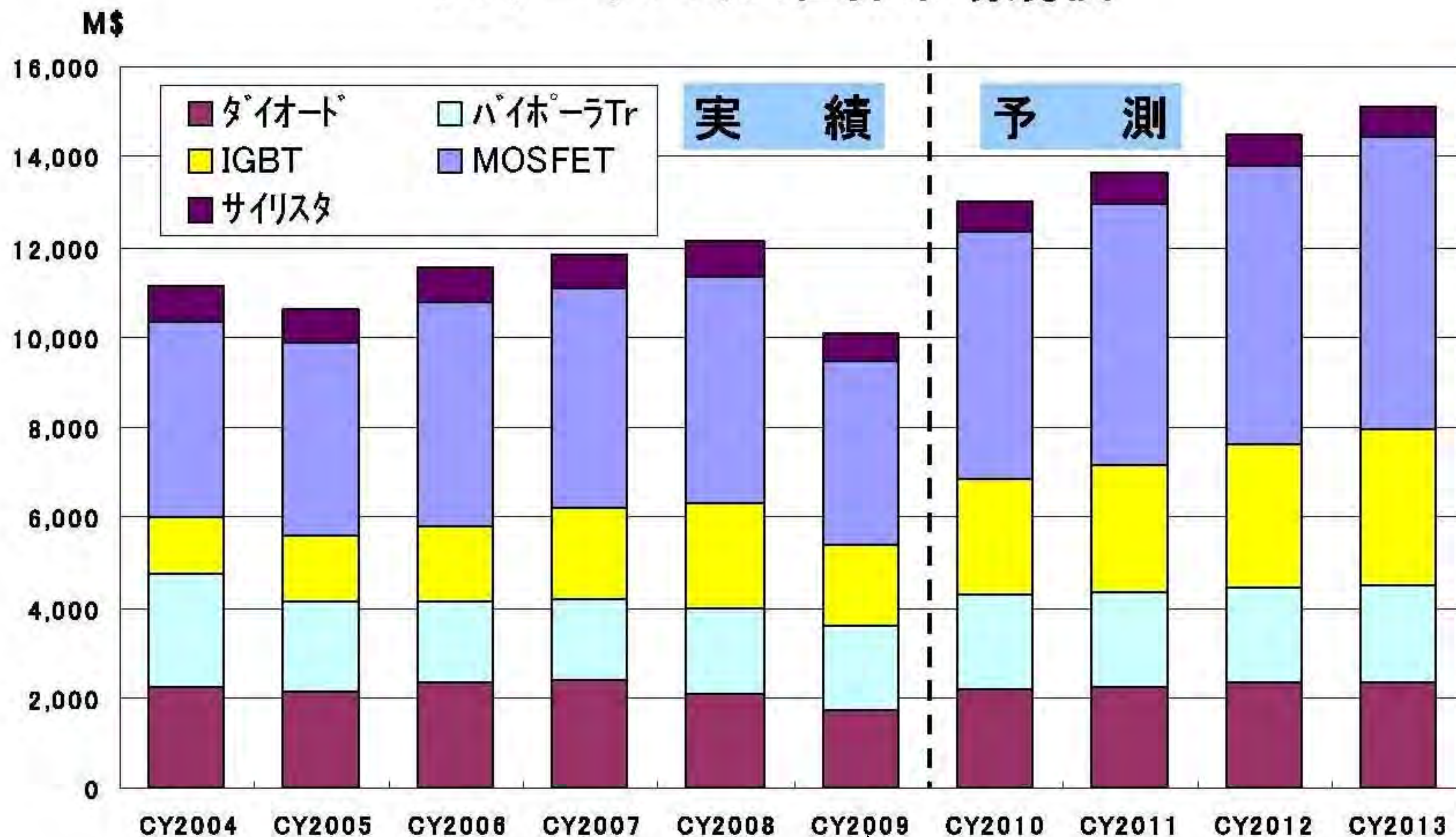
© 2012 • 10

YOLE Développement

出所：SEMI Forum Japan June 14 2012
Yole Development



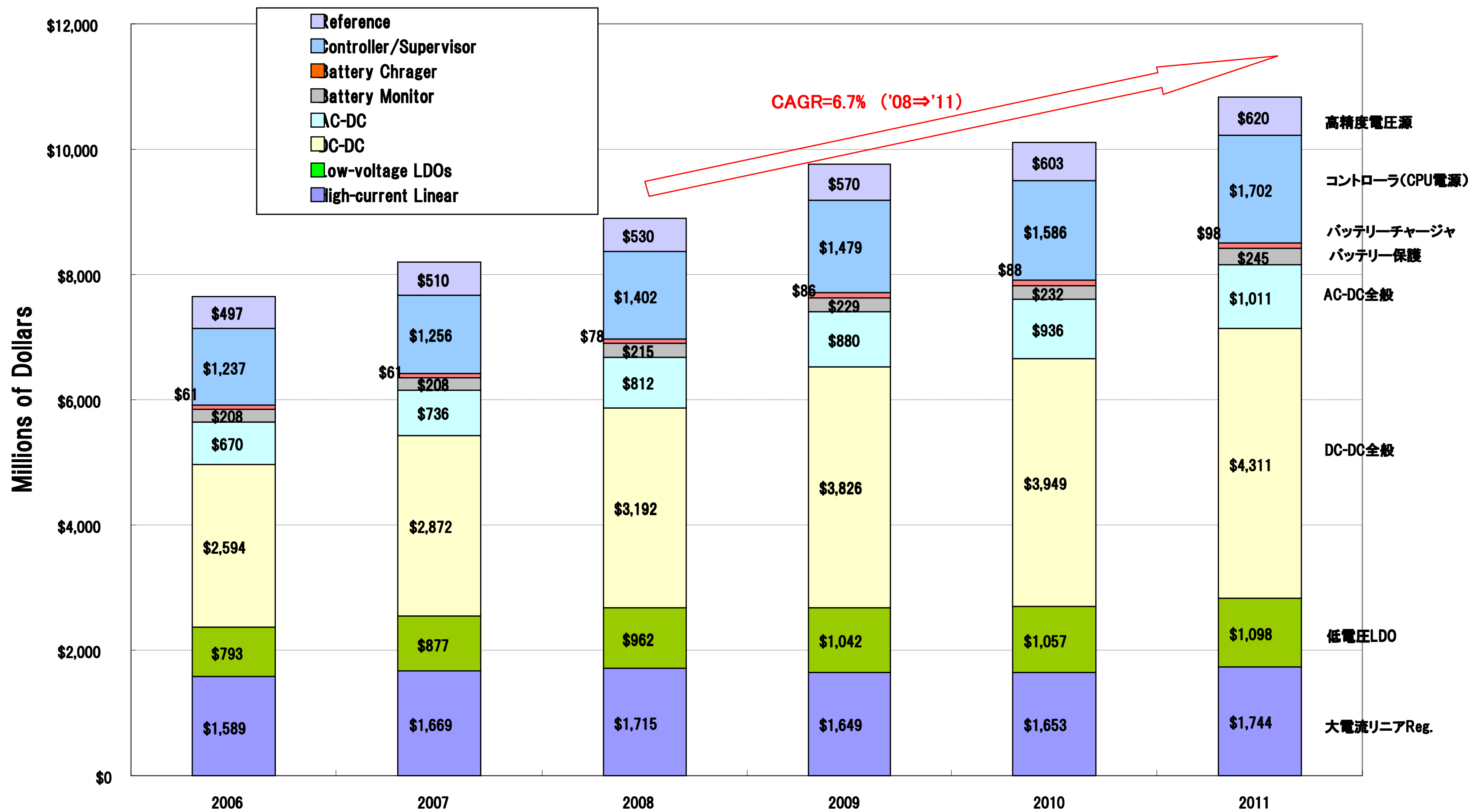
出所：SEMI Forum Japan June 14 2012
Yole Development


パワーデバイス世界市場規模
M$
16,000
14,000
12,000
10,000
8,000
6,000
4,000
2,000
0
ダイオード
バイポーラTr
IGBT
MOSFET
サイリスタ
実　績
予　測
CY2004
CY2005
CY2006
CY2007
CY2008
CY2009
CY2010
CY2011
CY2012
CY2013
出典：WSTSデータをベースに三菱電機まとめ
リーマンショック

電源半導体の世界市場

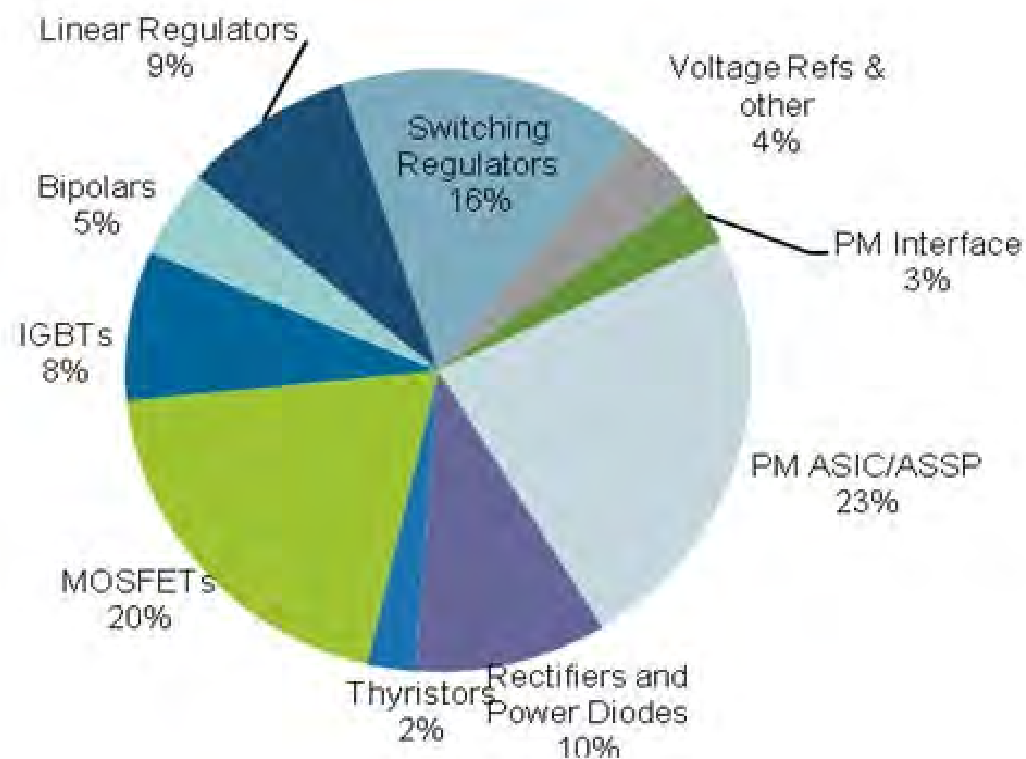
１兆円＠2010年

WW voltage regulator revenue forecast(＄M)



出典:Gartner

広義のパワーデバイス市場は２兆円超え



パワー･マネージメント半導体の2008年市場規模

出所：南川 明＝アイサプライ･ジャパン

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８. 新材料デバイス
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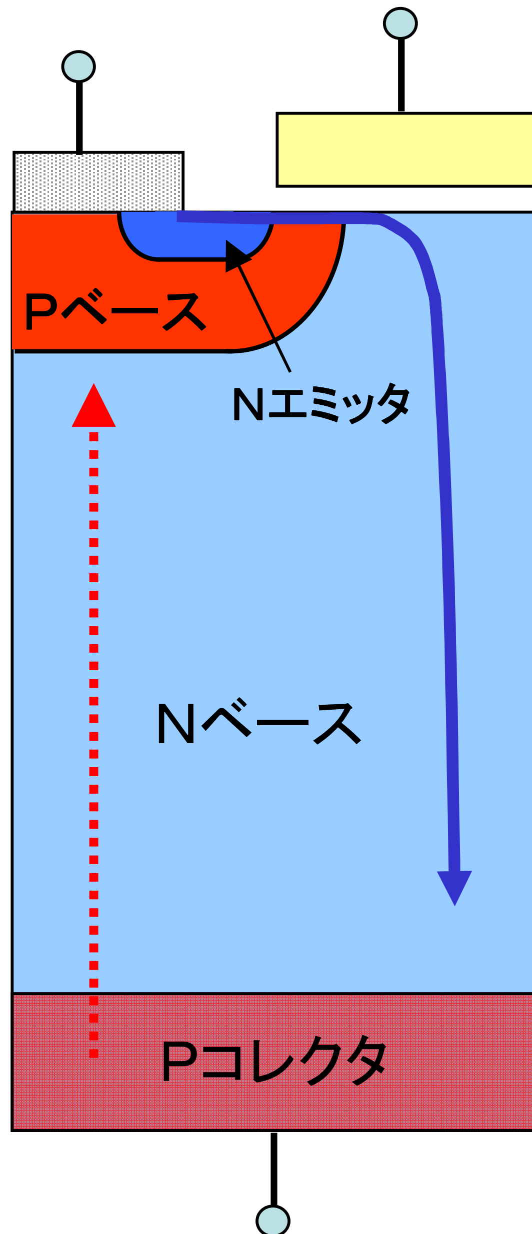
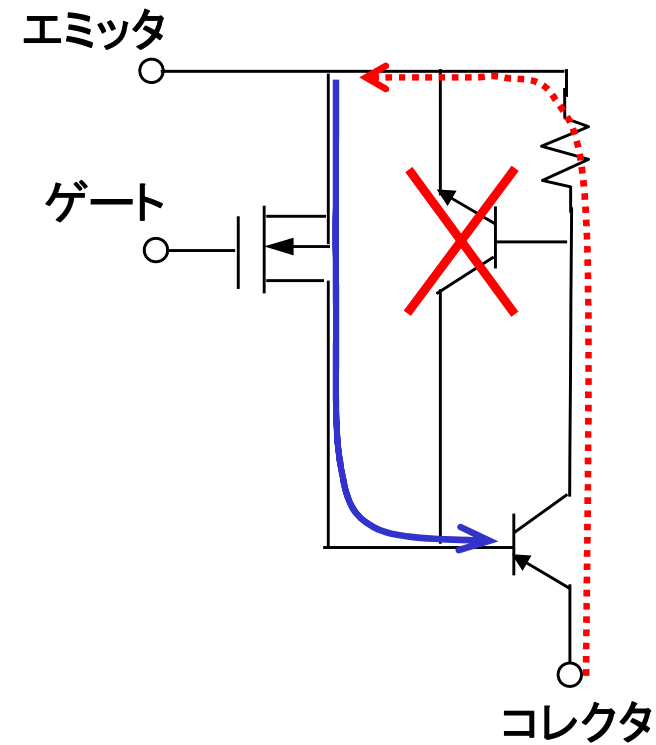
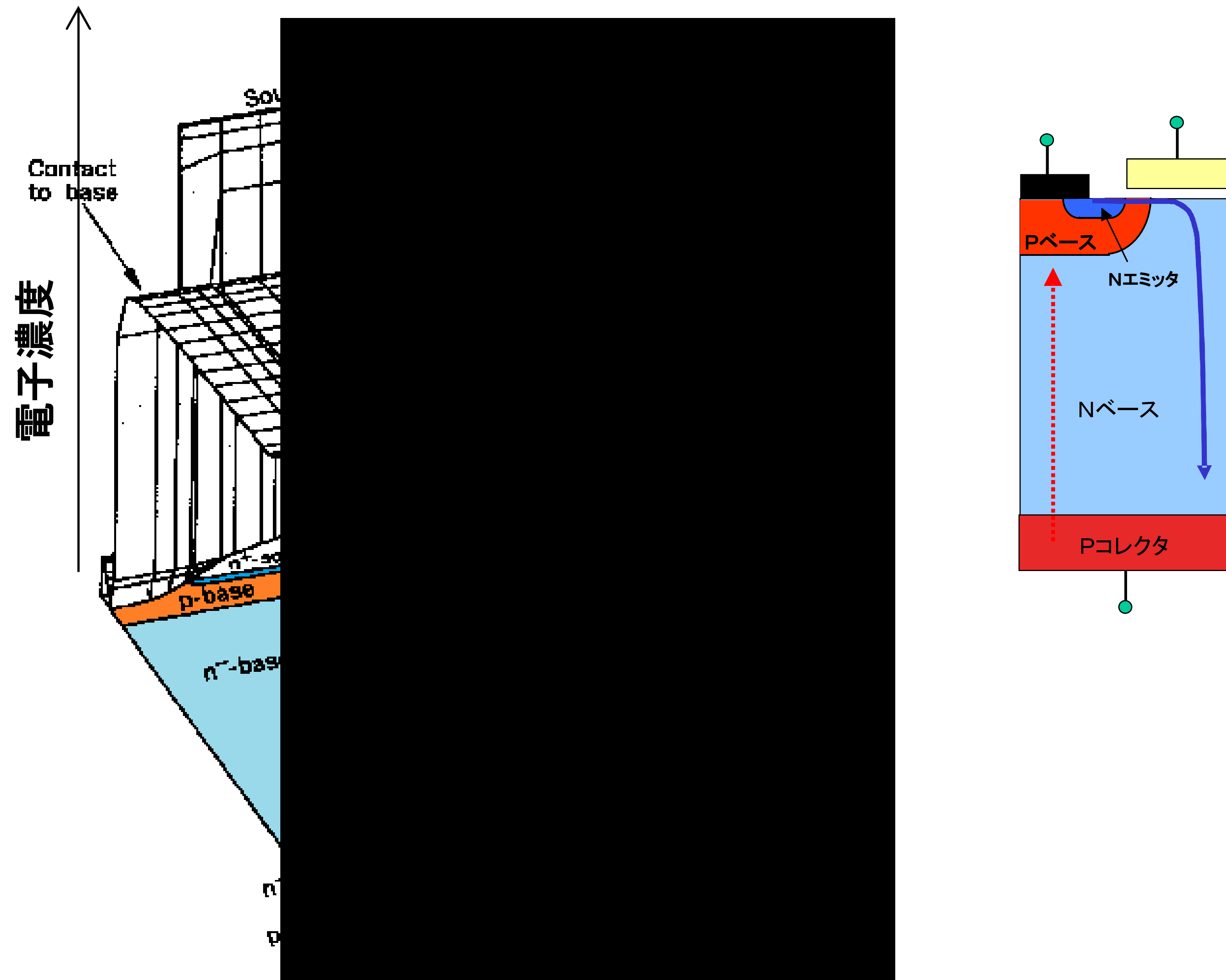
10. まとめ

IGBT(絶縁ゲートバイポーラTr)の動作

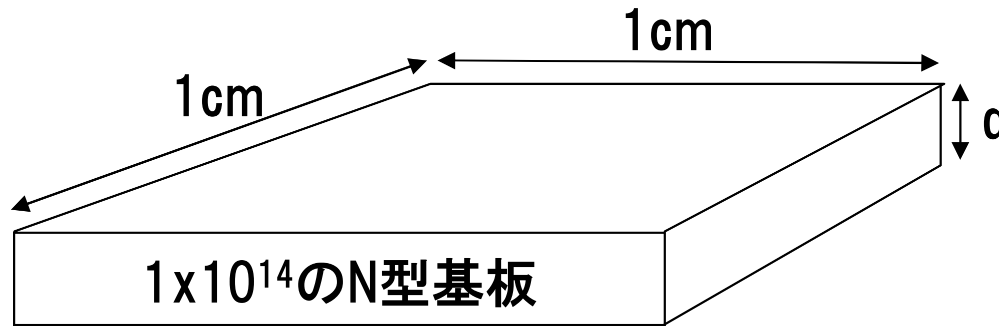






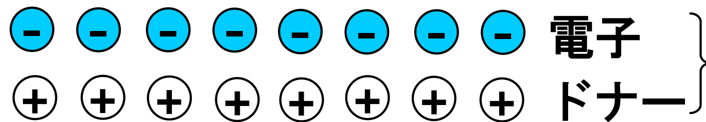
Nベースにキャリアが蓄積、伝導度変調により抵抗が下がる!!

伝導度変調（Conductivity Modulation）



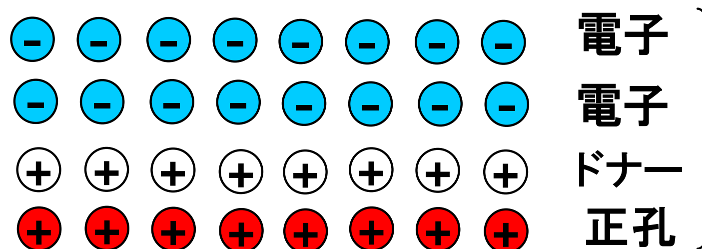
$$J = q\mu n \frac{V}{d}$$

$$R = \frac{V}{J} = \frac{d}{q\mu n} = 50 \cdot d(cm)\Omega$$



電子
ドナー

電気的中性
電子だけを増やすと大きな電圧が出てしまう。

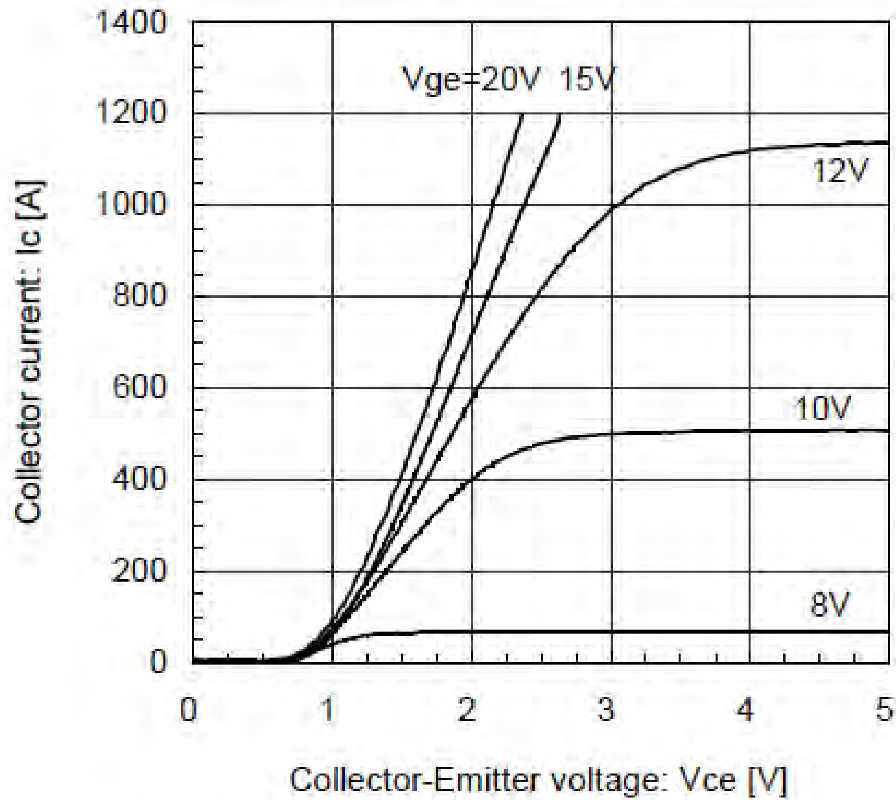


電子
電子
ドナー
正孔

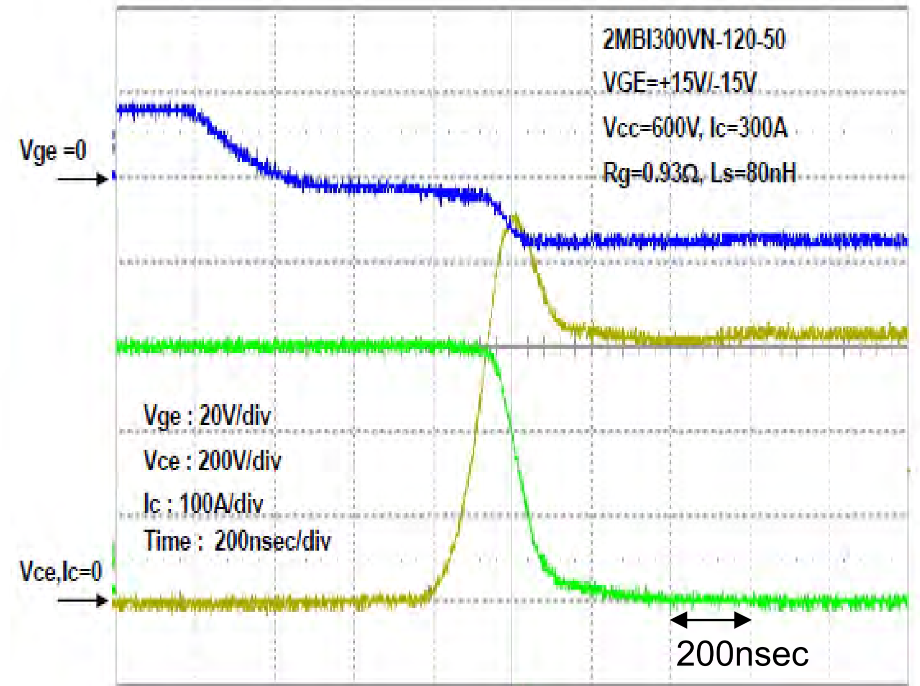
正孔と電子を同じ数だけ増やすと
電気的中性の条件を満たして抵抗が下げられる

1200V 600A素子の電流電圧特性

600V 300Aのターンオフ特性



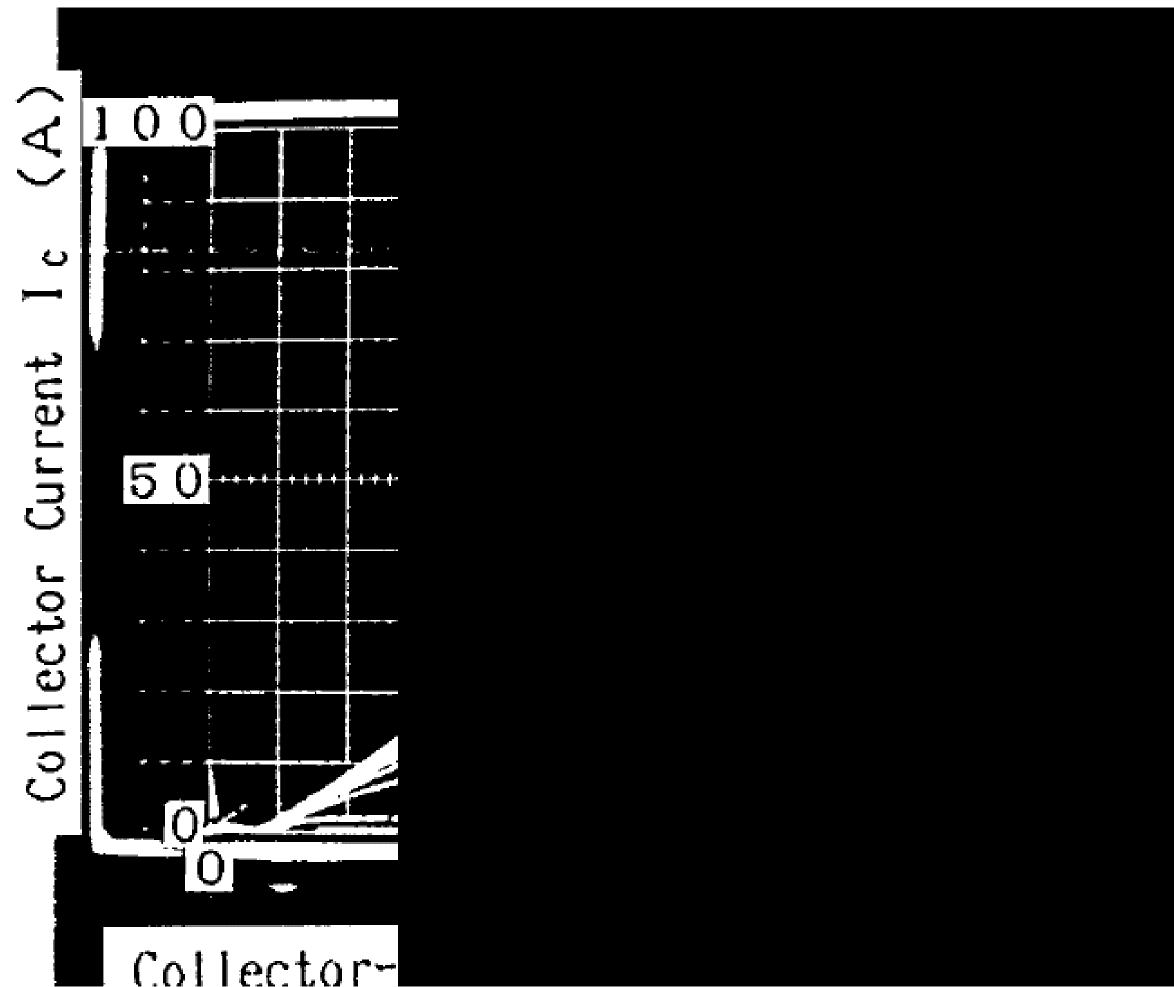
2MB1600VN-120-50



2MBI300VN-120-50(1200V/300A) ターンオフ電流・電圧波形

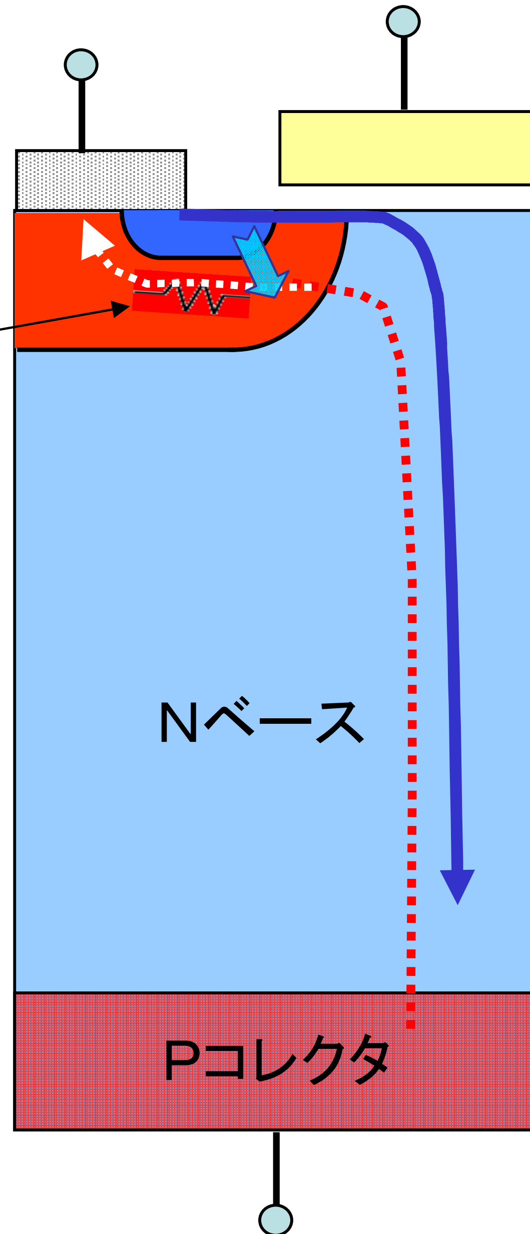
１９８３年

ＩＧＢＴは壊れやすく、ラッチアップを防ぐことは不可能に近いと考えられた!!!



ラッチアップ

Pベース抵抗の電圧降下がpn接合のビルトイン電圧を超えるとn+層からpベースに電子の注入が起き、npn Trが動作する。



高い目標を掲げる!!!

その１：
1983年 ラッチアップしない
ＩＧＢＴの開発

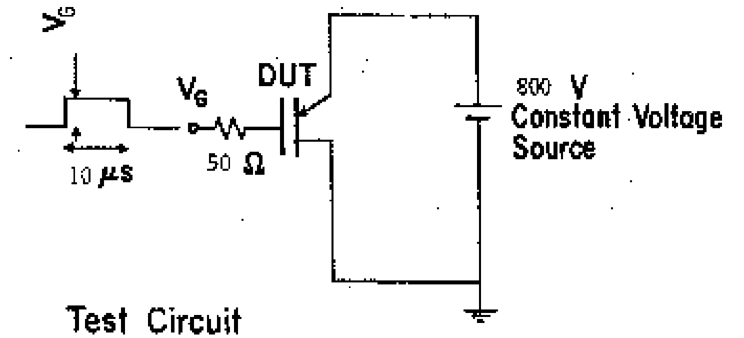
Non-Latch-Up IGBTができてしまうと、　1984年

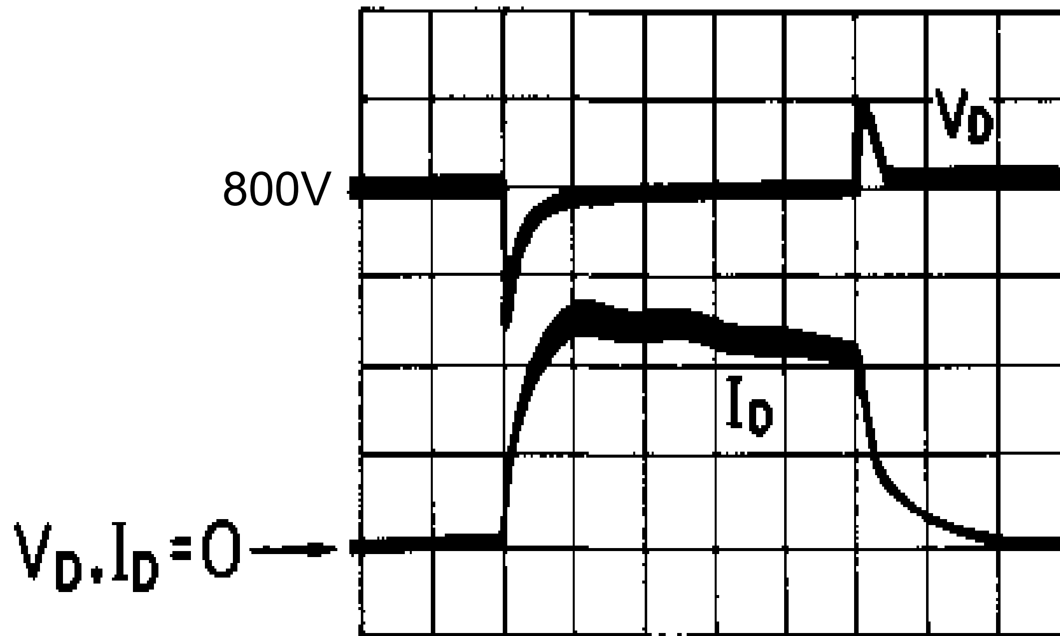
実現したNon-Latch-up IGBTは
思った以上に良い素性を持っていた!!!

ノンラッチアップIGBT最初の論文
IEDM Late News 1984年12月

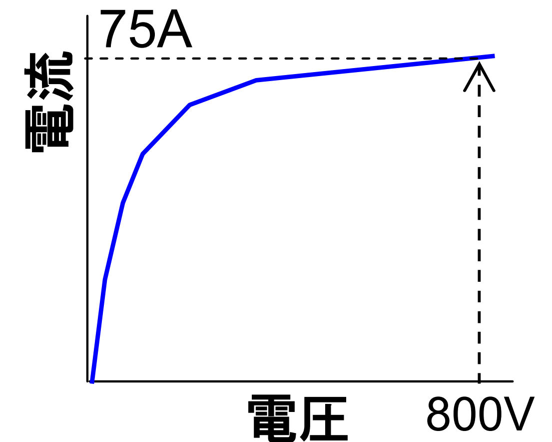
IGBTが負荷短絡に耐えられるとは誰も考えなかった!!!

『IGBTは非常に強い素子』と評価が180度転換



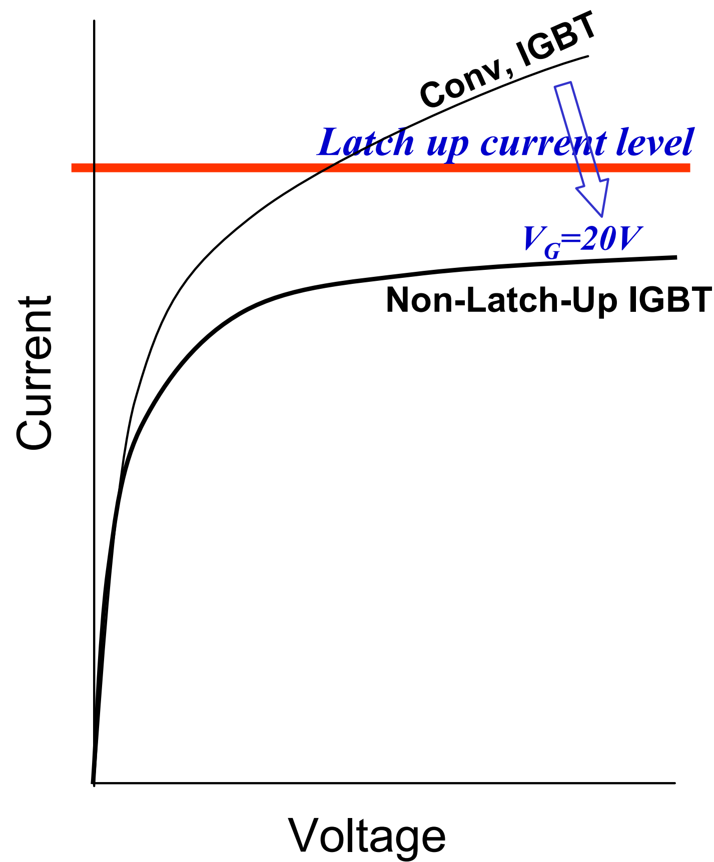


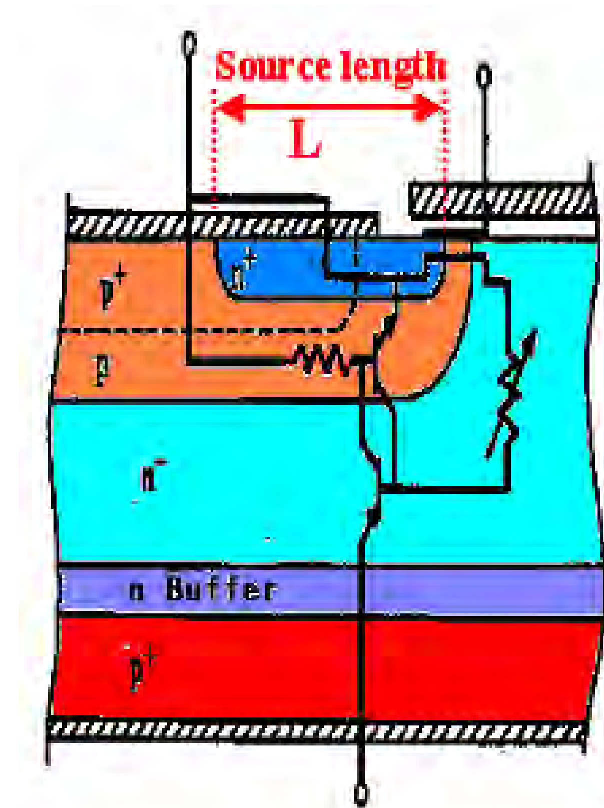
ID:30A/Div
VD:200V/Div
Time:2μs/Div



Design principle of Non-latch-Up IGBT

Saturation current(@ V_G =20V) < Latch-up current

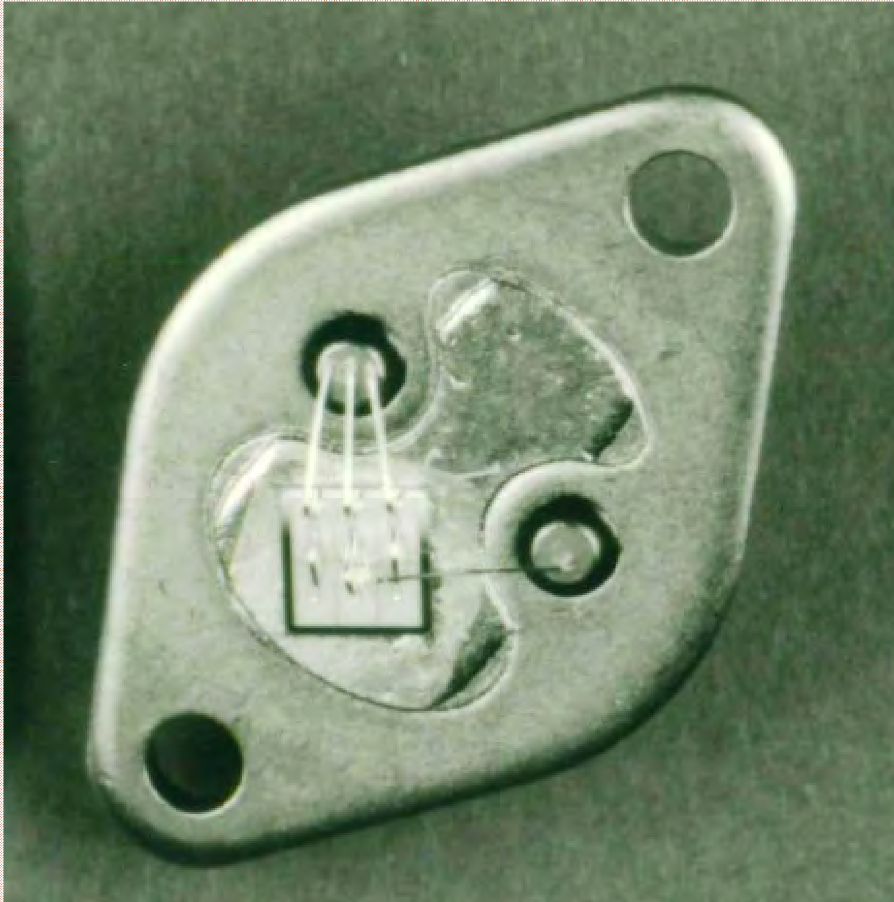




Non-Latch-Up IGBT構造

Hole Bypass： チャネルを切って低抵抗の正孔バイパスを形成

First Non-Latch-Up IGBT in 1984.



2010年　9月 IEEE William E. Newell Power Electronics Award

For development of non-latch-up IGBTs

IGBTの特許

1972 Yamagami -- He invented the basic structure of IGBT
(He filed patent only in Japan)

1978 J.D. Plummer discovered “ IGBT mode operation in thyristor”
and was grated a patent.

1980 Hans Becke invented basic idea of IGBT.
He claimed “no thyristor action occurs
under any device operating conditions”

1984 Nakagawa invented the design concept of Non-Latch-Up IGBT.
Saturation current ＜ Latch-up current

ISSCC 78

SESSION XVI: LSI DESIGN, TESTING AND INTERFACING

FAM 16.6: A MOS-Controlled Triac Device*

Brad W. Scharf and James D. Plummer

Stanford University

Stanford, CA

A MERGED DEVICE based upon double-diffused MOS (DMOS) technology and combining the MOS and thyristor families has been developed, resulting in an insulated gate triac structure applicable to areas now served by current-controlled PNPN switches. The device – MOS-controlled Triac (TRIMOS) – may be integrated with other MOS components, for use in crosspoint switching, output stages and power control.

Although it is a single regenerative device, TRIMOS can be viewed, as can I^2L, as several merged conventional components, MOSFETs, BJTs, and resistors. Such a partitioning gives rise to a circuit which can be analyzed by a nonlinear circuit analysis program to provide physical insight into the three modes of TRIMOS operation.

Figures 1 and 2(*a*), cross section and photomicrograph of TRIMOS, show that the device is formed by merging two high-voltage DMOS transistors[1] around a common drain. Contact is made to the source and diffused channel of each DMOS, forming symmetrical anode and cathode contacts, and to the shared gate metal, forming the TRIMOS control electrode.

With the cathode grounded and the gate held below the positive DMOS threshold voltage, the PN^- junction at the cathode end blocks any applied positive anode voltage, holding the switch off up to its breakdown voltage; 200V at present.

For gate potentials above threshold, there are three distinct regions of operation. In the low-level realm, anode potentials of less than about 1.5V allow both DMOS channels to become inverted. Both transistors are in their linear regions and all the anode-to-cathode current is carried by electrons at the surface. The device exhibits the low on-resistance and I-V characteristics of two short channel (2.5μ) DMOS transistors in series.

The intermediate level of operation occurs for increasing anode bias which causes the P^+N^- anode junction to become forward biased as indicated in Figure 1, serving as the emitter of a wide base PNP lateral transistor. Its injected holes drift and diffuse to the cathode P region where they are collected and contribute an added component to the device current. The result is an increase in transconductance in this region. Figure 3(*a*) shows the measured characteristics of these first two modes of operation.

As the PNP collector current increases with anode or gate potential, its flow through the pinched resistor R_p raises the potential of the cathode's P region beneath the gate and begins to turn on the vertical NPN transistor inherent in the DMOS structure. This NPN, which can be identified in Figure 4, forms with the PNP a four-layer diode which regeneratively switches when ($\alpha_{NPN} + \alpha_{PNP}$) equals unity. In its *on* state, TRIMOS exhibits a dynamic resistance of less than 10Ω and can pass currents on the order of amperes; Figure 2(*a*).

Control of the switching point by the $I_{CPNP}R_P$ product has been demonstrated by fabrication of devices with anode switching currents varying from tens of microamps to hundreds of milliamps by varying the geometrical layout. By shunting R_P with a switch (Figure 4), the TRIMOS may be switched out of its on state or inhibited from triggering. This type of shunt switch has been realized by an MOS transistor fabricated adjacent to the TRIMOS. Without such a bypass structure, a TRIMOS typically has turn-on and turn-off times on the order of 200ns and its single pulse dv/dt capability exceeds 1000V/μs.

As the discussion of operation has indicated and as Figure 4 illustrates, several bipolar and MOS transistors and resistors can be identified within the TRIMOS structure. Analysis of the circuit formed by these components has resulted in a model for operation below regeneration. A circuit analysis program containing sophisticated models of both bipolar and MOS devices must be used to obtain accurate simulation of device characteristics. This has been done on the Mini-MSINC[2] program using a DMOS model developed earlier[3] and an integral charge-control bipolar model[4,5]. The comparison of measured and modelled characteristics in Figure 3 delineates the two regions of operation and shows quantitative agreement over a rather large operating region. The apparent increase in g_m for $V_{DS} > 1.5V$ as the lateral PNP turns on is visible in both the experimental and simulated curves.

There are several advantages to the discretized model. First, it corresponds to the physical structure and aids in an intuitive understanding of the different modes of TRIMOS operation since the individual building blocks are familiar devices. Secondly, the parameters required for the model are those routinely measured on the BJT and MOSFET. Many of these can be measured directly from the TRIMOS component of interest and the others may be inferred from ordinary test structures or process characteristics. Lastly, process variations affecting the component parameters are well understood and the partitioned model translates such variations into TRIMOS performance. Thus, the impact of structure changes can be evaluated, making the model valuable for design as well as analysis.

For modeling the high current operation, after regenerative switching, common thyristor models[6] can be expected to apply within the rather stringent limitations of their approximations and the added constraints of a two-dimensional planar structure rather than one dimensional discrete devices.

*Project performed under NIH Grant No. 1 P01 GM17940-5 and NSF Grant No. ENG74-18419.

[1] Plummer, J.D. and Meindl, J.D., "A Monolithic 200-V CMOS Analog Switch", *IEEE J. Solid State Circuits*, Vol. SC-11, p. 809-817; Dec., 1976.

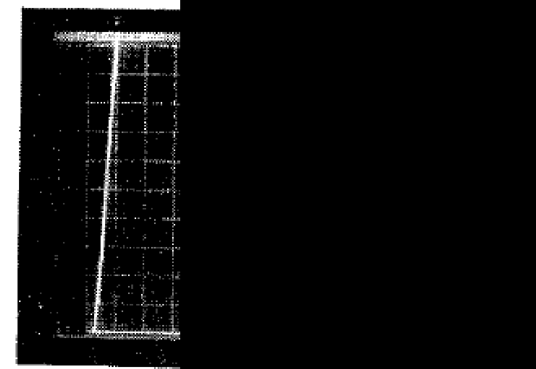
[2] Young, T.K. and Dutton, R.W., "Mini-MSINC — A Minicomputer Simulator for MOS Circuits with Modular Built-In Model", *IEEE J. Solid State Circuits*, Vol. SC-11, p. 730-732; Oct., 1976.

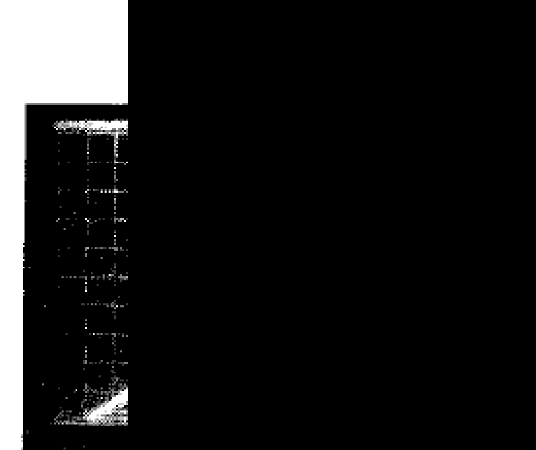
[3] Pocha, M.D. and Dutton, R.W., "A Computer-Aided Design Model of High Voltage Double Diffused MOS (DMOS) Transistors", *IEEE J. Solid State Circuits*, Vol. SC-11, p. 718-726; Oct., 1976.

[4] Gummel, H.K. and Poon, H.C., "An Integral Charge Control Model of Bipolar Transistors", *Bell System Technical Journal*, Vol. 49, p. 827-852; May/June, 1970.

[5] Divekar, D.; private communication.

[6] Blicher, A., "Thyristor Physics" (Ch. 7), *Springer-Verlag*; 1976.





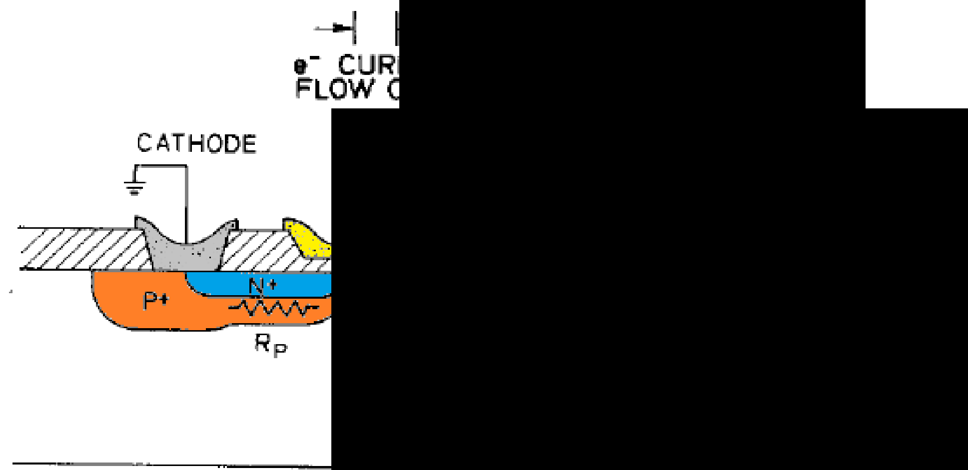


FIGURE 1—TRIM
merg

PlummerのラッチアップするIGBT特許

United States Patent [19] — **Plummer**

[11] **4,199,774**
[45] **Apr. 22, 1980**

[54] **MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE**

[75] Inventor: **James D. Plummer**, Mountain View, Calif.

[73] Assignee: **The Board of Trustees of the Leland Stanford Junior University**, Stanford, Calif.

[21] Appl. No.: **943,200**

[22] Filed: **Sep. 18, 1978**

[51] Int. Cl.² **H01L 7/02**
[52] U.S. Cl. **357/41**; 357/23; 357/55; 357/48; 307/304
[58] Field of Search 357/41, 48, 55, 23; 307/304

[56] **References Cited**

U.S. PATENT DOCUMENTS

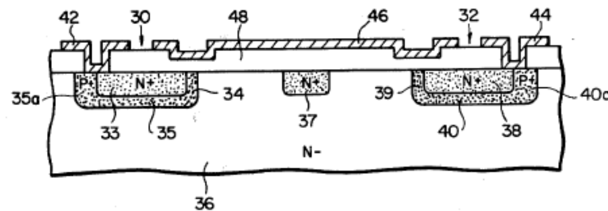
3,926,694	12/1975	Cauge	148/187
3,974,486	8/1976	Curtis	340/173 R
3,996,655	12/1976	Cunningham	29/571
4,119,996	10/1978	Jhabrola	357/23
4,145,703	3/1979	Blanchard	357/55

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.

25 Claims, 20 Drawing Figures



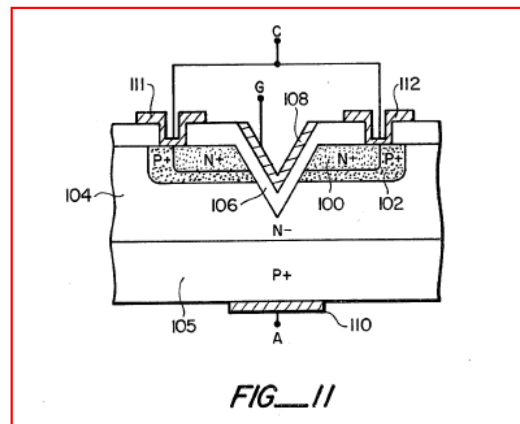


FIG.__11

United States Patent [19] — **Plummer**

[11] E Patent Number: **Re. 33,209**
[45] **Reissued** Date of Patent: **May 1, 1990**

[54] **MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE**

[75] Inventor: **James D. Plummer**, Mt. View, Calif.

[73] Assignee: **Board of Trustees of the Leland Stanford Jr. Univ.**, Stanford, Ill.

[21] Appl. No.: **539,111**

[22] Filed: **Dec. 5, 1983**

Related U.S. Patent Documents

Reissue of:
[64] Patent No.: **4,199,774**
Issued: **Apr. 22, 1980**
Appl. No.: **943,200**
Filed: **Sep. 18, 1978**

[51] Int. Cl.⁵ **H01L 29/78**
[52] U.S. Cl. **357/23.4**; 357/23.9; 357/39; 357/48; 357/55; 357/41
[58] **Field of Search** 357/23.4, 23.9, 55, 357/48, 41, 39

[56] **References Cited**

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3,996,655	12/1976	Cunningham	29/571
4,072,975	2/1978	Ishitami	357/23.4
4,119,996	10/1978	Jhabrola	357/23
4,145,703	3/1979	Blanchard	357/23.4 X

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] **ABSTRACT**

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.

20 Claims, 4 Drawing Sheets

1. A monolithic semiconductor *SCR device* comprising:

a semiconductor [body] *substrate of one conductivity type and an epitaxial layer of opposite conductivity type, said epitaxial layer* having at least one major surface, and

[a body region adjacent to said surface of one conductivity type,] first and second spaced regions of [opposite] *said one* conductivity type formed in said [body region] *epitaxial layer* and abutting said major surface, third and fourth regions of said [one conductivity] *opposite conductivity* type formed in said first and second regions, respectively, abutting said major surface and defining first and second channel regions in said first and second regions, respectively,

a layer of insulation on said major surface,

a gate electrode formed on said layer of insulation and above said first and second channel regions, an ohmic contact to said first and third regions, and an ohmic contact to said second and fourth regions, *and*

an ohmic contact to said semiconductor substrate.

BeckeのIGBT特許

United States Patent [19] — **Becke et al.**

[11] **4,364,073**
[45] **Dec. 14, 1982**

[54] **POWER MOSFET WITH AN ANODE REGION**

[75] Inventors: **Hans W. Becke**, Morristown; **Carl F. Wheatley, Jr.**, Somerset, both of N.J.

[73] Assignee: **RCA Corporation**, New York, N.Y.

[21] Appl. No.: **133,902**

[22] Filed: **Mar. 25, 1980**

[51] Int. Cl.³ **H01L 29/00**
[52] U.S. Cl. **357/23**; 357/37
[58] Field of Search .... 357/37, 38, 23, 23 R

[56] **References Cited**

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3,900,771 8/1975 Krause 357/38
4,199,774 4/1980 Plummer 357/23

FOREIGN PATENT DOCUMENTS

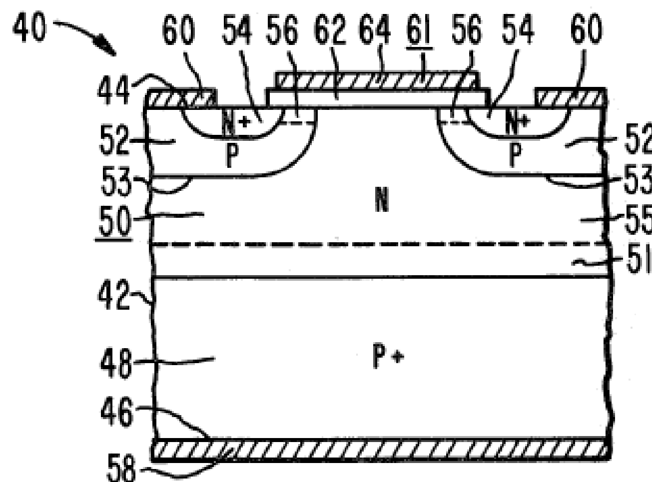
1367325 9/1974 United Kingdom .
2034114 5/1980 United Kingdom .

Primary Examiner—R. A. Rosenberger
Attorney, Agent, or Firm—Birgit E. Morris; Donald S. Cohen; Kenneth R. Glick

[57] **ABSTRACT**

A vertical MOSFET device having source, body and drain regions, includes an anode region in series with the drain region. The source, body and drain regions have a first forward current gain and the anode, drain and body regions have a second forward current gain, such that the sum of the current gains is less than unity. The anode region provides minority carrier injection into the drain region, enhancing device performance in power applications.

17 Claims, 5 Drawing Figures



1. A vertical MOSFET device, comprising:
a semiconductor substrate, including in series, adjacent source, body, drain and anode regions of alternate conductivity type;
the body region being adjacent to a surface of the substrate;
the source and drain regions being spaced so as to define a channel portion in the body region at said surface;
the source, body and drain regions having a first forward current gain α_1 and the anode, drain and body regions having a second forward current gain α_2, such that the sum $\alpha_1+\alpha_2$ is less than unity, and no thyristor action occurs under any device operating conditions.

IGBTの特許

1978 J.D. Plummer discovered “ IGBT mode operation in thyristor”
and was grated a patent.

GE(バリガ)のIGBTはラッチアップするPlummer特許の範囲

1980 Hans Becke invented basic idea of IGBT.
He claimed “no thyristor action occurs
under any device operating conditions”

**Becke特許はnon-latch-up IGBTsの出現で
IGBTの基本特許に昇格!!!**

現在のIGBTはPlummer特許には抵触しない!!

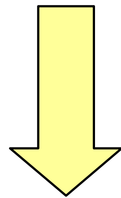
1984 Nakagawa invented the design concept of Non-Latch-Up IGBT.
Saturation current ＜ Latch-up current

高い目標 その２：

無謀とも言う
べき課題

BTrはIGBT化できた!

次はGTOのMOSゲート化



POST-GTO PJの発足＠1989年

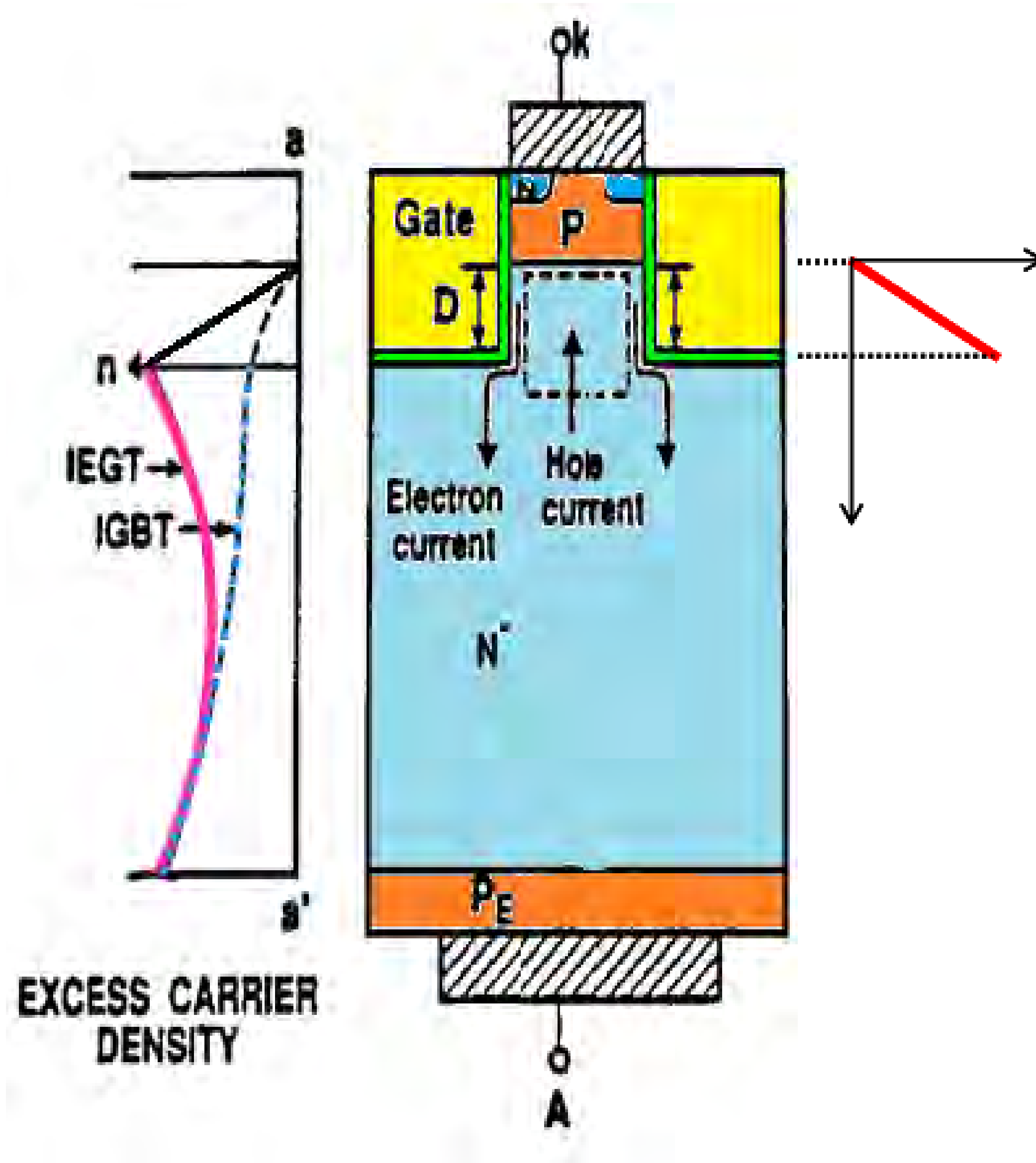
IGBTはオン電圧が高いという先入観から
MOSGTOを試作・検討するが全くうまく行かない!!!

--- 行き詰る ---

デバイスシミュレータによる試行錯誤の検討!!!

1990年 Injection Enhanced IGBT（IE効果）の発見

デバイスシミュレータでの予測　(特許出願1991、発表1993)



正孔電流 $J_p = qD_p \dfrac{\partial p}{\partial x}$

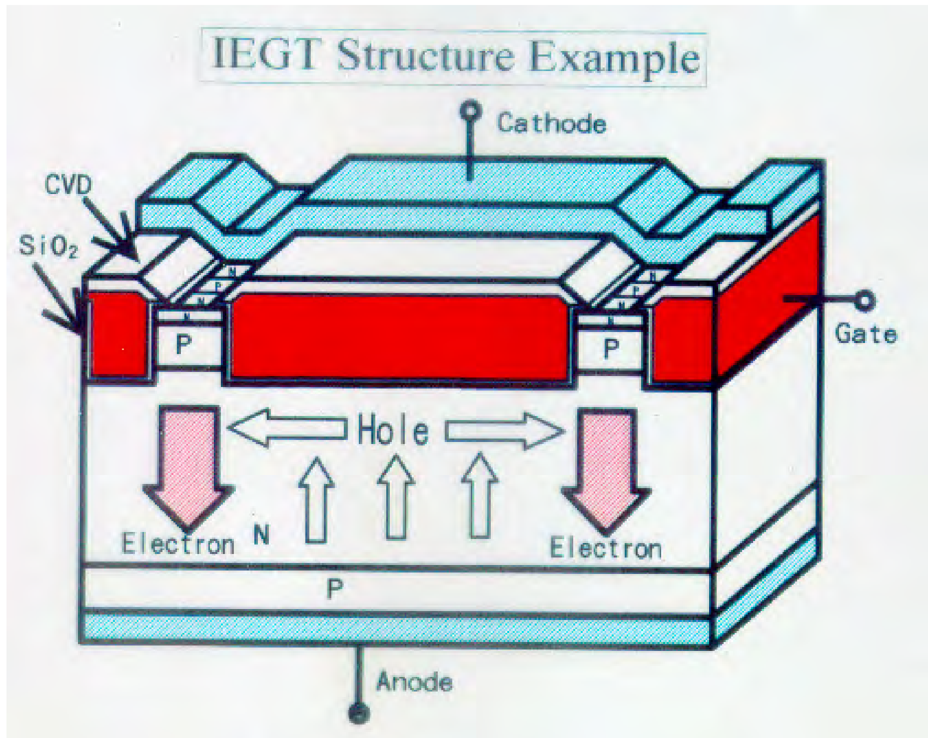
キャリアの勾配で
正孔を蓄積

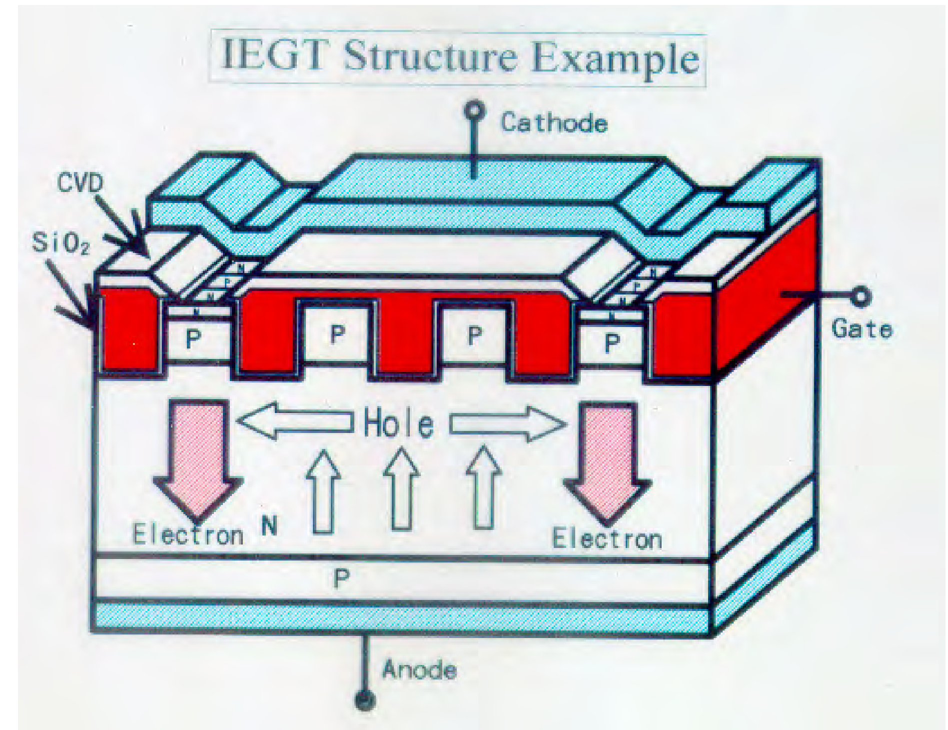
サイリスタのキャリア分布を実現

Kitagawa, 1993 IEEE IEDM Tech. Digest, pp.679

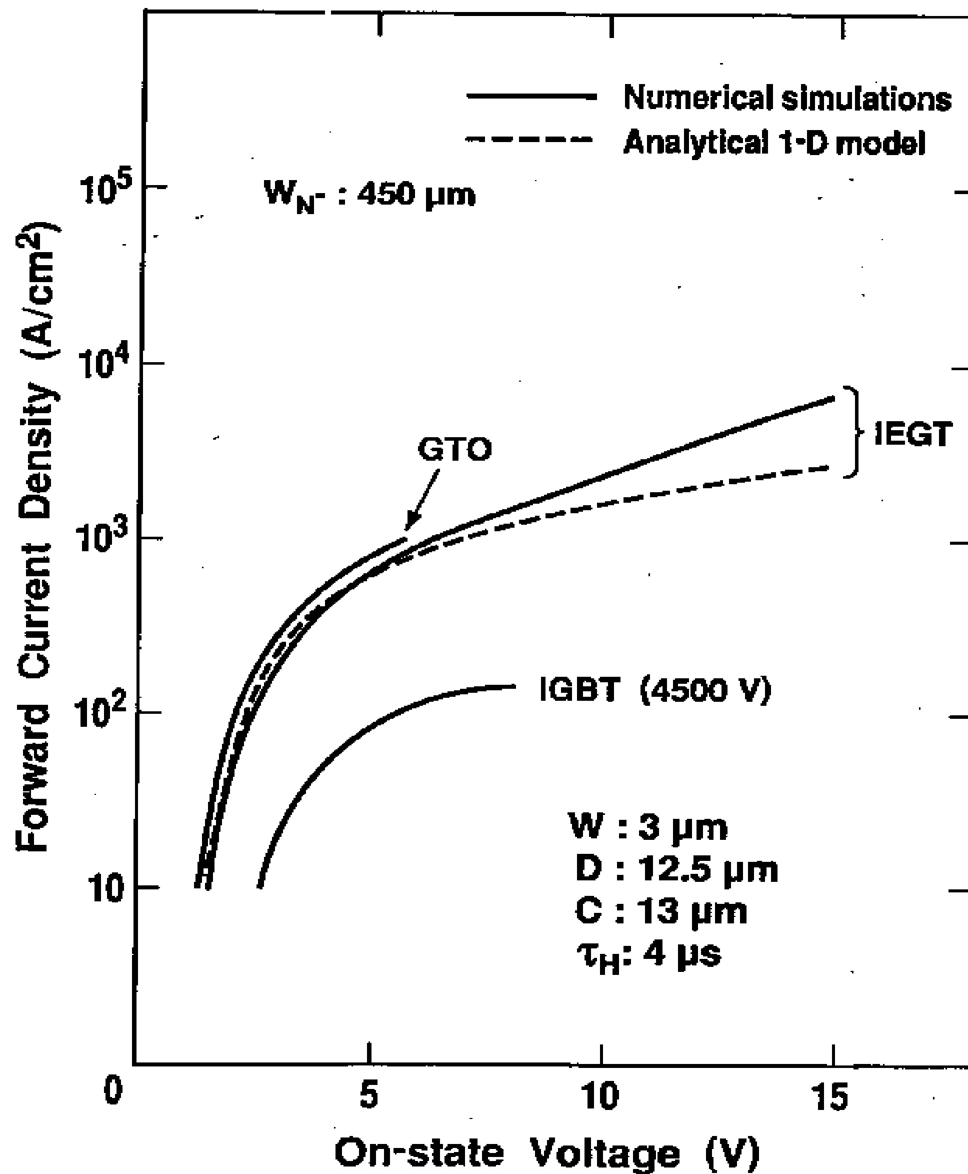
理想のIEGT

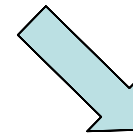
現実的構造





2000年 4.5kV IEGTの実現へ

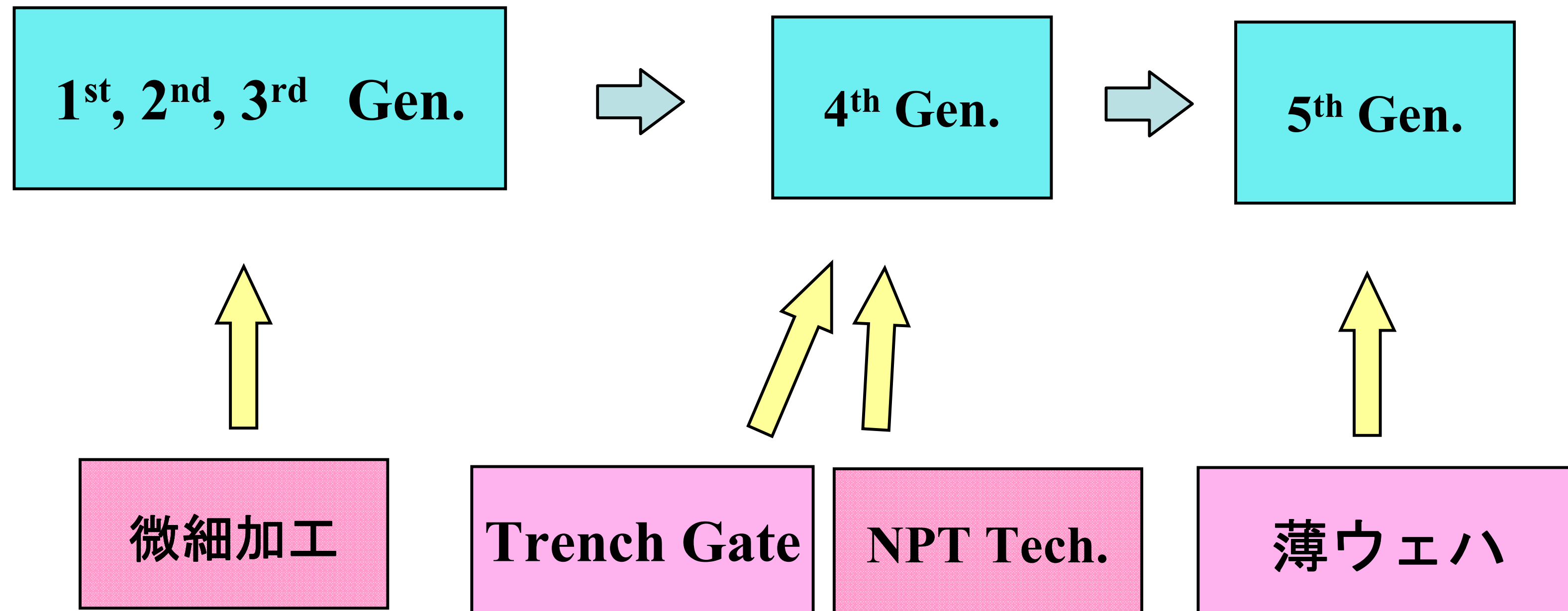




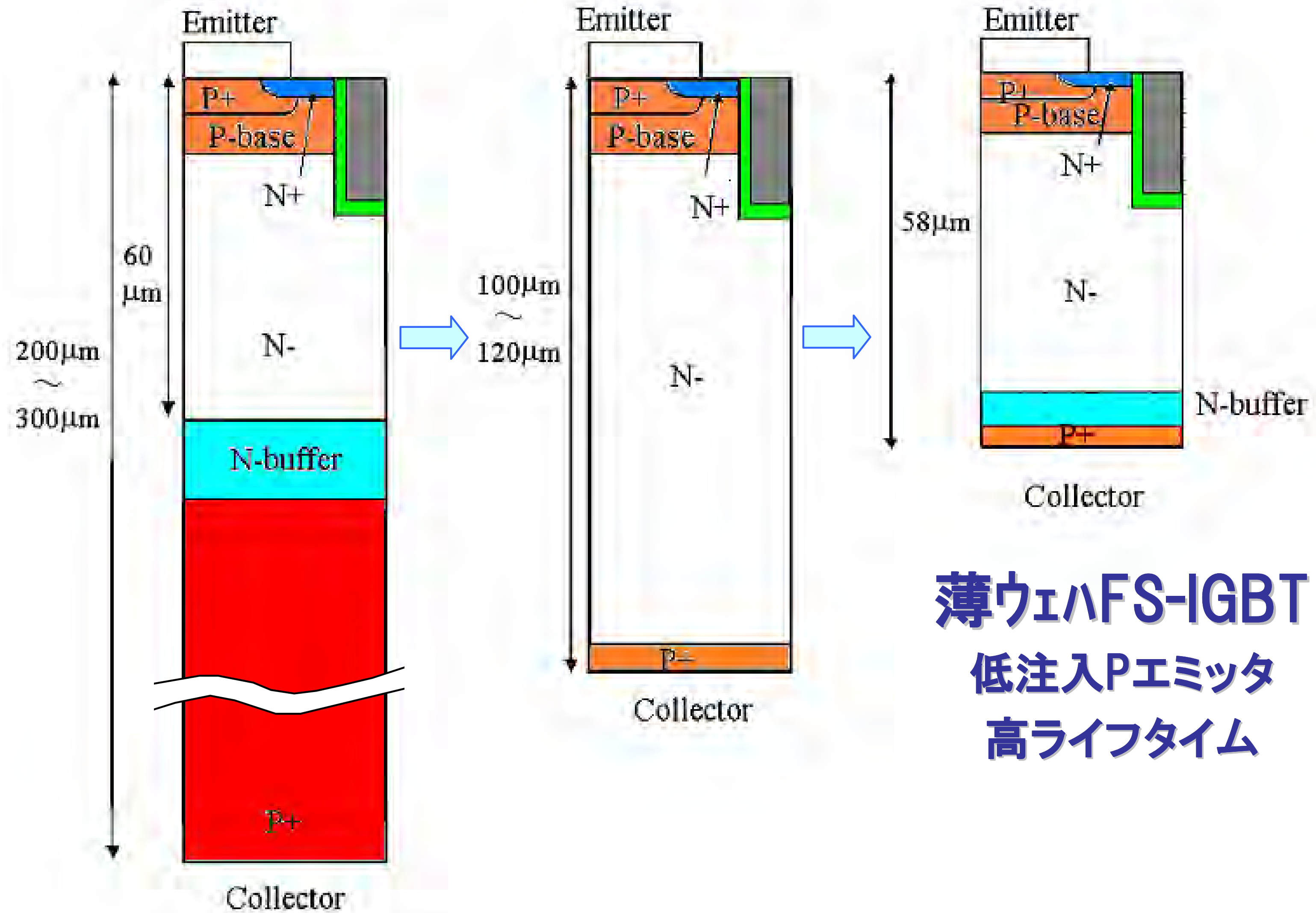
1995年 圧接型パッケイジ
2.5kV圧接型IGBT

2000年 4.5kV IGBT（IEGT)

600-1200V IGBT
技術トレンド



代表的IGBT構造



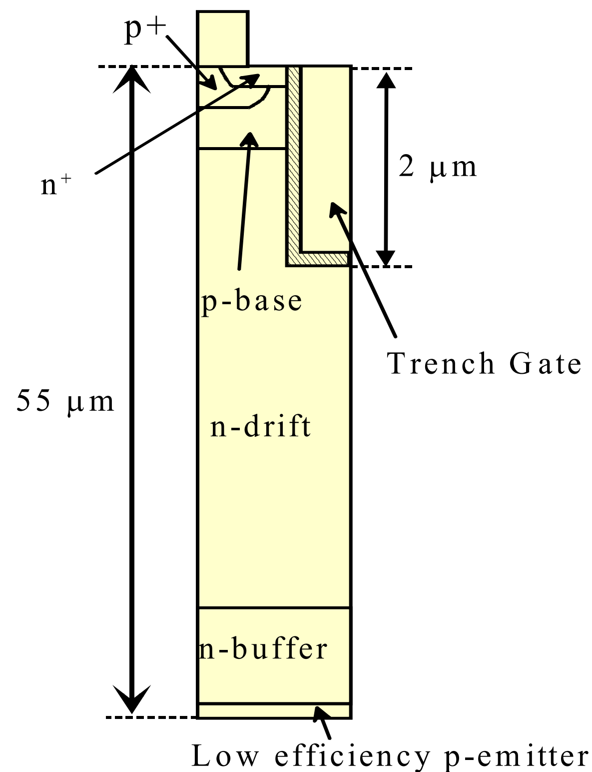
薄ウェハFS-IGBT
低注入Pエミッタ
高ライフタイム

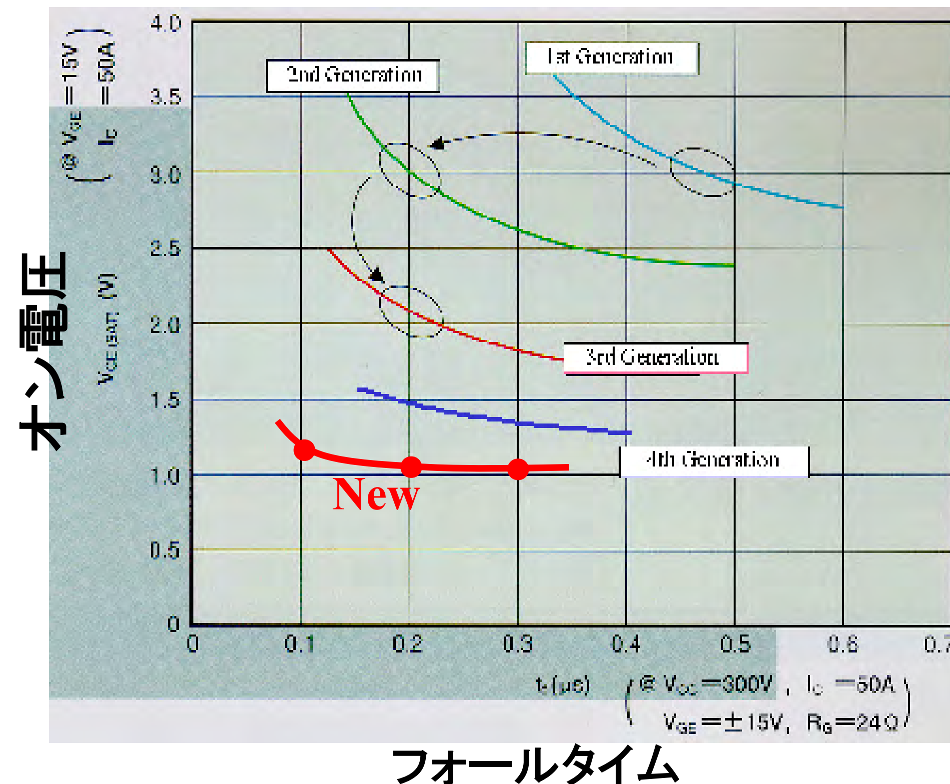
PT-IGBT
高注入Pエミッタ
低ライフタイム

NPT-IGBT
低注入Pエミッタ
高ライフタイム

最新世代IGBT技術 FSIGBT

n-buffer & Low efficiency emitter
Thin wafer technology

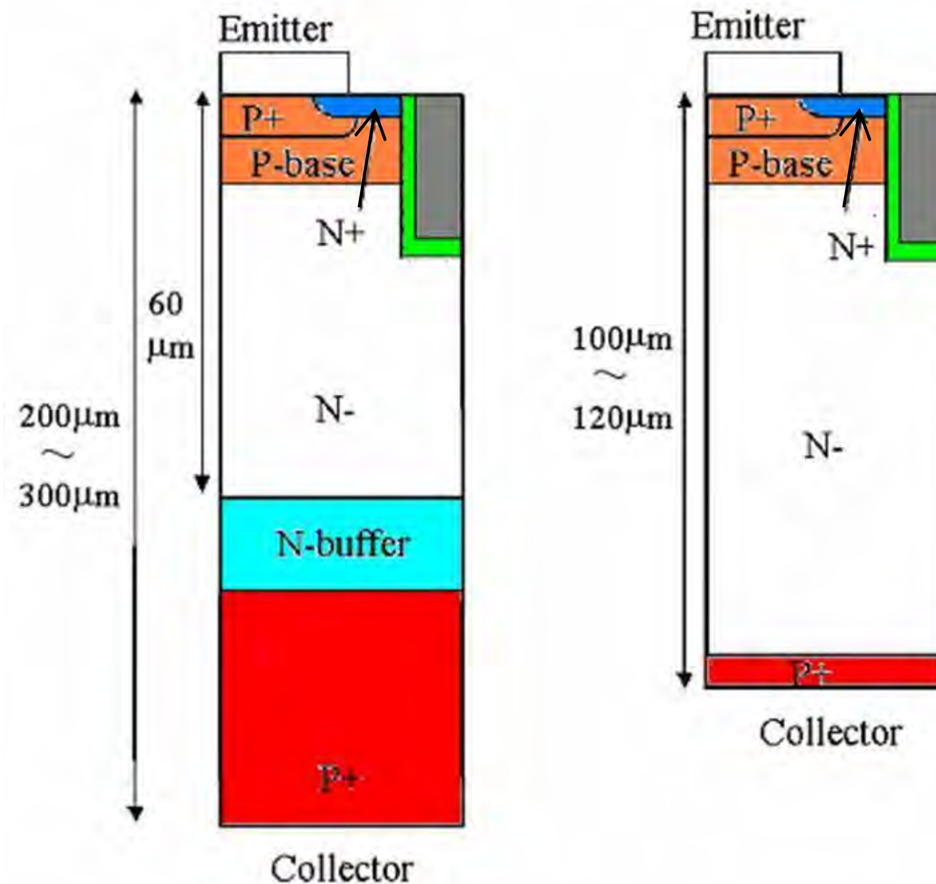




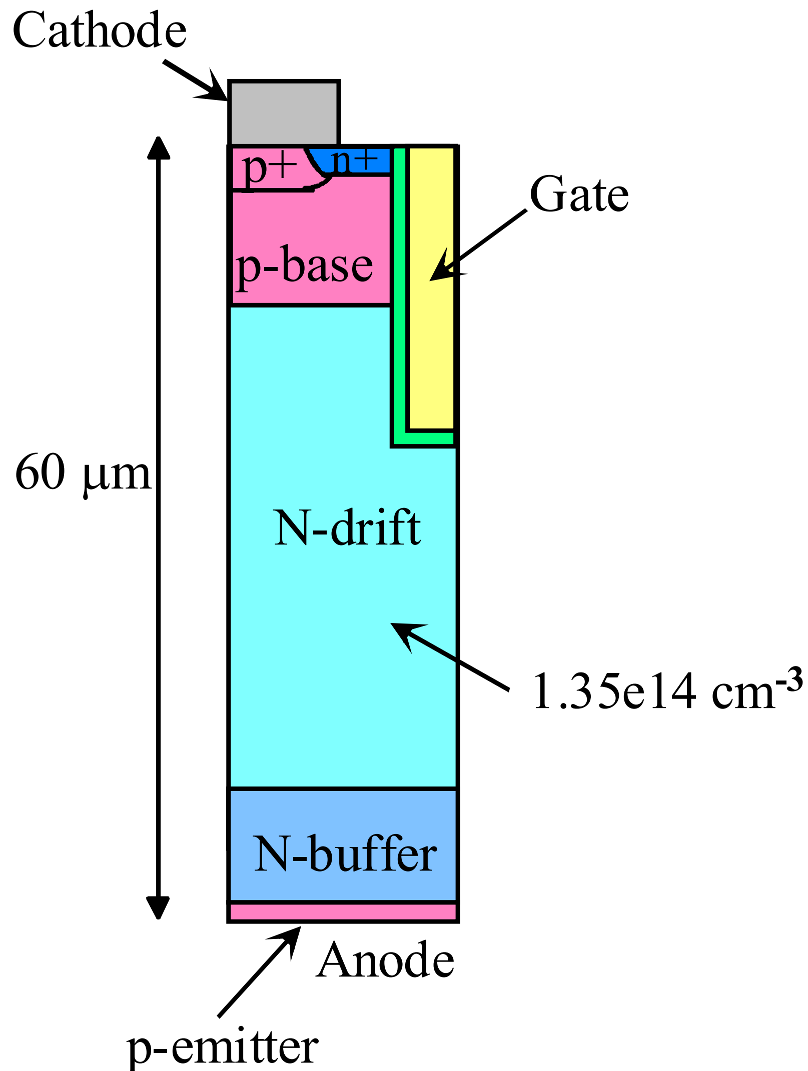
高い目標その3： IGBTで1.0Vのオン電圧@1998年

NPT-IGBT全盛の時：

NPTがPTより良いはずがない!!!
最初のIGBTでPT構造を採用
NPTが良いのはライフタイム制御をやめて低濃度エミッタであるはず!!!
“PT+低注入＋微細加工”で高性能IGBTは可能であろう…と予測!!!

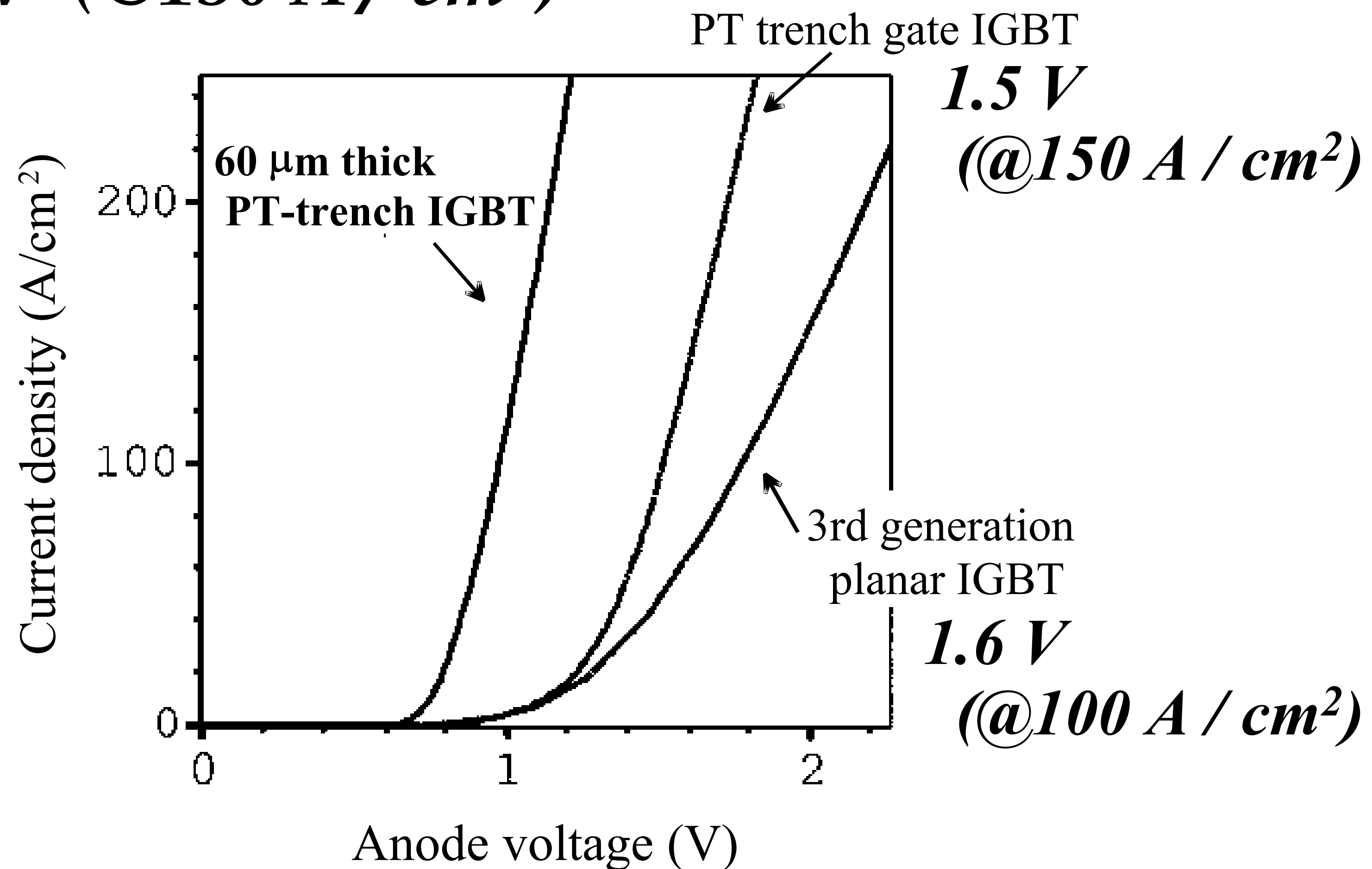


そして、計算した構造の特性が非常に良かった!!! @1998年

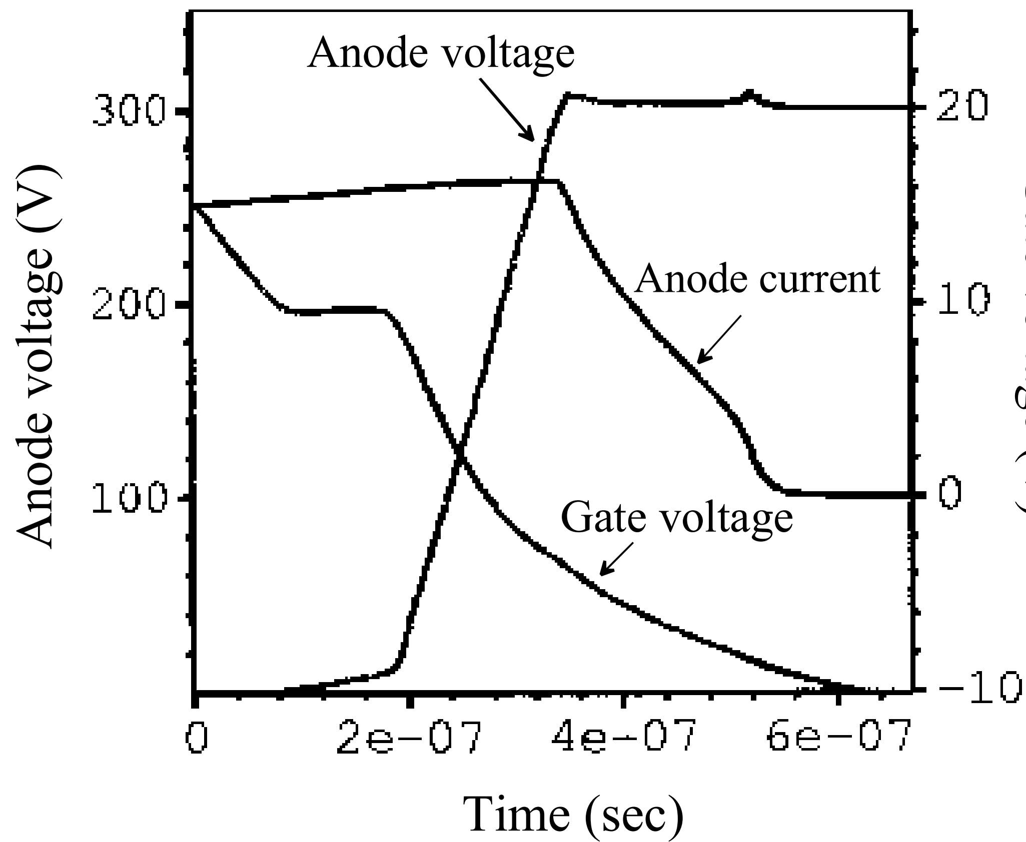


- Total wafer thickness
  - ➔60 µm
- N-buffer layer
  - ➔PT-IGBT
- 低濃度 p-emitter
  - ➔High speed switching
- High carrier lifetime

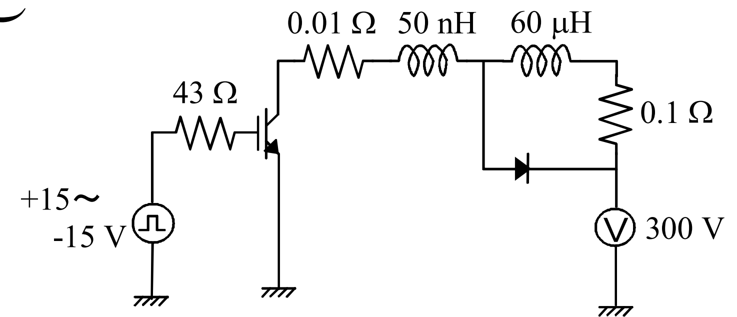
Calculated forward current-voltage characteristics



Turn-off characteristics



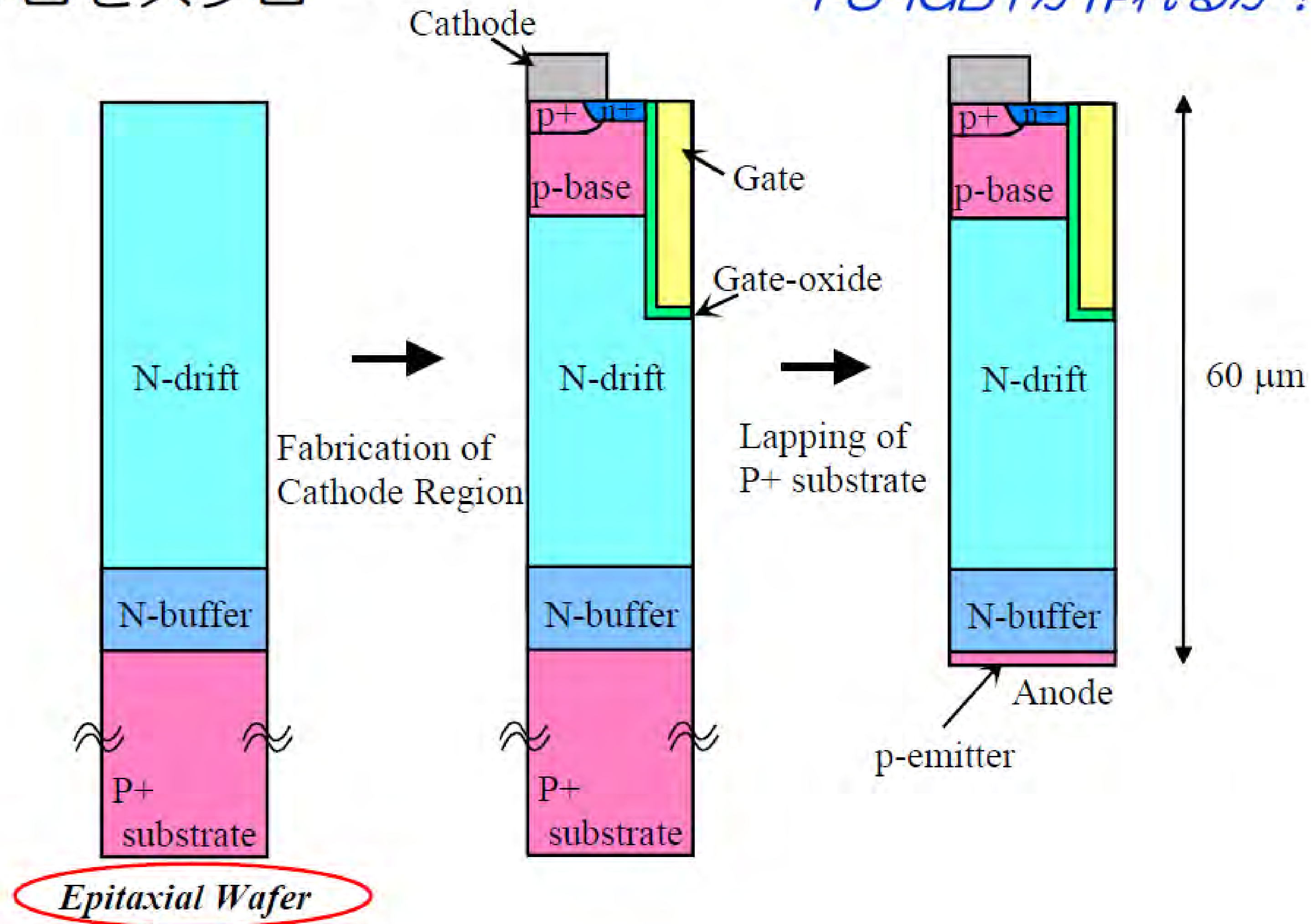
tf = *170 nsec*



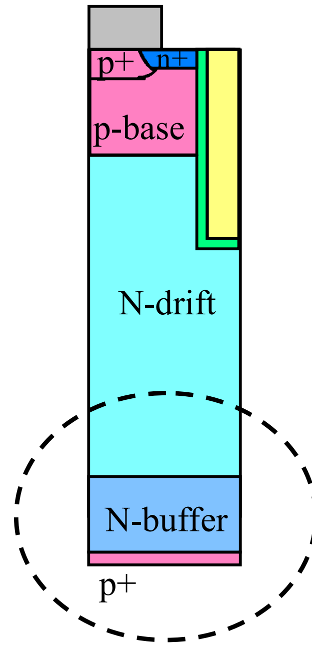
裏面削り残し

プロセスフロー

どうやれば今の自分たちに、FS-IGBTが作れるか？

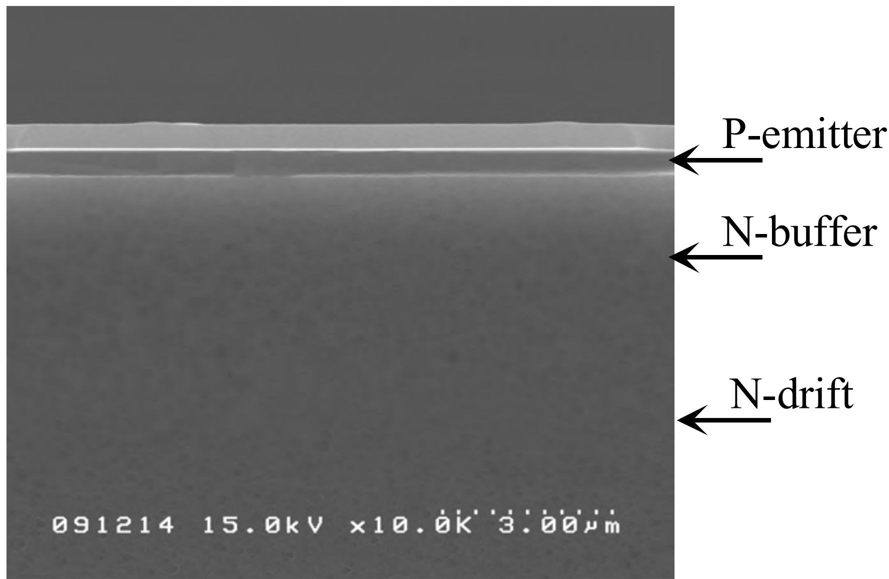


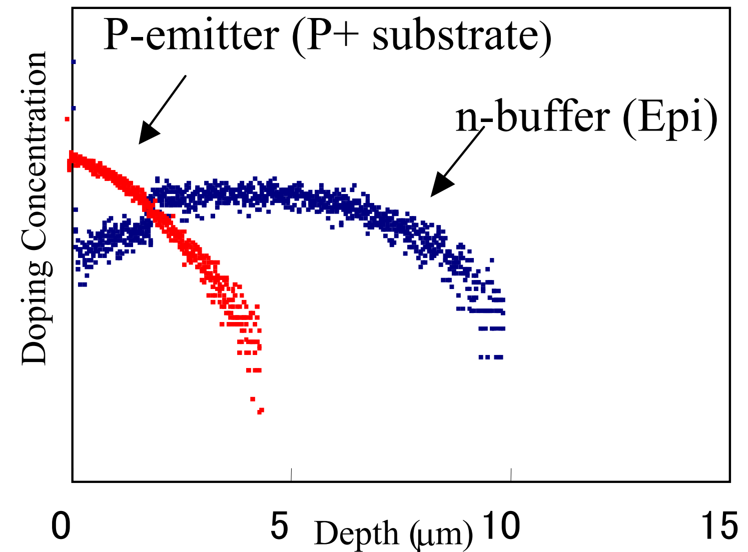
60um厚みの最初のIGBT



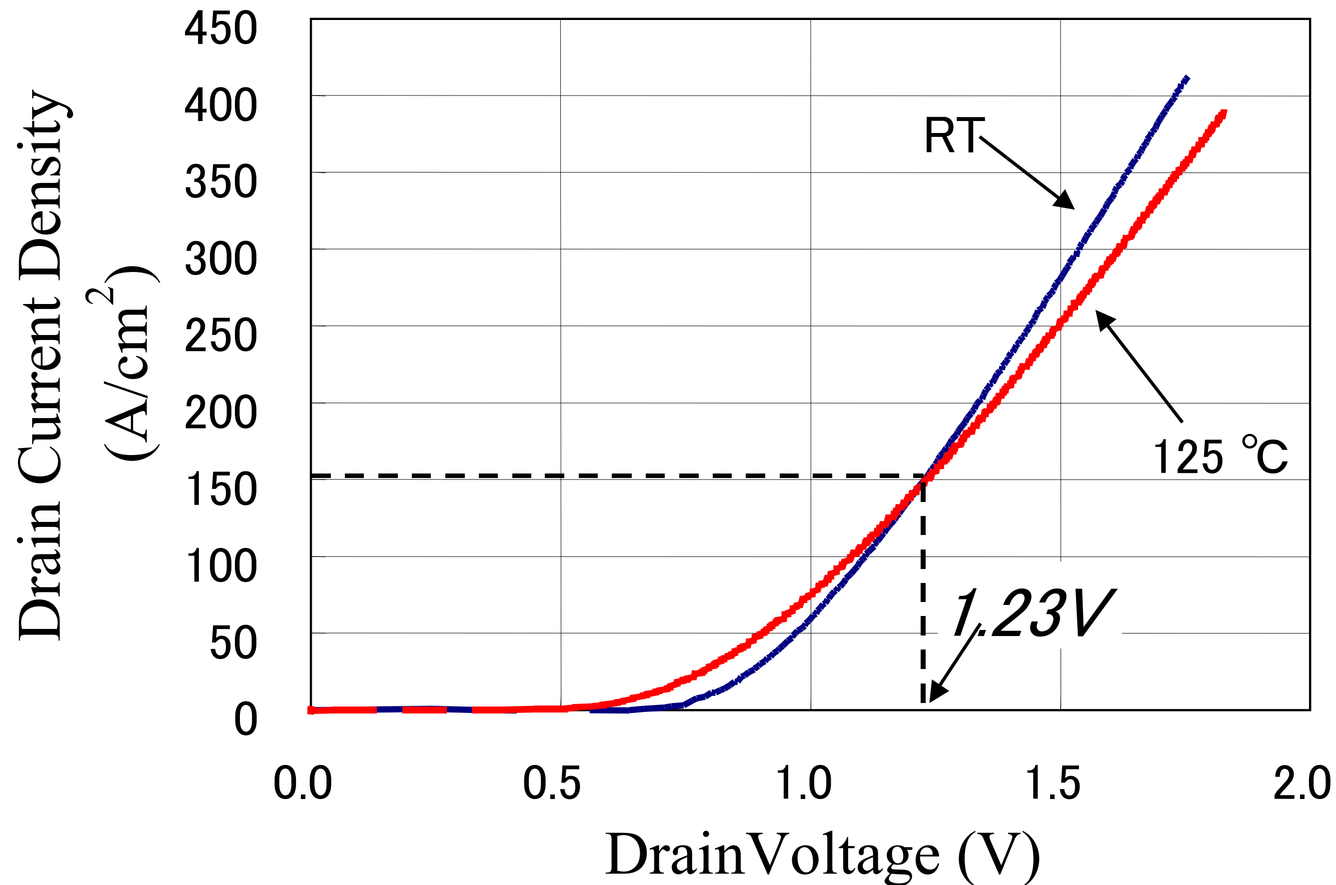
SEM photograph

Impurity distributions



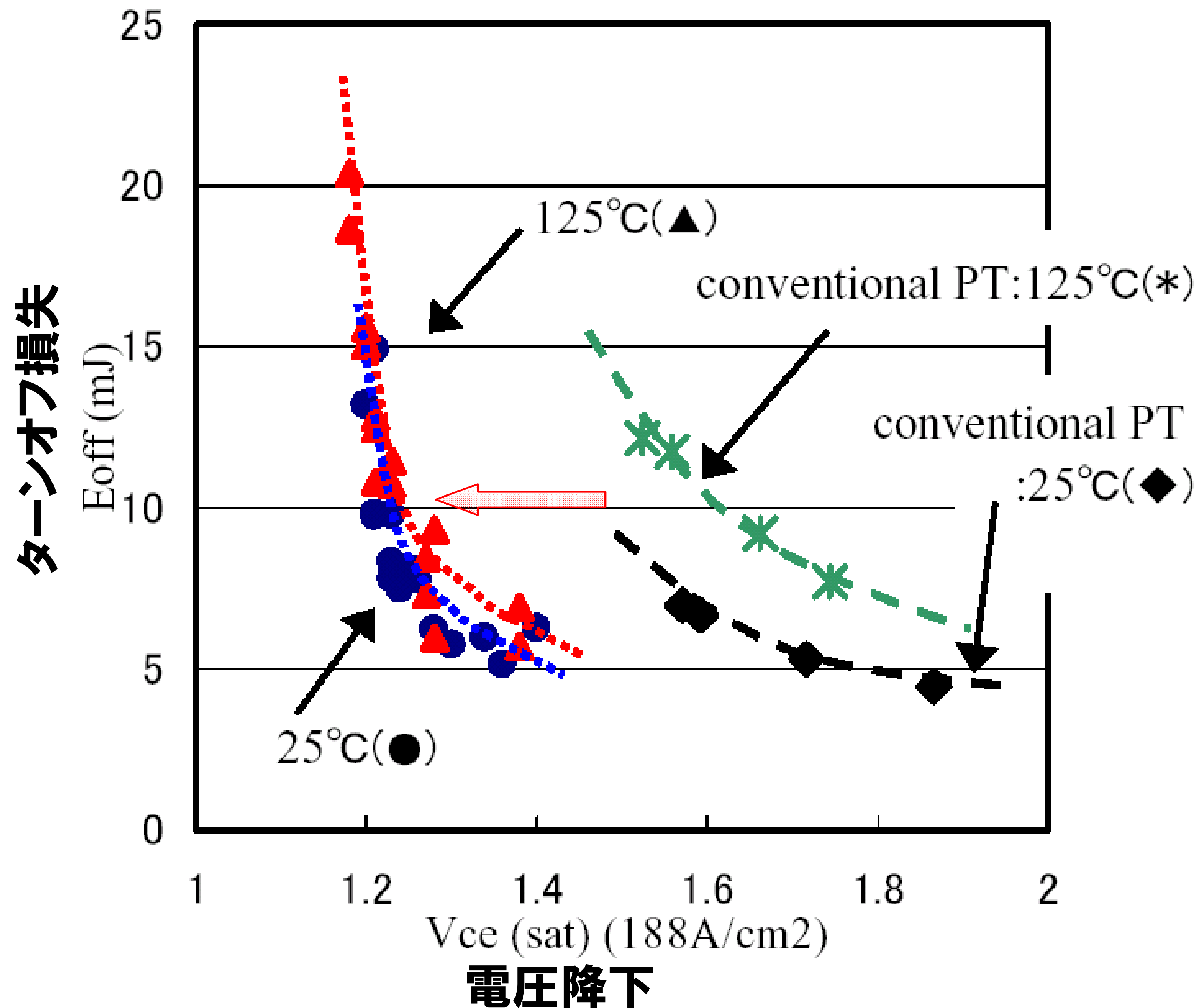


Measured forward current-voltage characteristics



Trade-Off 特性

ISPSD2001



IGBTのウェハ厚み

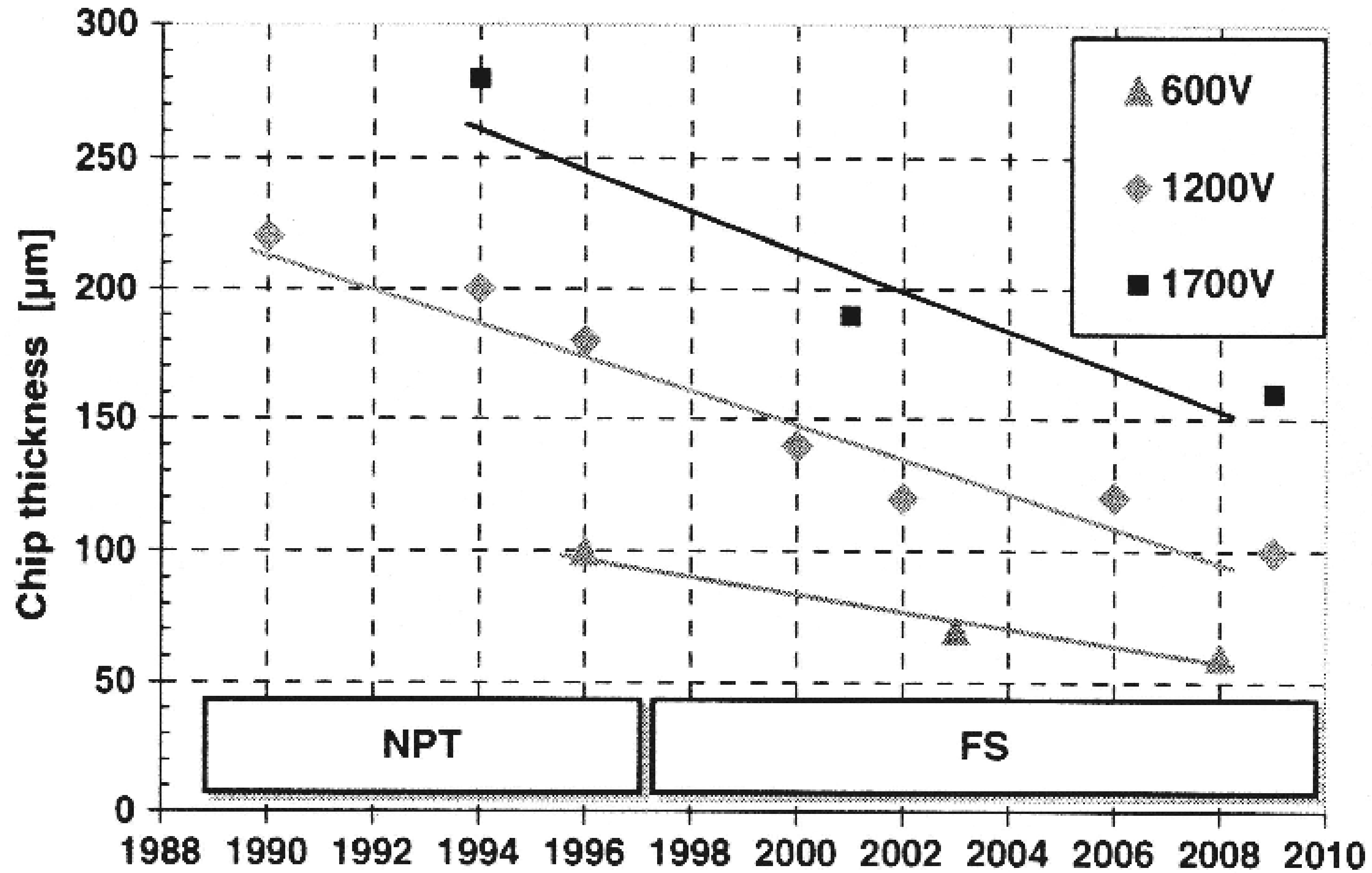


Fig. 12.38 Device thickness for different IGBT generations of the manufacturer Infineon.

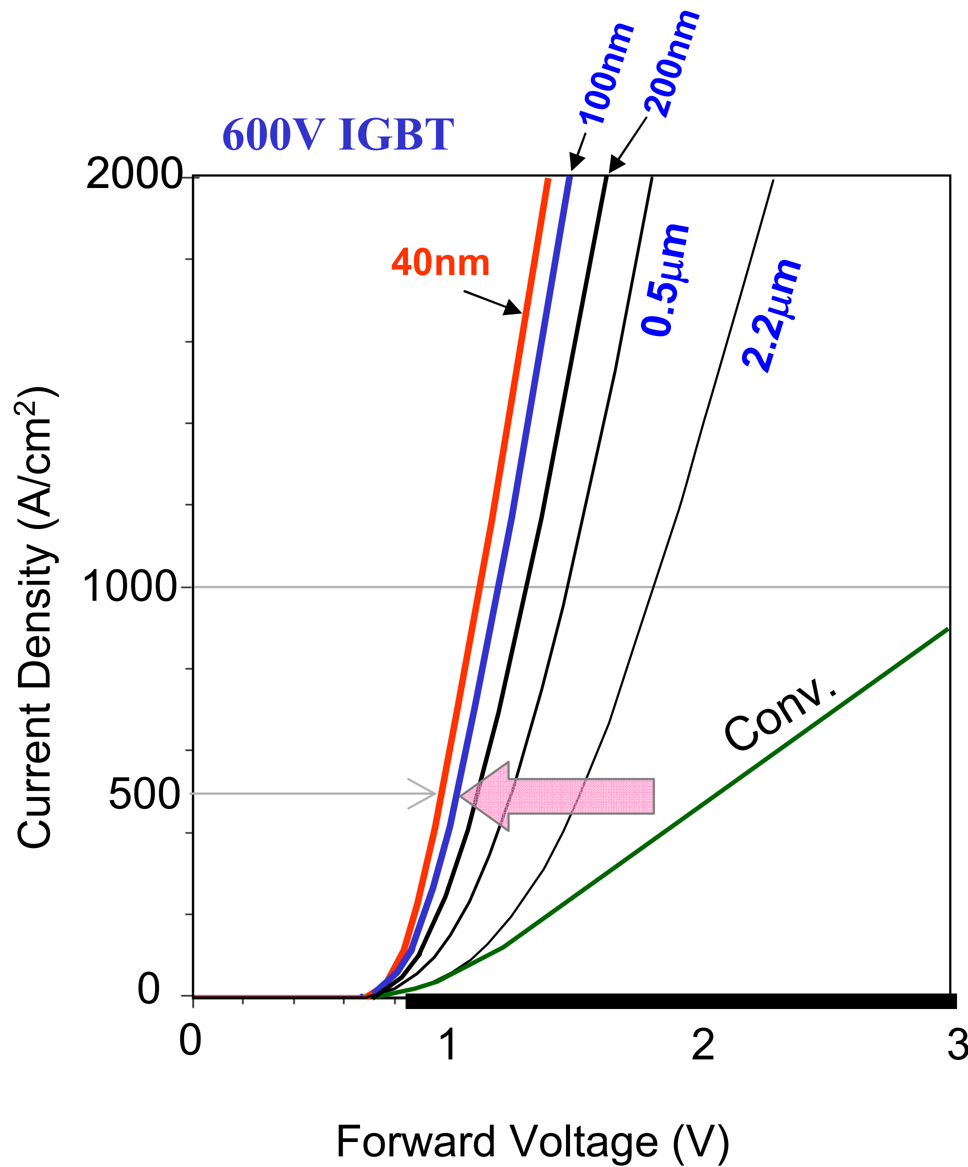
出所: Lutz, Semiconductor Power Devices Springer

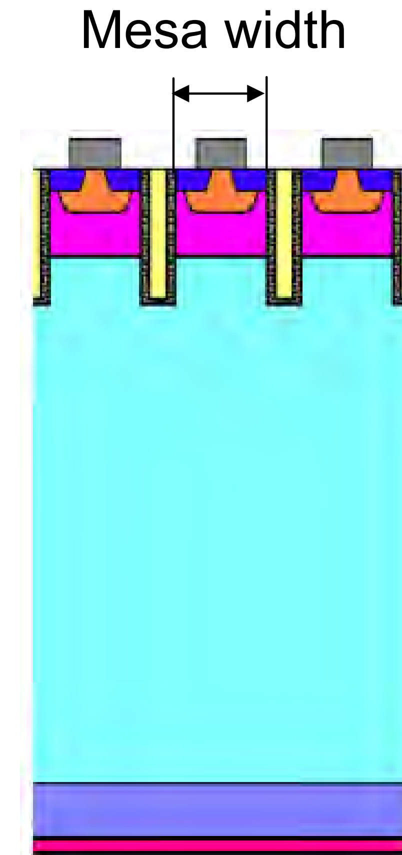
目次

１．序
２．電気に依存する社会
３．パワーエレクトロニクス
４．パワーデバイスの市場
５．IGBTとその発展の経緯
<u>６．IGBTのシリコン限界に向けた今後の展開</u>
７．パワーMOSFETの発展の経緯と今後の可能性
８．新材料デバイス
９．製造プロセス
10．まとめ

IGBTのシリコン限界

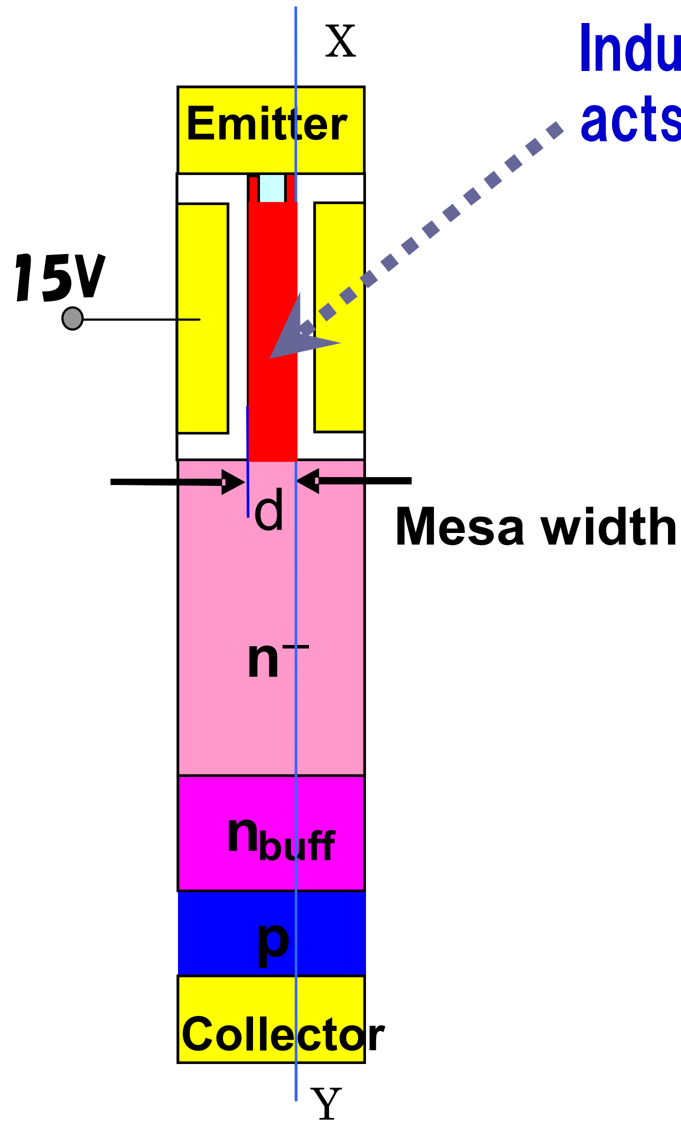
Forward voltage can be greatly improved by reducing mesa width.

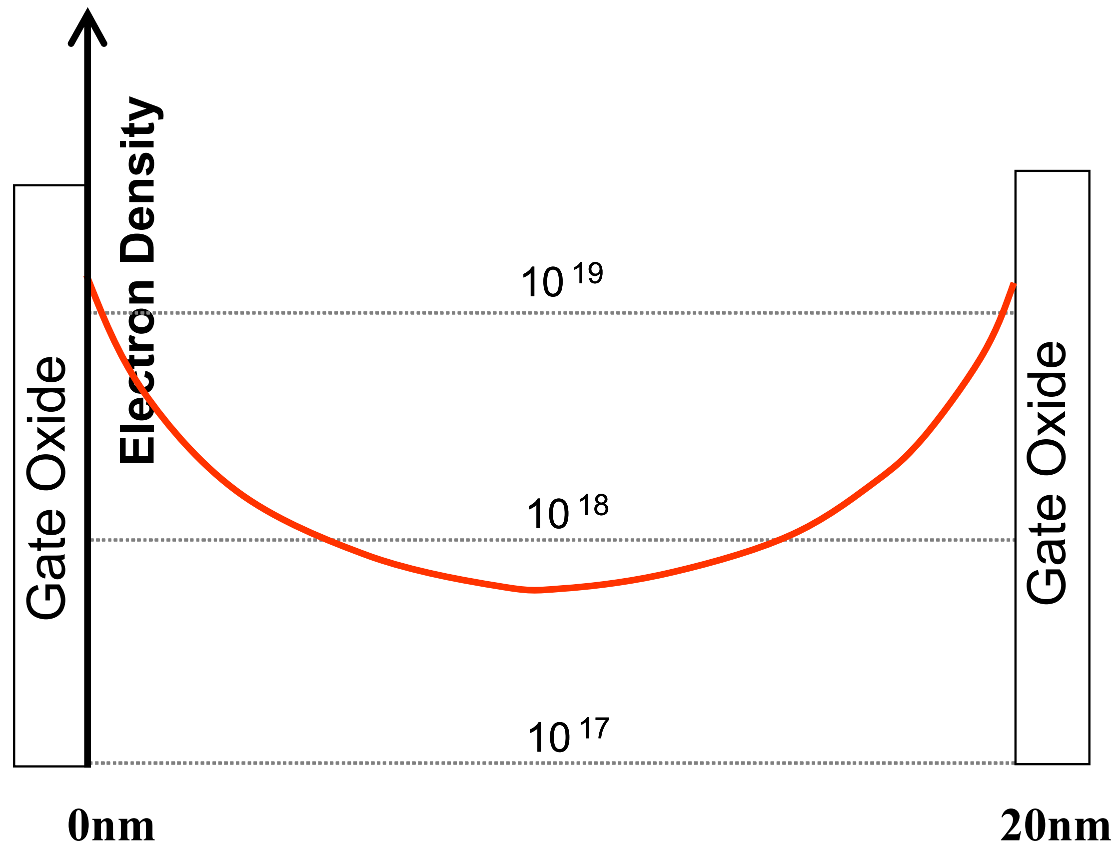




Very Narrow Mesa IGBT

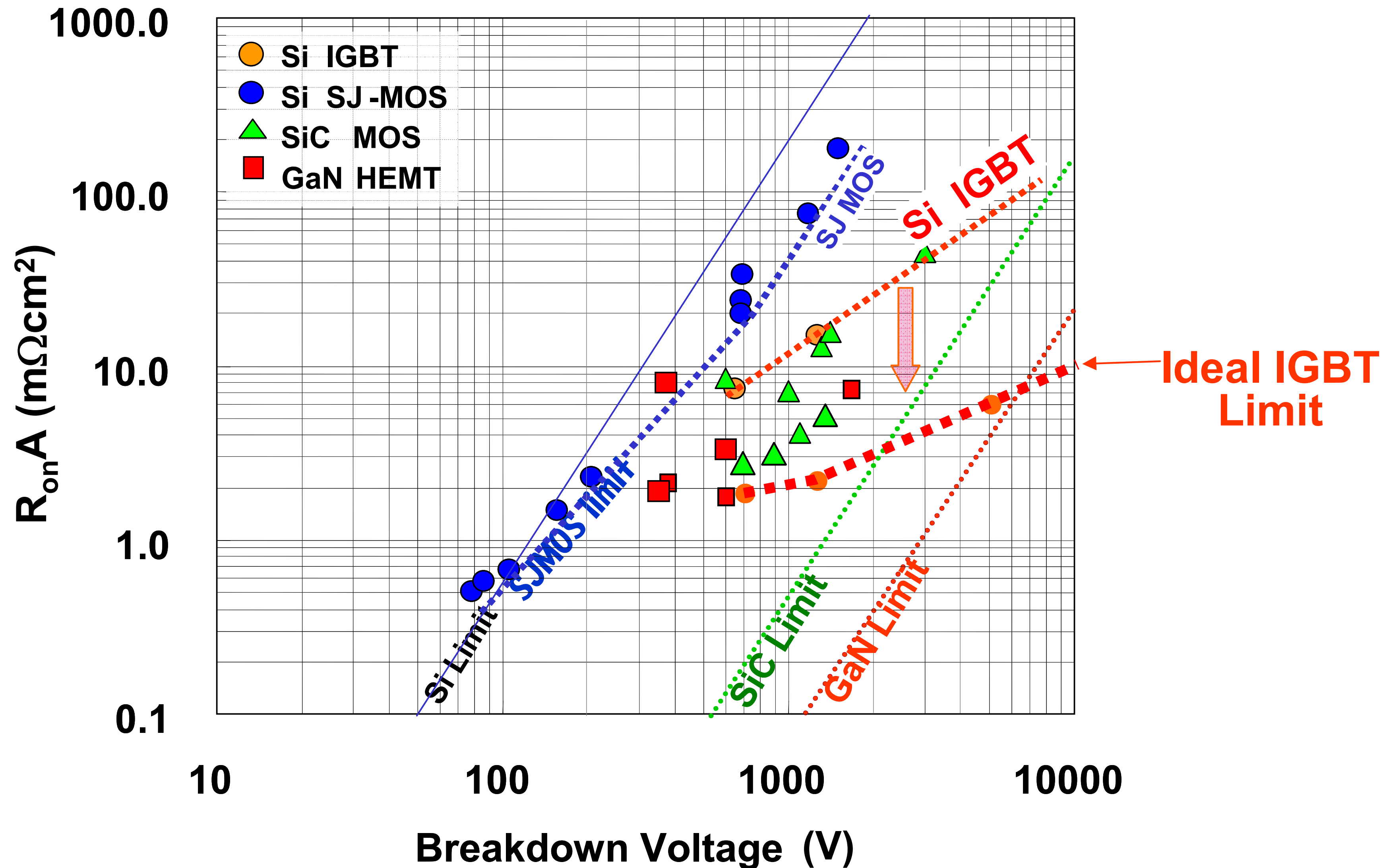
Induced inversion layer
acts as N barrier for holes
→ high injection efficiency > 0.9



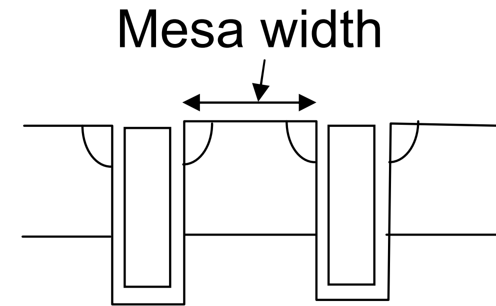


Theoretical limit of IGBT

IGBTs can still be greatly improved in future



Silicon Limit Analysis based on TCAD for 1200V IGBT



1200V IGBT

Mesa width (μm)	$I_{Saturation}$ = 800A/cm² (V)	Large I_{Sat} case (V)
0.05		0.9
0.1		0.93
0.2	1.15	1.07
0.6	1.4	1.36

Conditions:

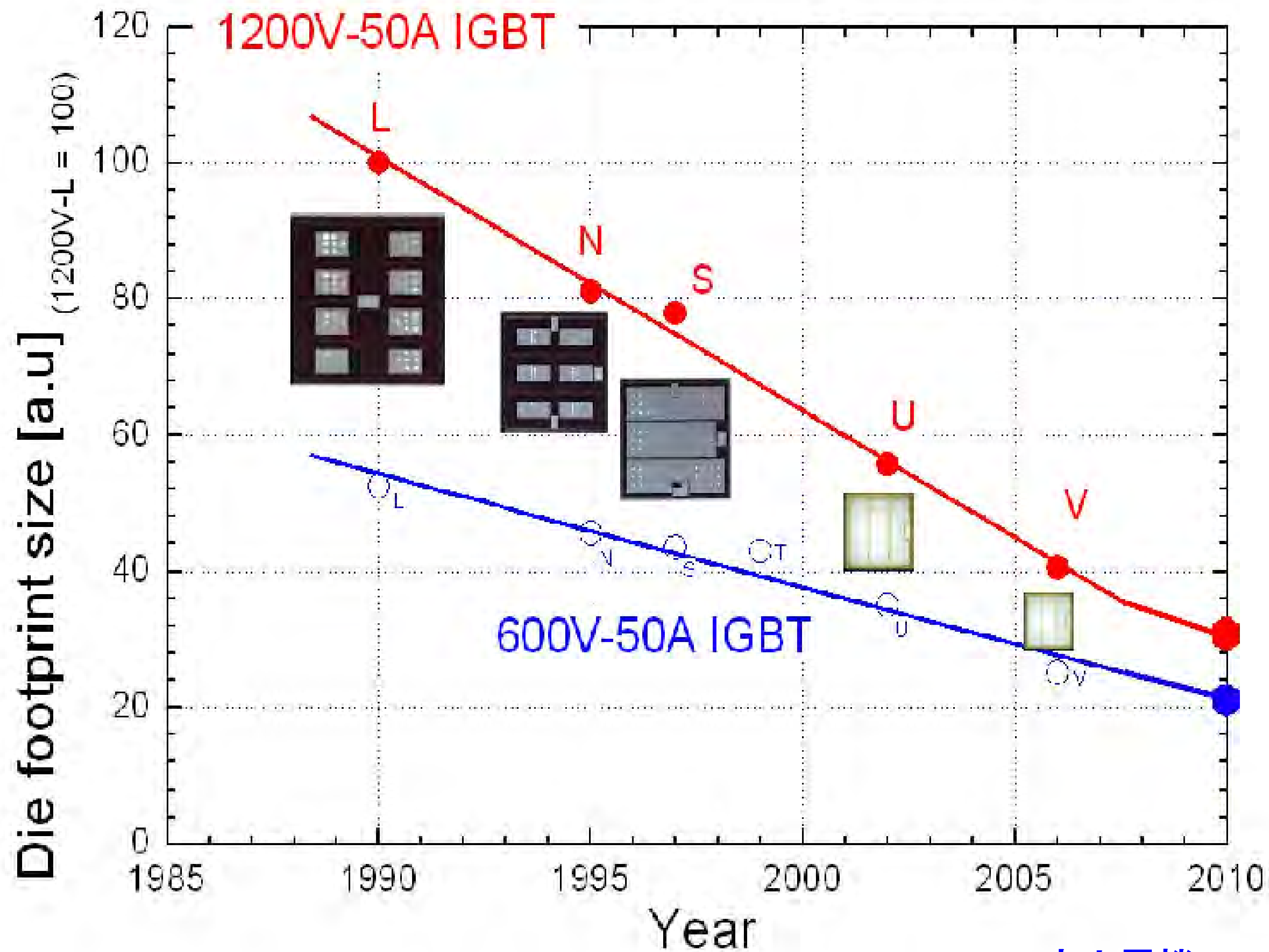
Si thickness=100μm

Current density= 150A/cm2

Temp.=150C

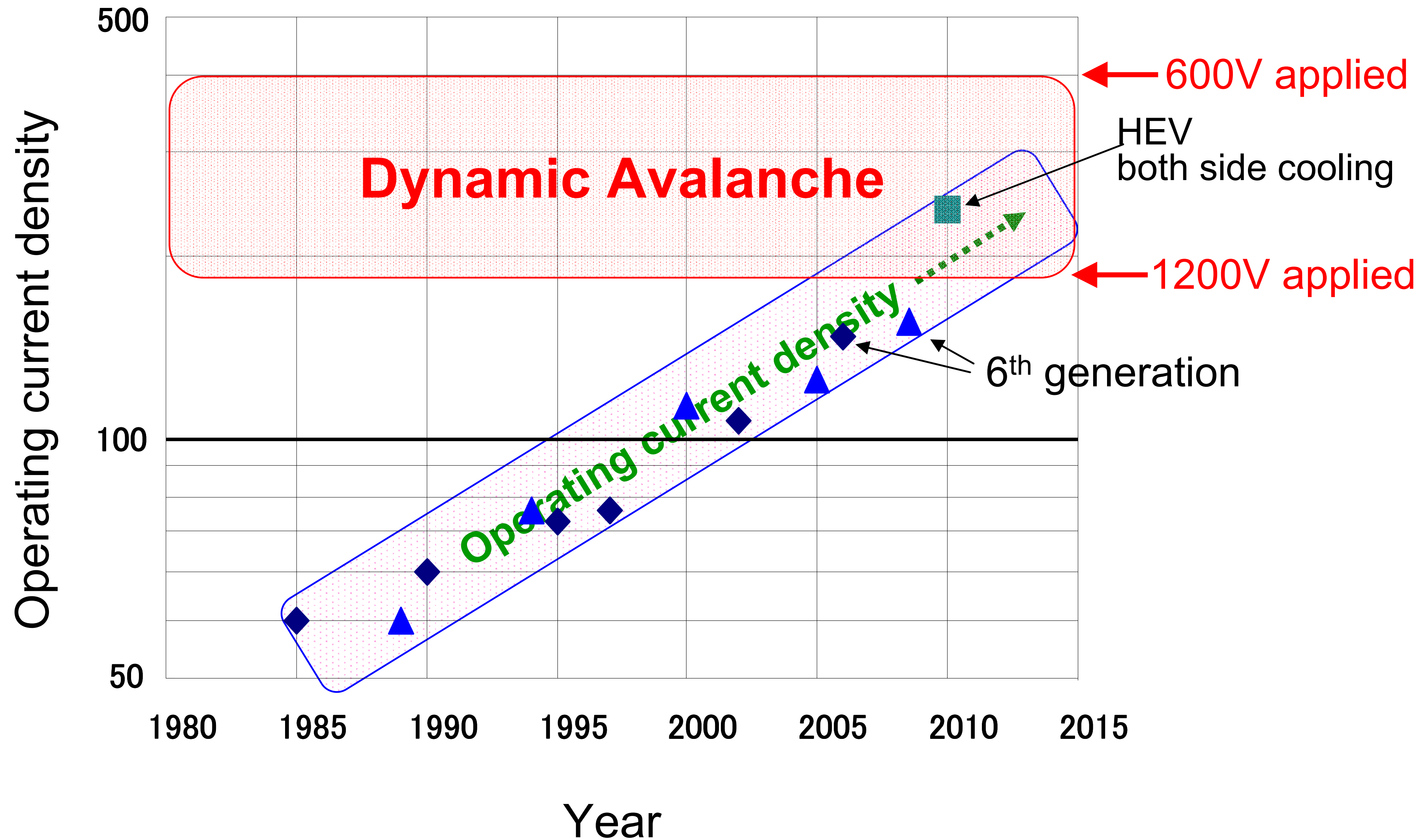
Turn-off loss is fixed at 120μJ/A

IGBT Chip footprint as a function of year



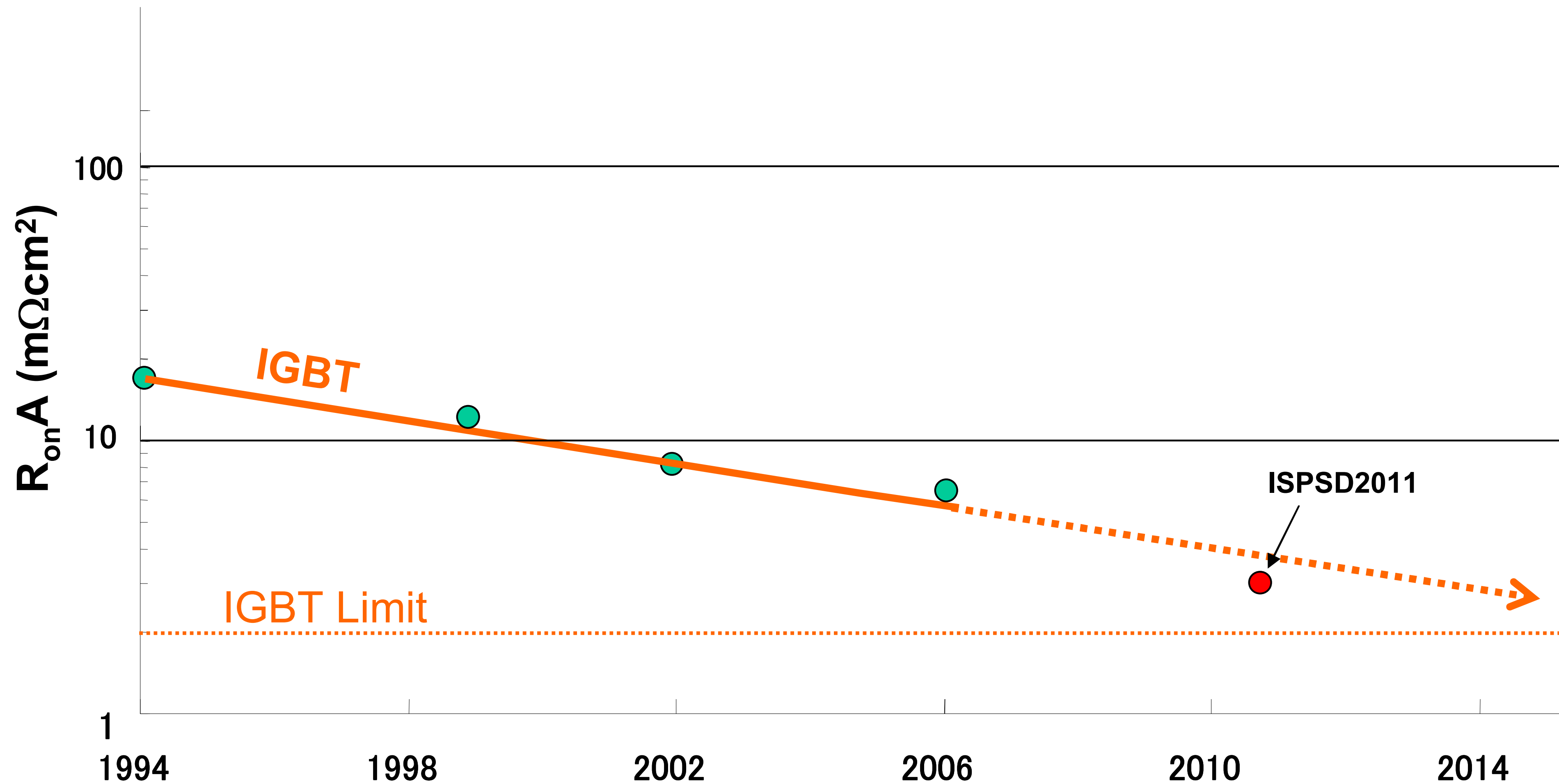
富士電機

1200V IGBT operating current density



Trends of 600V IGBT

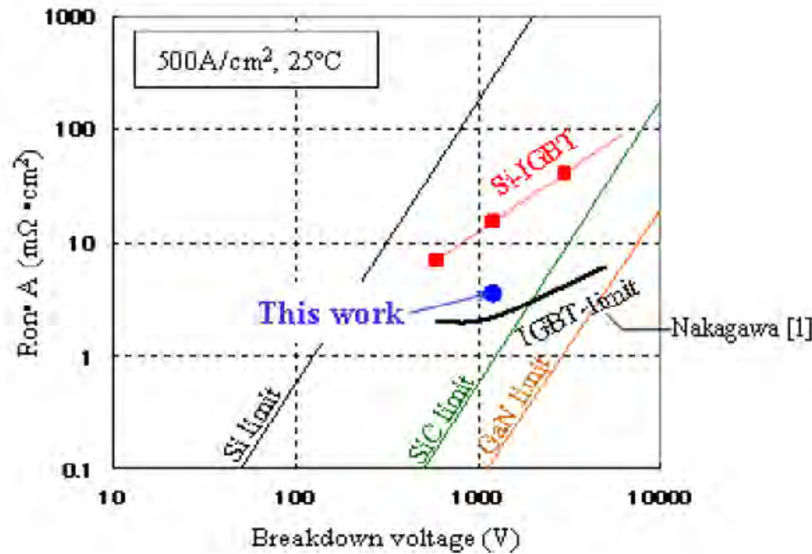
IGBT On-resistance has been steadily improved In the past,
It is predicted that it will approach the IGBT limit in near future.

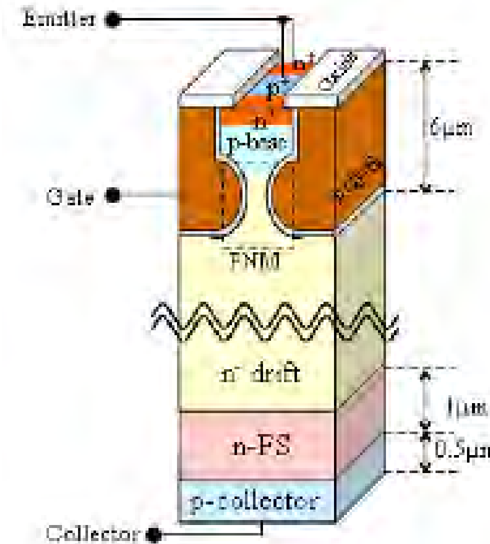


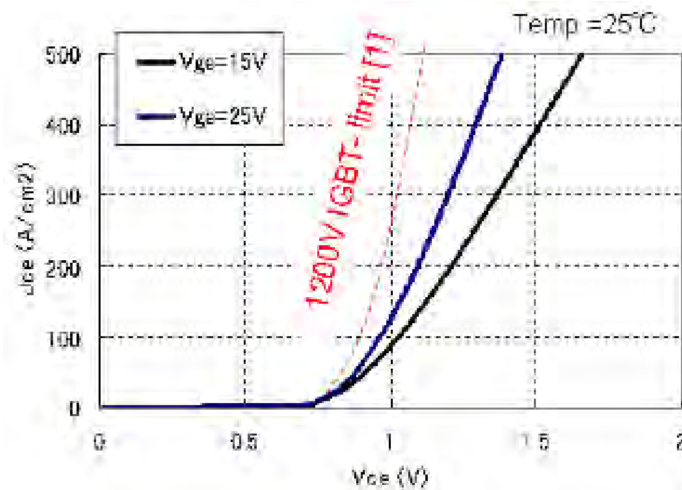
Low loss IGBT with Partially Narrow Mesa Structure (PNM-IGBT)

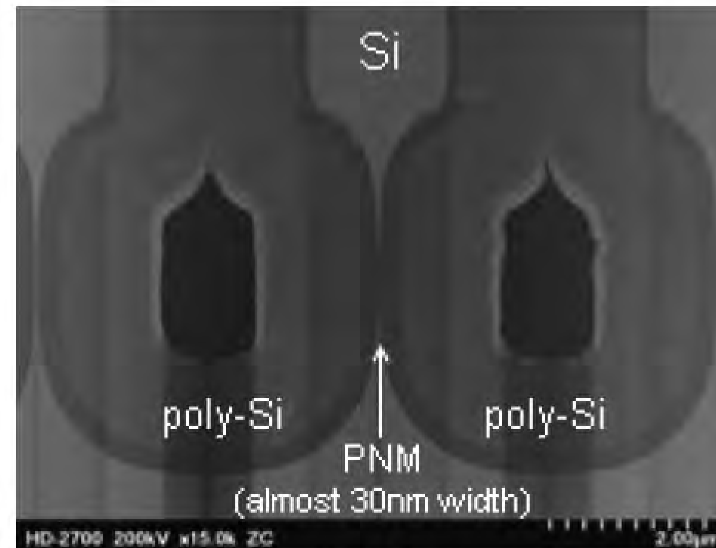
ISPSD' 12

Masakiyo Sumitomo, Junichi Asai, Hiroki Sakane, Kazuki Arakawa, Yasushi Higuchi and Masaki Matsui
DENSO CORPORATION
Research Laboratories
Nisshin, Aichi, 470-0111, Japan
masakiyo_sumitomo@denso.co.jp







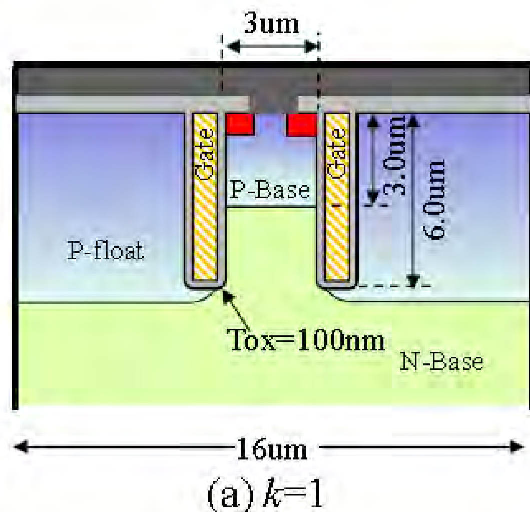


Cross-Sectional TEM image of the prototype

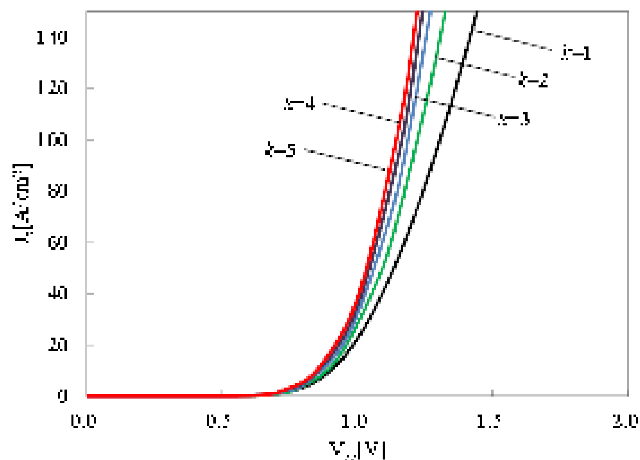
Scaling Rule for Very Shallow Trench IGBT toward CMOS Process Compatibility

ISPSD' 12

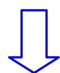
Masahiro Tanaka and Ichiro Omura
Kyushu Institute of Technology

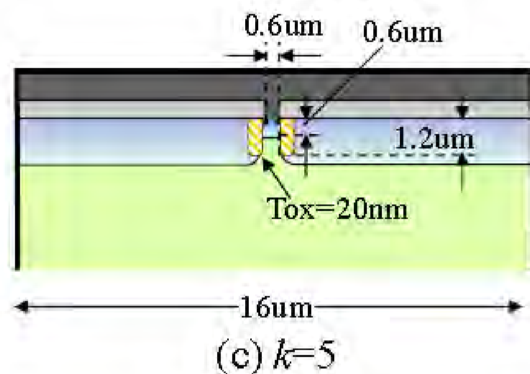


(a) k=1

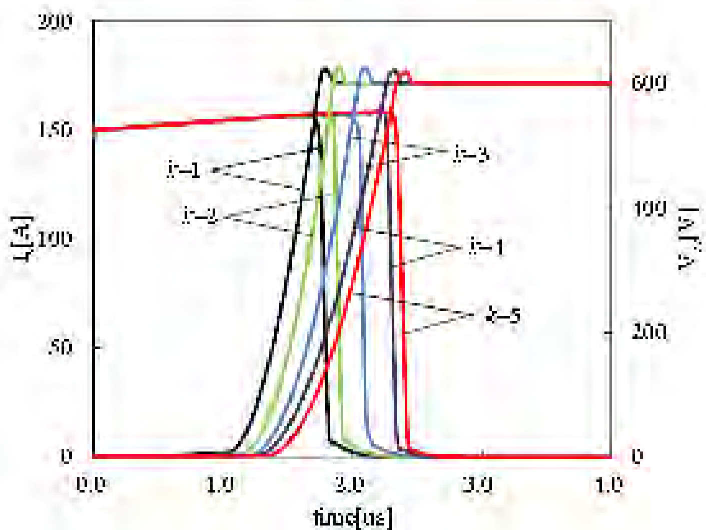


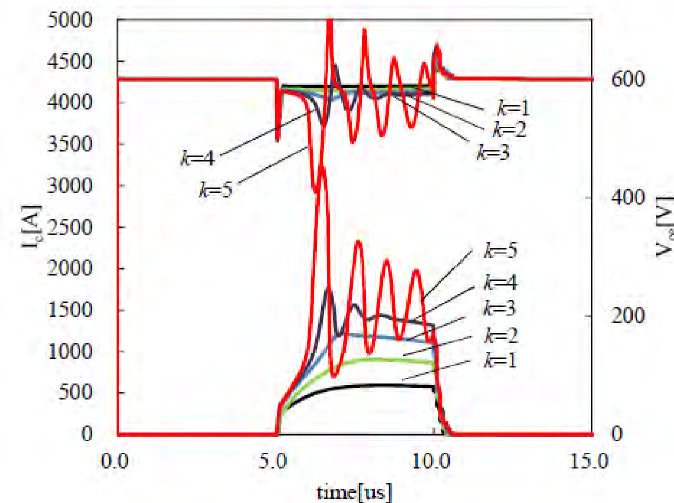
浅いトレンチゲートでも良好な特性。
CMOS Fab.で IGBT生産可能





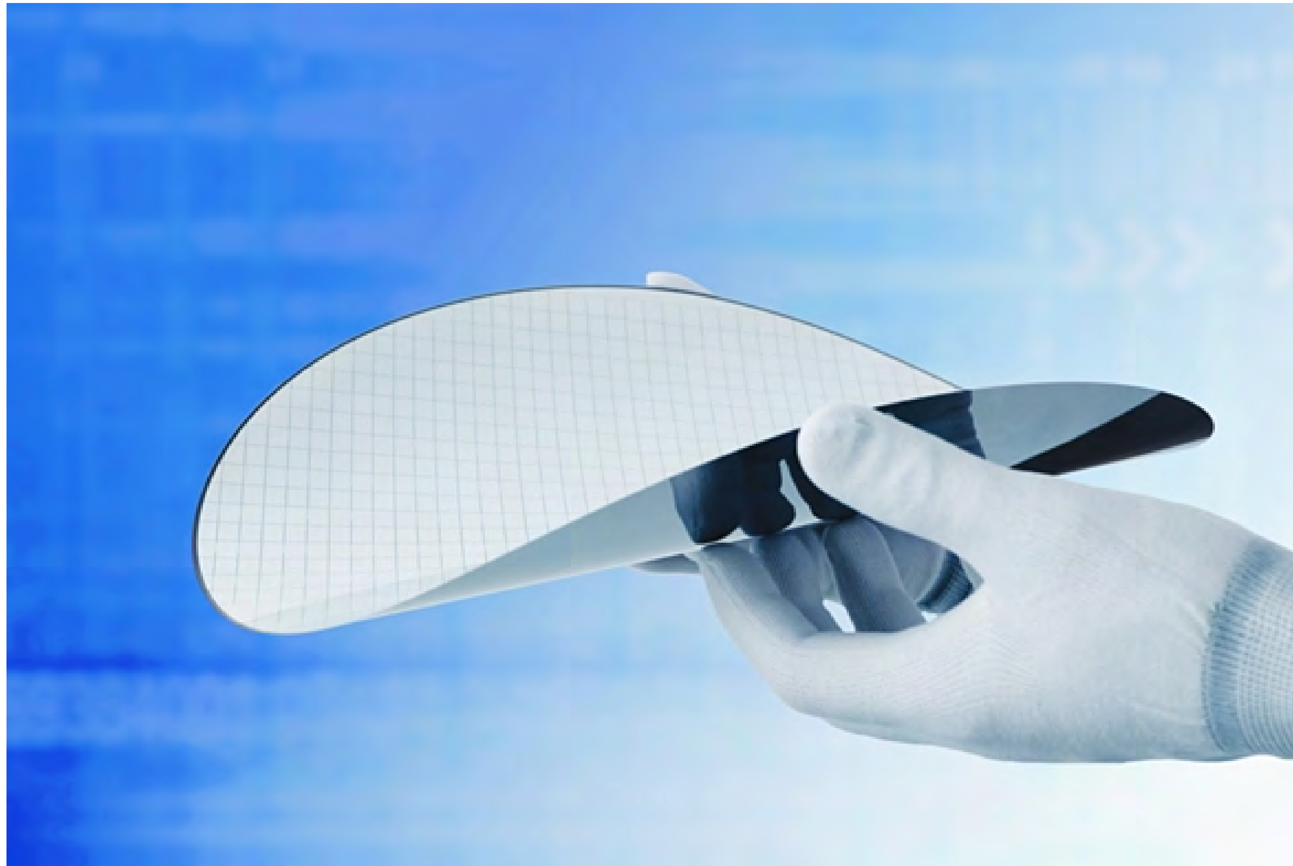
(c) k=5





30cm CMOS Fab for Power Devices

contributes to better performance and low cost.



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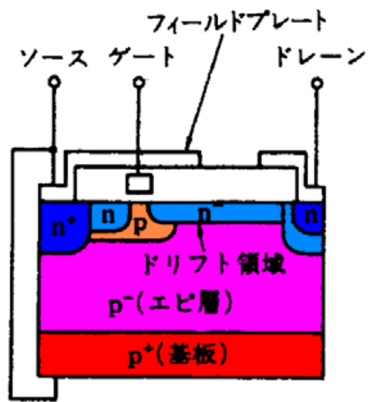
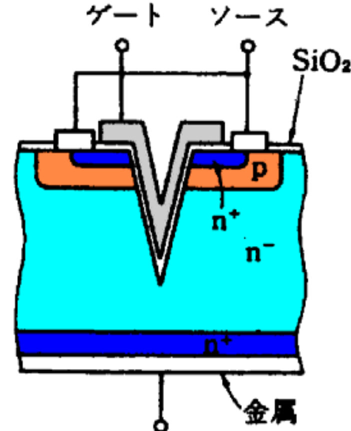
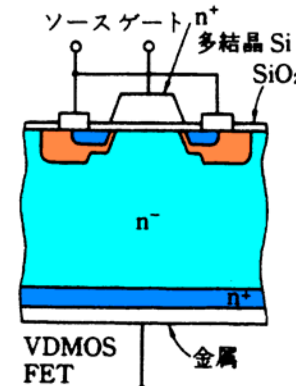
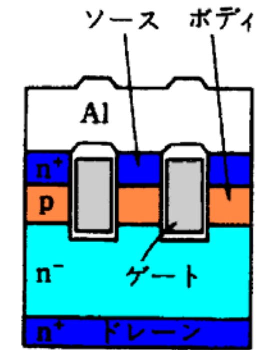
２．電気に依存する社会
３．パワーエレクトロニクス
４．パワーデバイスの市場
５．IGBTとその発展の経緯
６．IGBTのシリコン限界に向けた今後の展開
７．パワーMOSFETの発展の経緯と今後の可能性
８．新材料デバイス
９．製造プロセス
10．まとめ

MOSFET基本技術の歴史



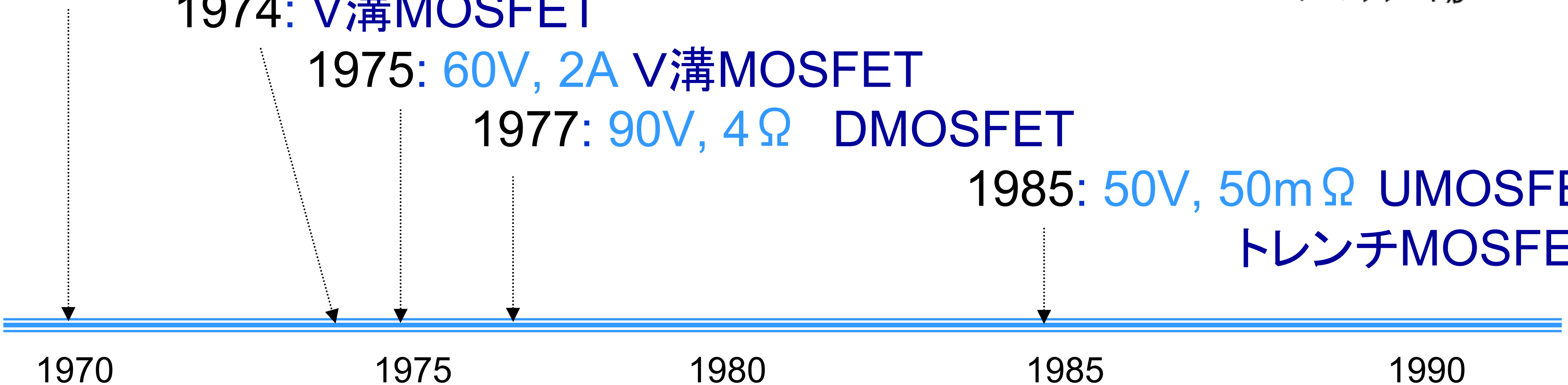






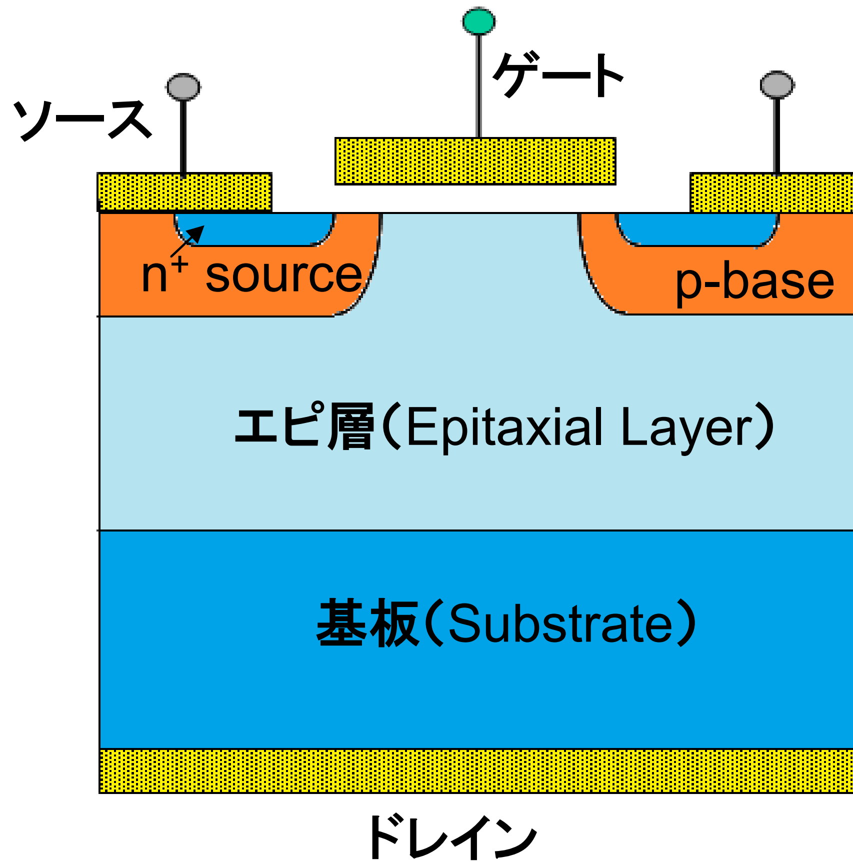
1970: DSA技術（DMOS技術）

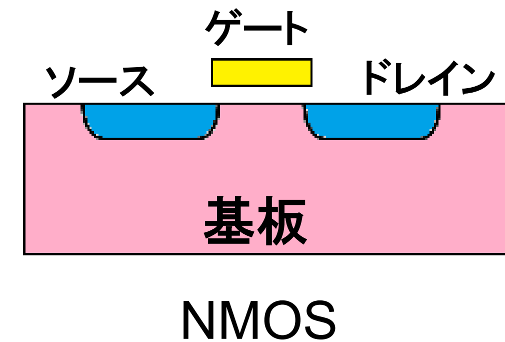
1970: 100V, 1A　オフセットゲートMOSFET



縦型パワーMOSFETの基本構造

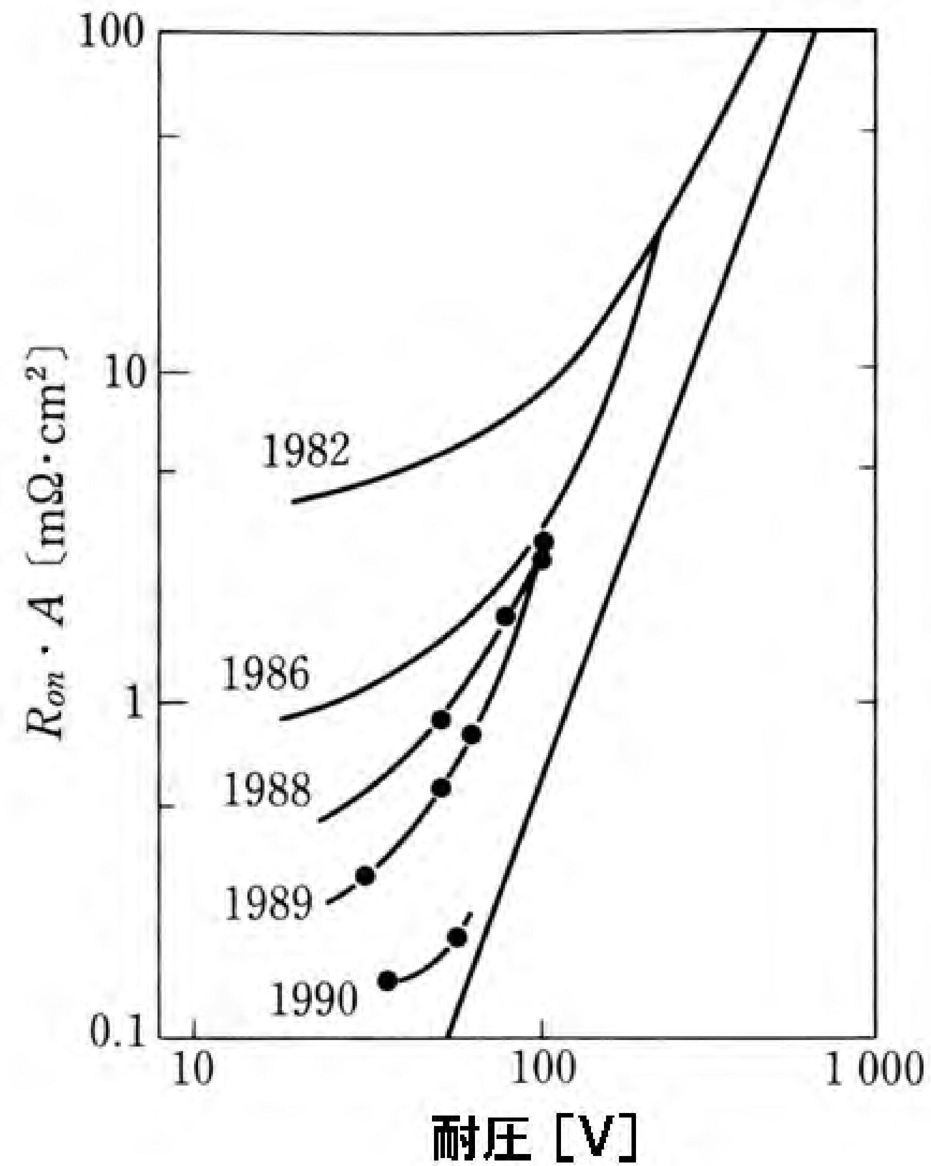
DMOSFET（Double Diffusion MOSFET）



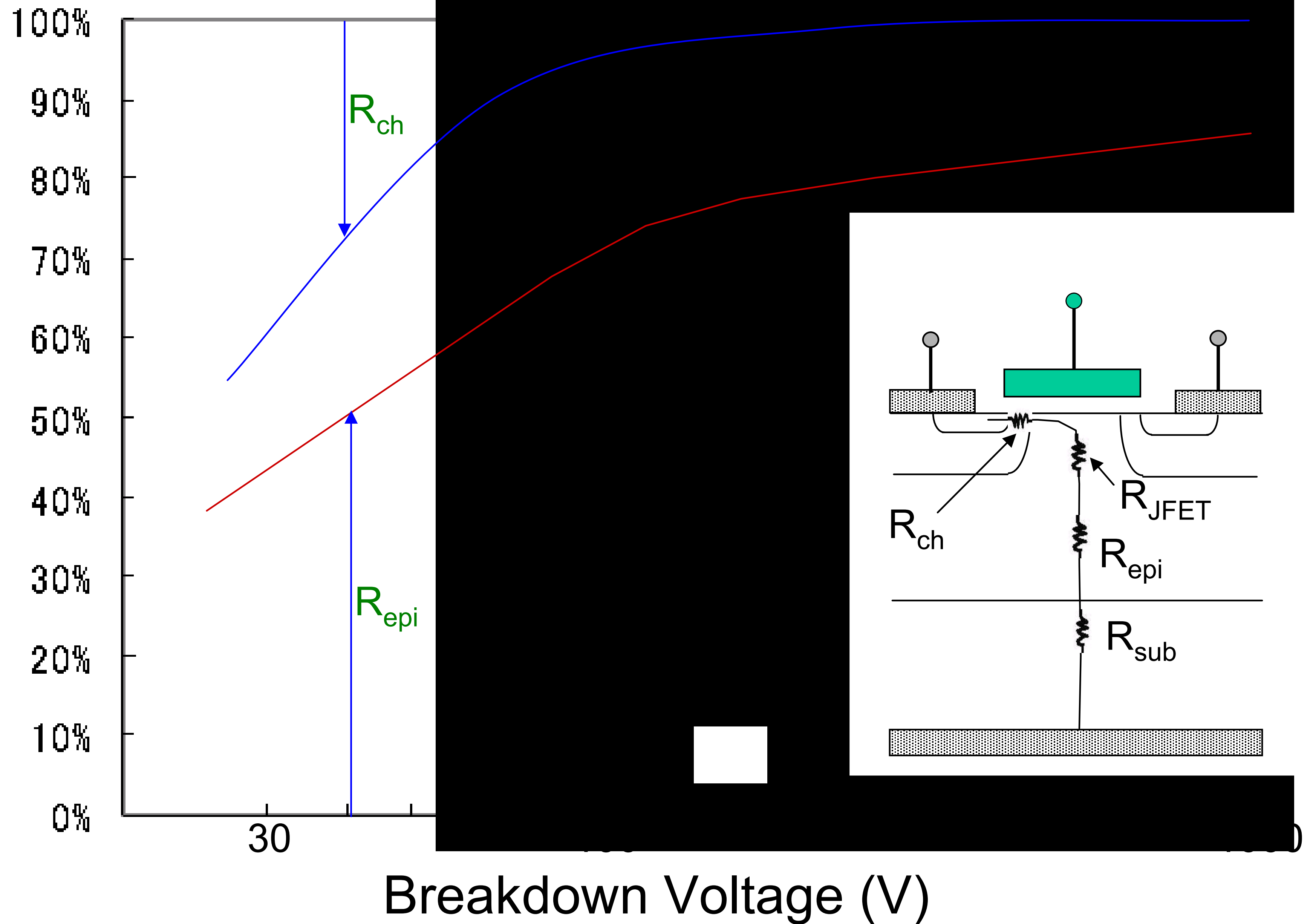


NMOS

シリコンMOSFETのオン抵抗の低減の歴史

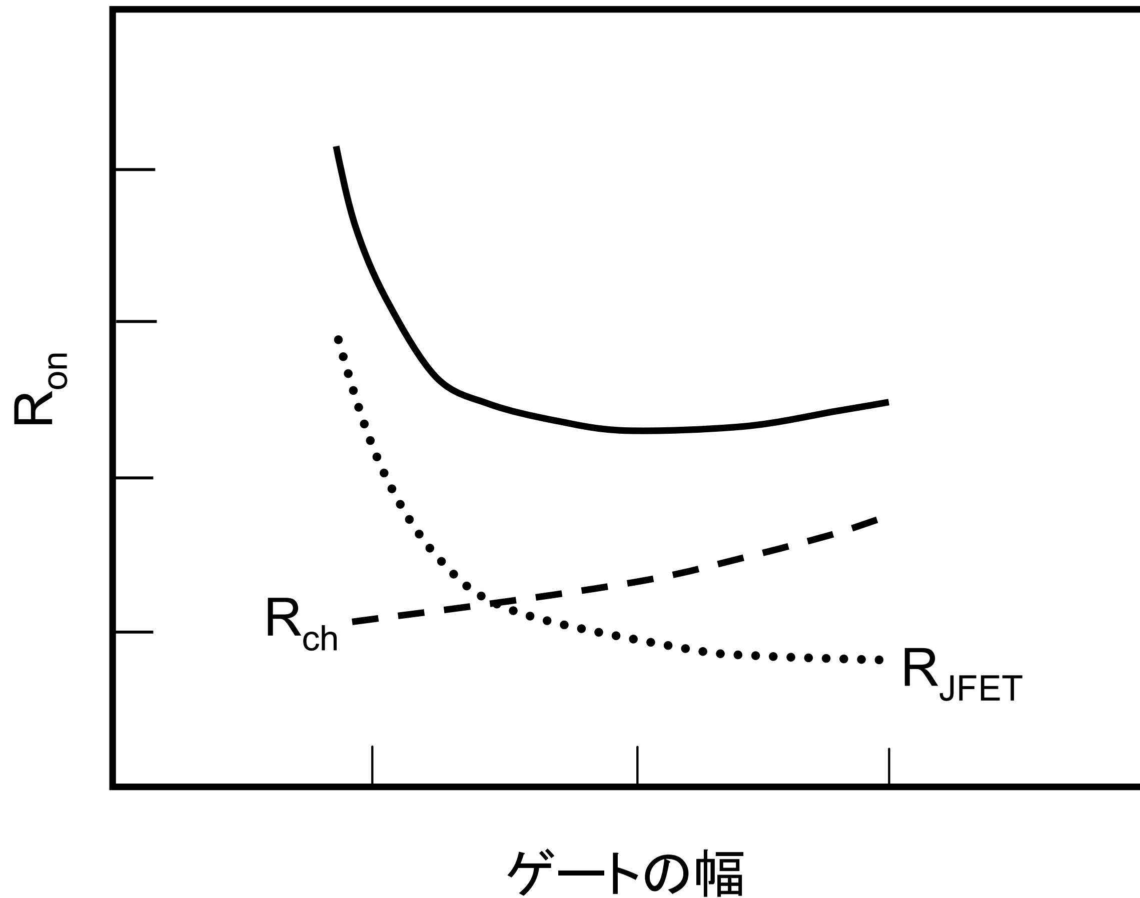


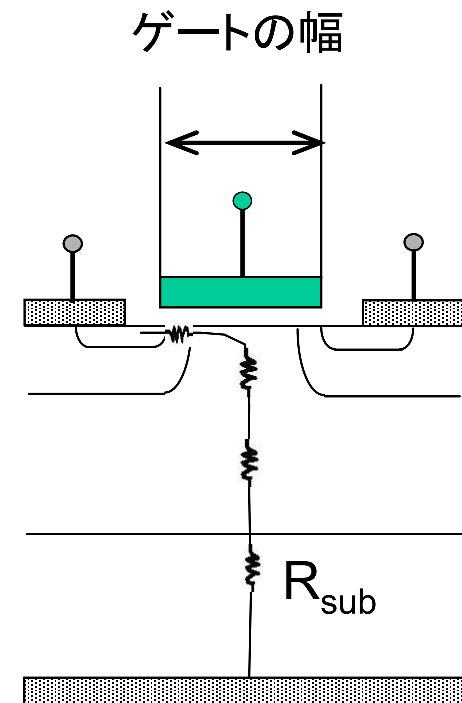
チャネル抵抗の占める割合



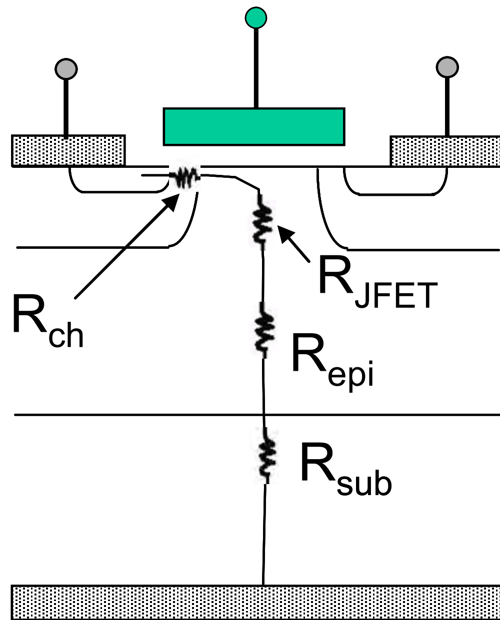
プレーナMOS：微細化によるオン抵抗低減の限界

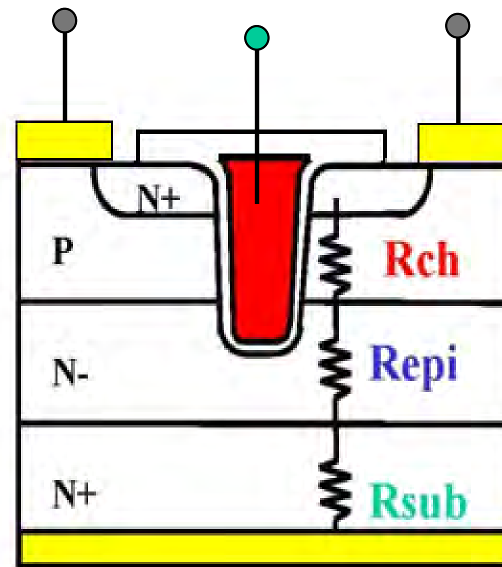
ポリシリコン幅とオン抵抗





トレンチゲートの利点





DRAM

4Gb

1G

256M

64M

16M

4M

1Mb

120Mcells/inch^3

Planar Vertical DMOS

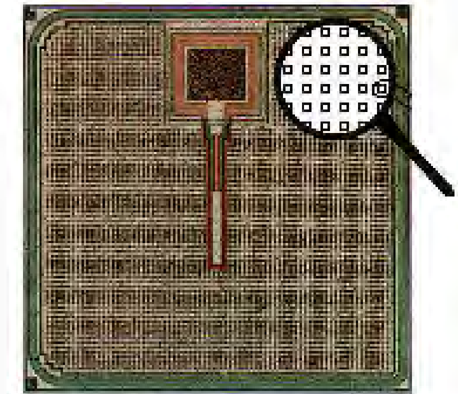
Trench Gate Vertical DMOS

# of transistors

10000
1000
100
10
1
0.1
0.01

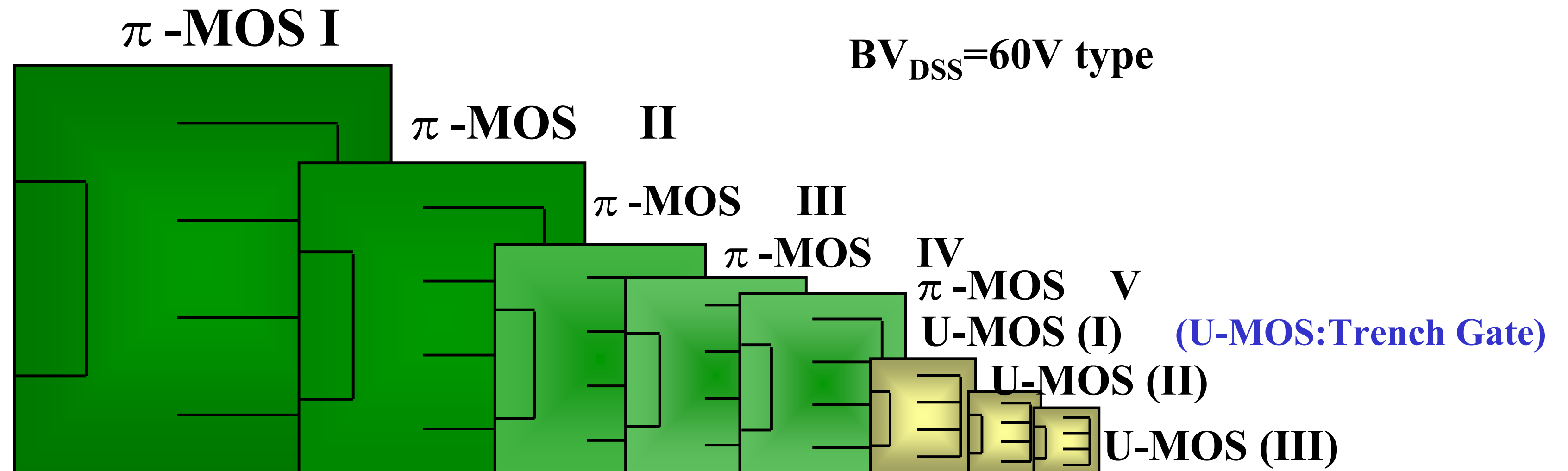
1980 1985 1990 1995 2000 2005 2010

Year



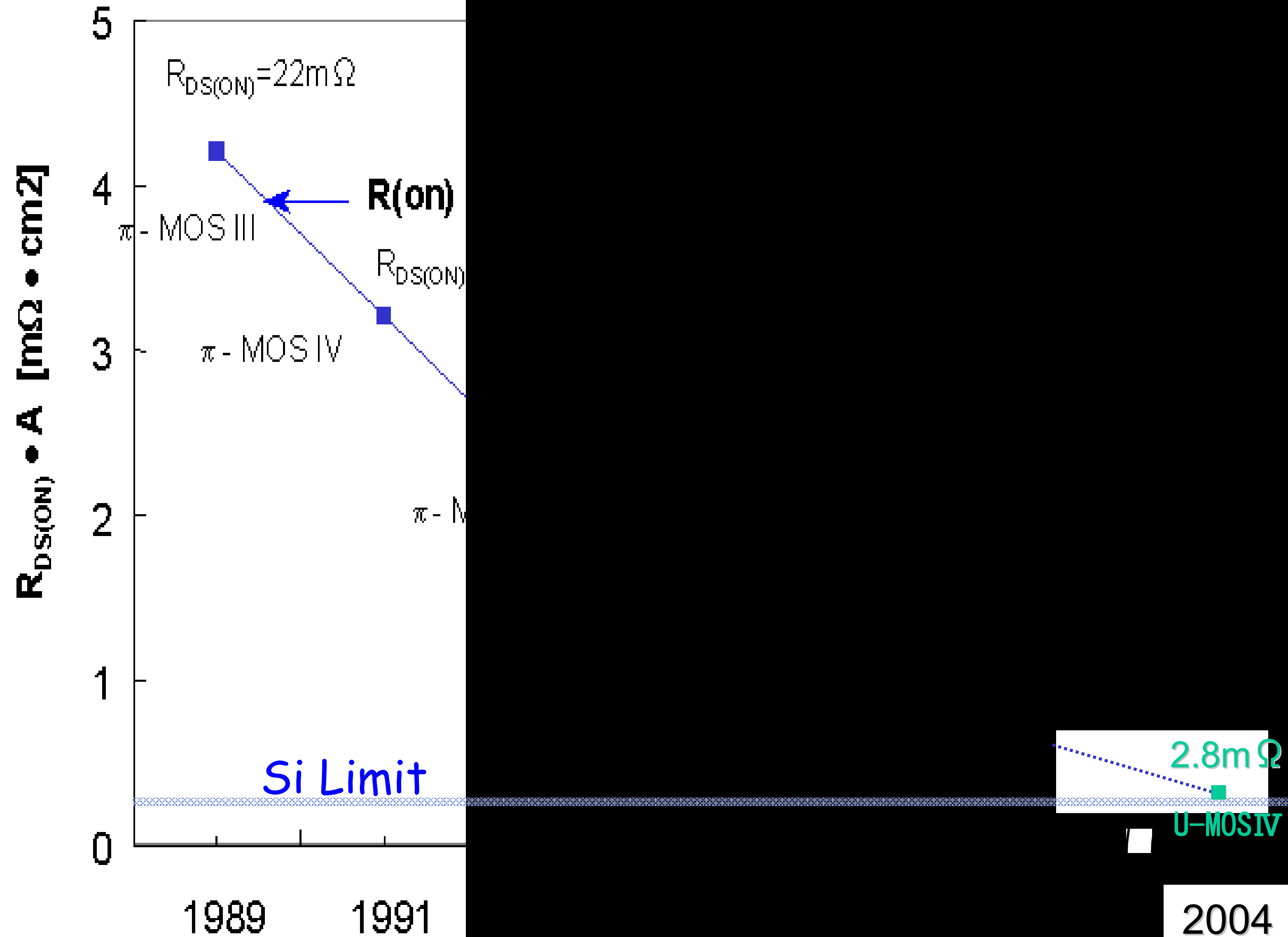
MOSFETチップ

パワーMOSFET チップ面積推移



	π-MOS I	π-MOS II	π-MOS III	π-MOS IV	π-MOS V	U-MOS(I)	U-MOS(II)	U-MOS(III)
チップサイズ（相対値）	1	0.6	0.33	0.25	0.2	0.08	0.05	0.04
$R_{DS(ON)}$ （mΩ・cm^2）	12.7	7.6	4.2	3.2	2.4	1	0.6	0.45
セル密度 （Mcells/Inch^2）		0.2	1	2	4	10	30	120
量産時期	1982	1984	1986	1989	1992	1994	1997	1999

60V MOSFETのオン抵抗の推移



Trends of Voltage Regulator Module (VRM)

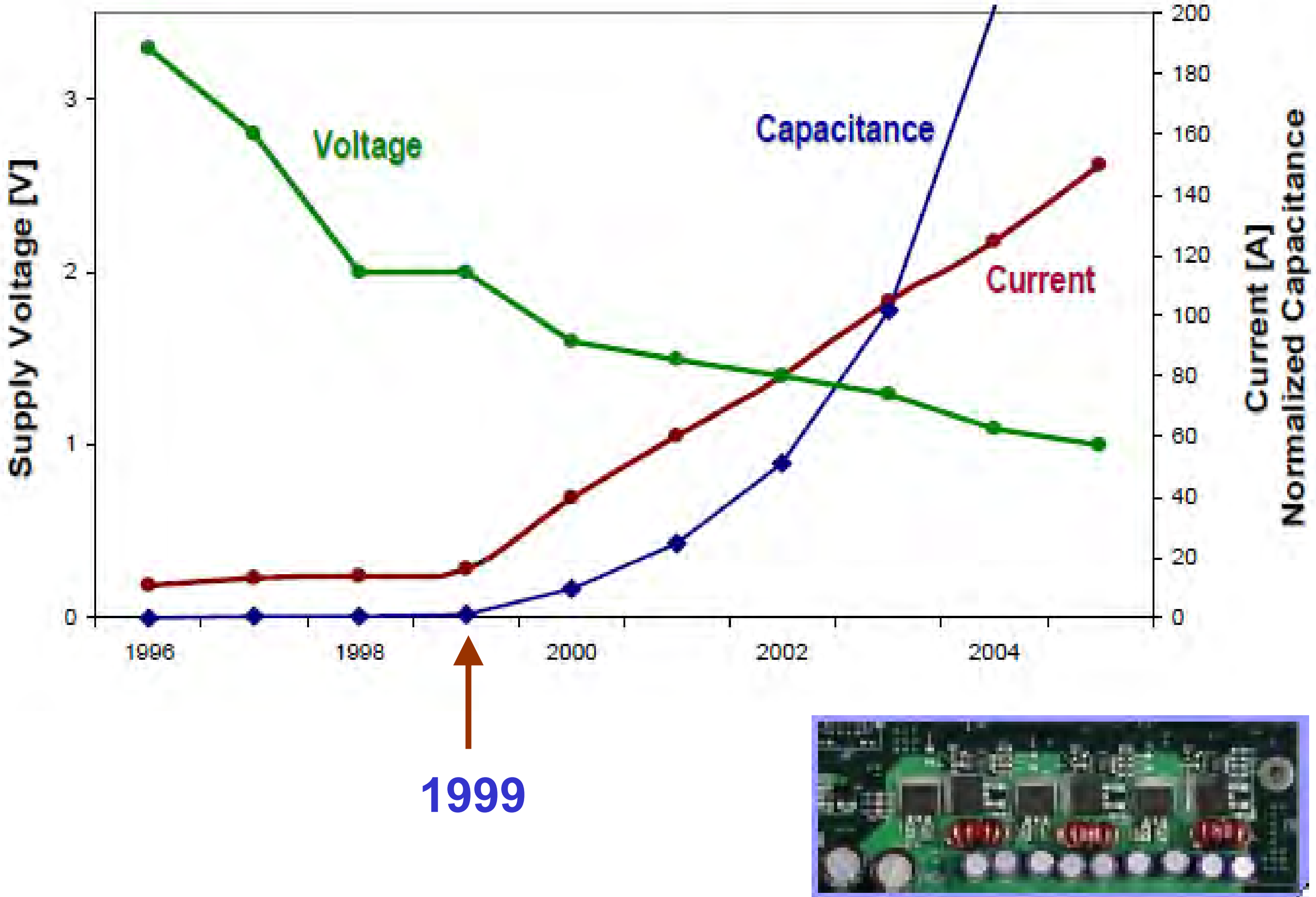
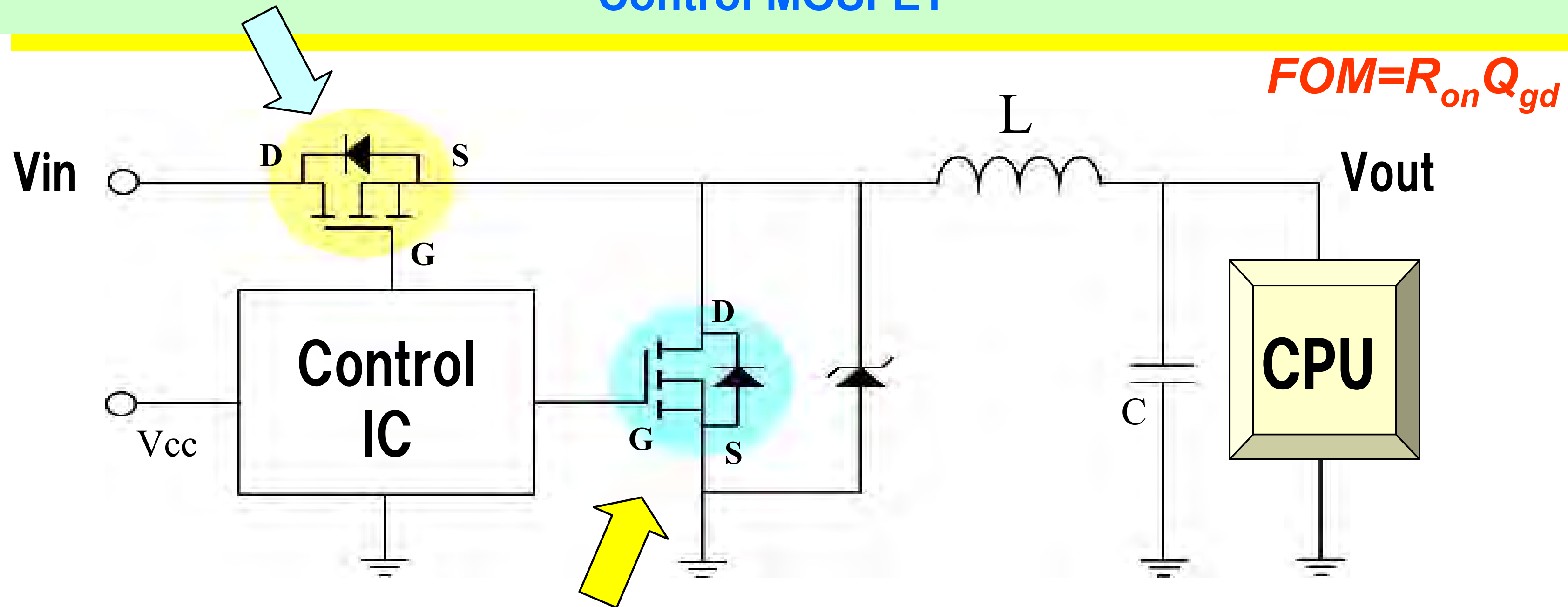


Figure of Merit

$P_{loss}=(I_d^2 \times R_{on}) + (I \times Q_{gd}/i_g \times V_{in} \times f) + (Q_g \times V_g \times f) + (Q_{oss}/3 \times V_{in} \times f)$

Control MOSFET



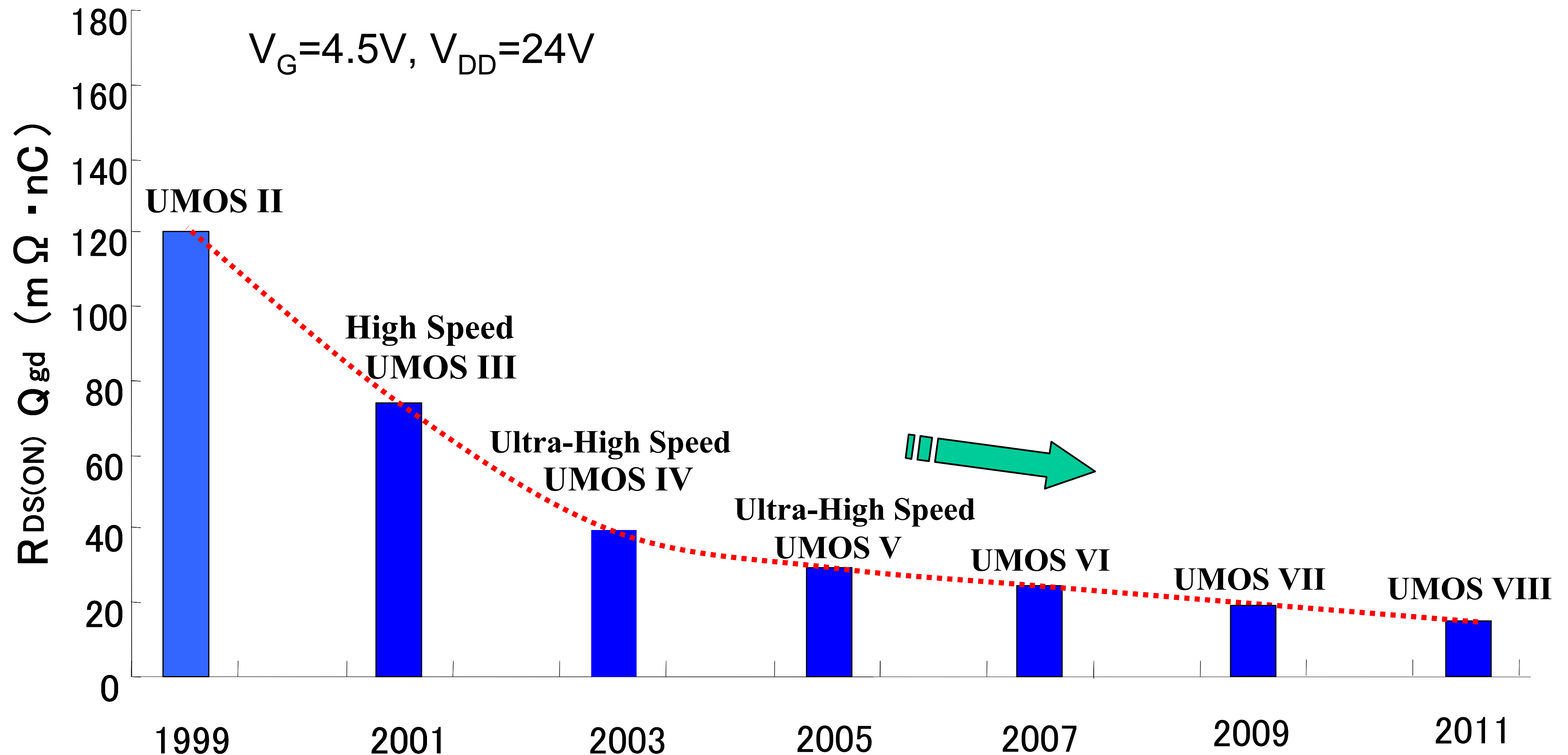
$P_{loss}=(I_d^2 \times R_{on}) + (Q_g \times V_g \times f) + (Q_{oss}/3 \times V_{in} \times f)$

Synchronous MOSFET

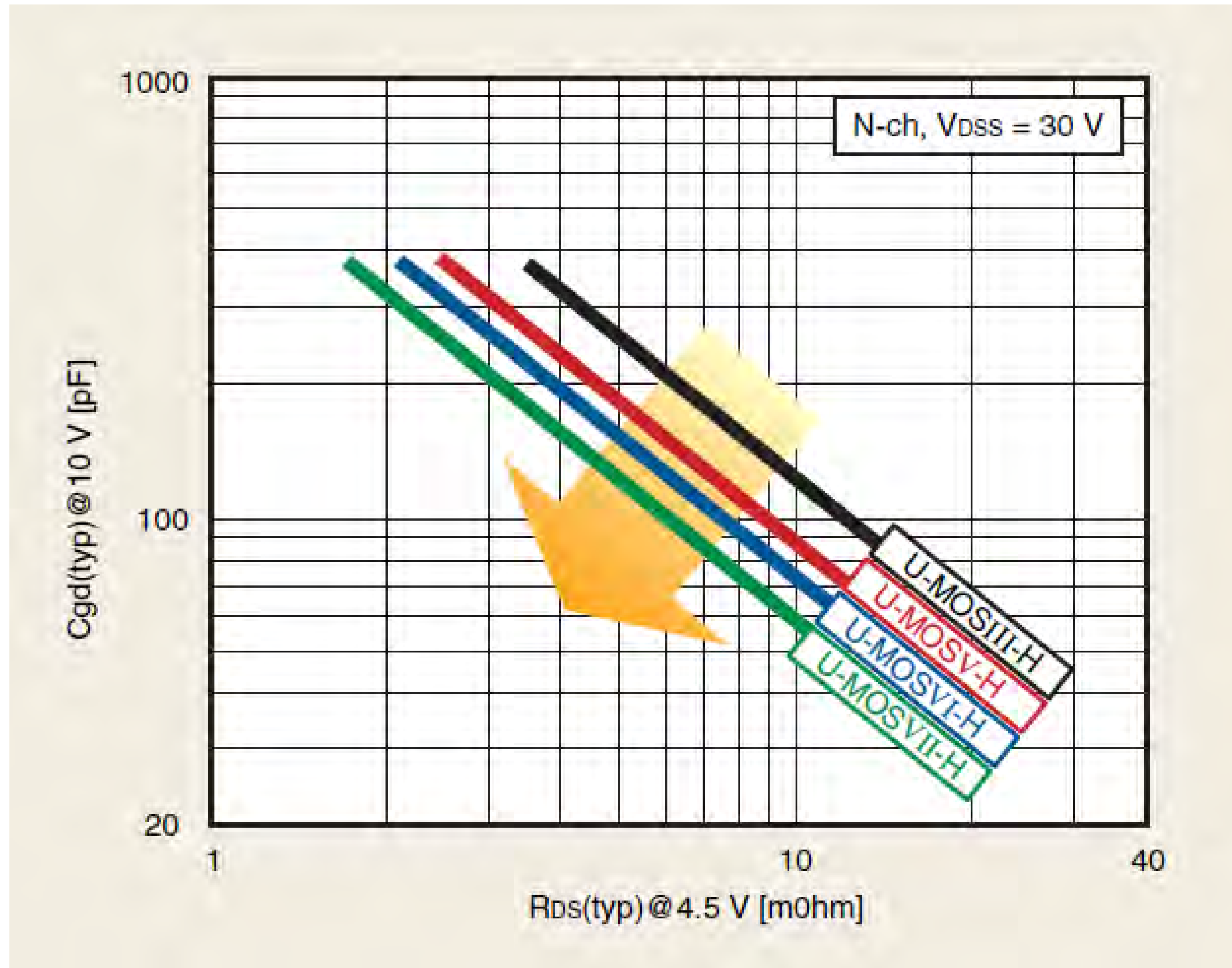
FOM=$R_{on}A$

Trend of High Speed MOSFET

Figure of Merit: $R_{on}Q_{gd}$



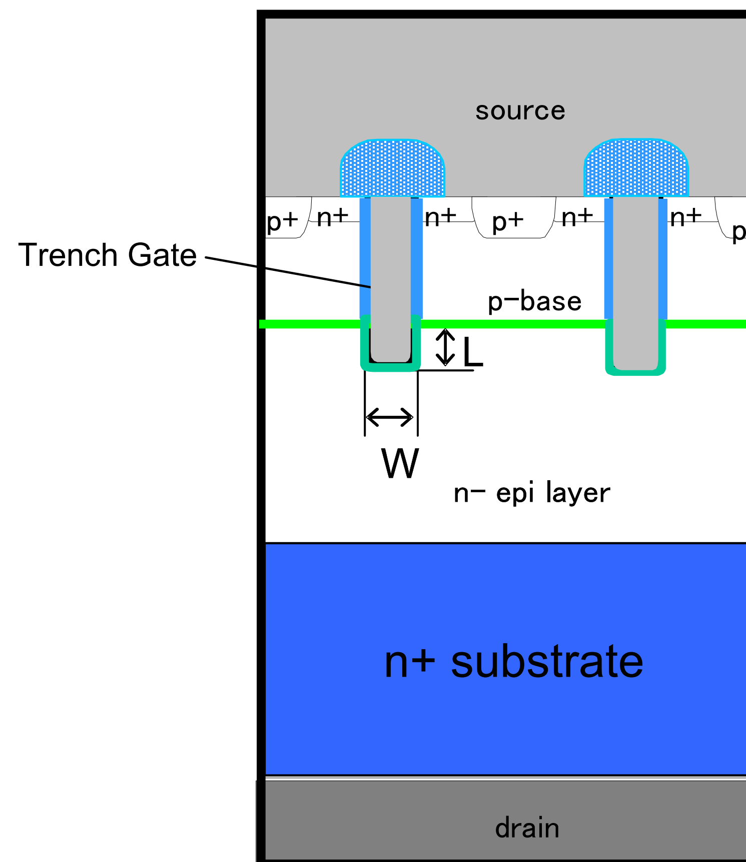
Technical Trend of High Speed U-MOS



縦型パワー MOSFETの容量

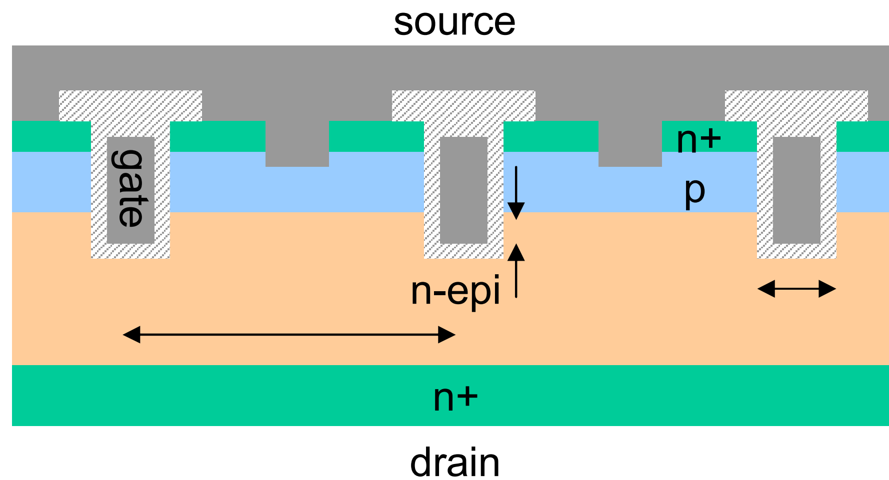
入力容量：Ciss＝Cgs+Cgd
出力容量：Coss＝Cgd+Cds
帰還容量：Crss＝Cgd

1999年以降、特に重要!!

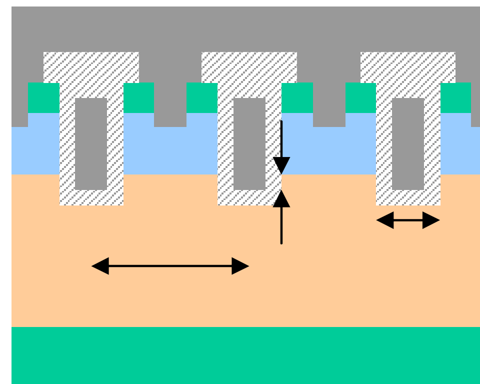


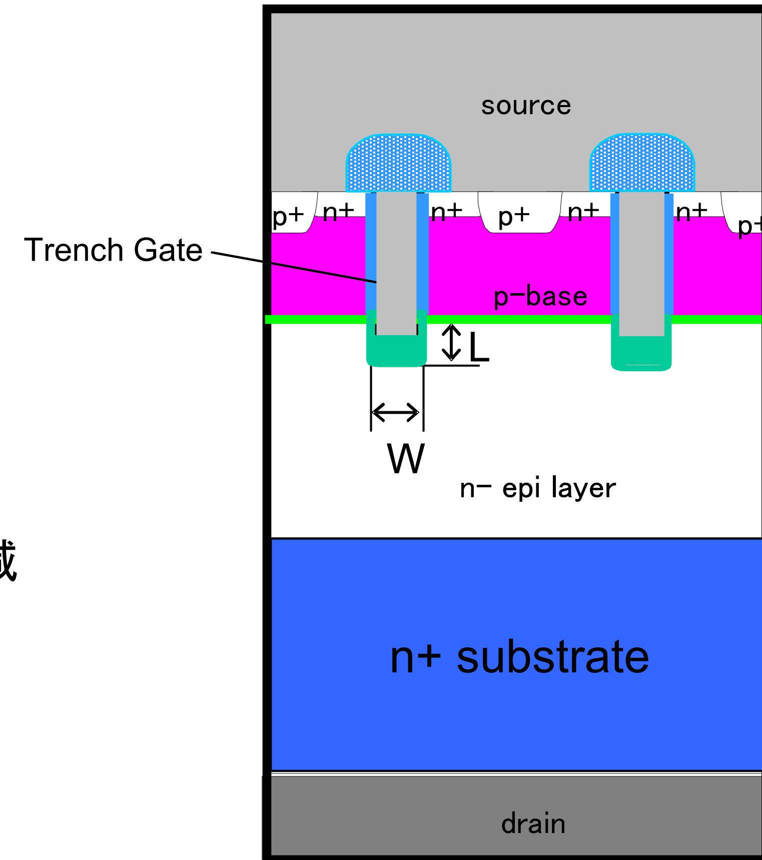
Ph-III

$R_{on}Q_{gd}$を下げる



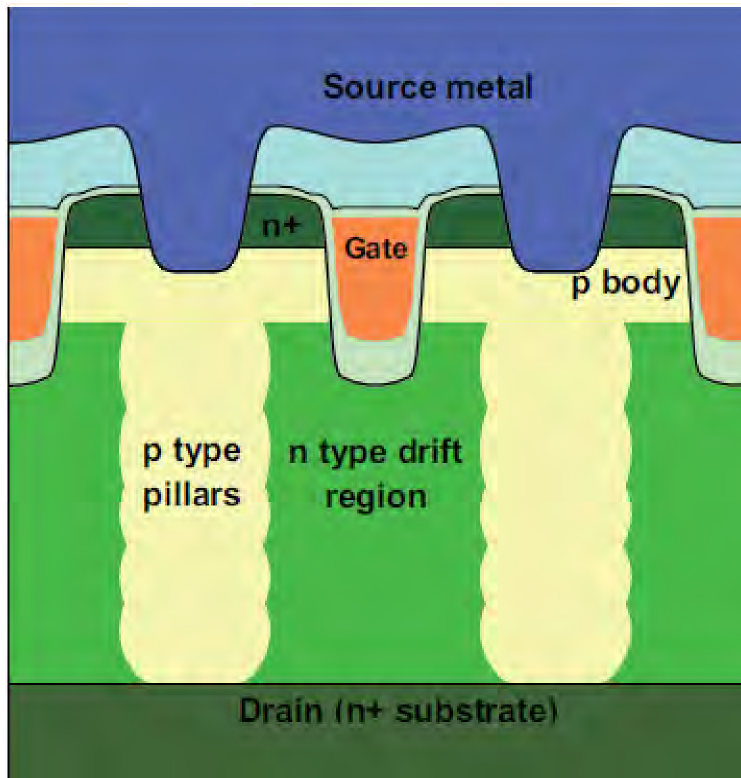
微細化
トレンチピッチ縮小によるRonA低減
トレンチ幅、トレンチ突出量縮小によるCgd低減



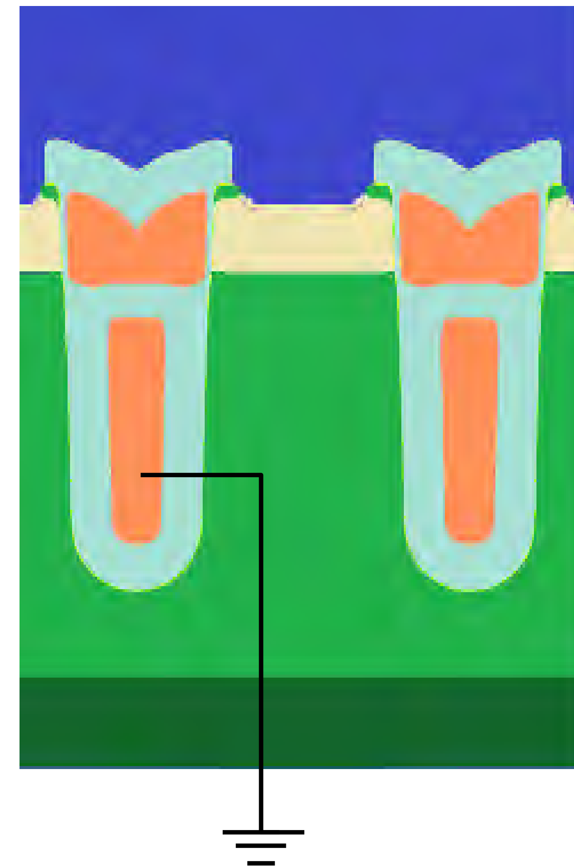


底を厚くする

Super Junction

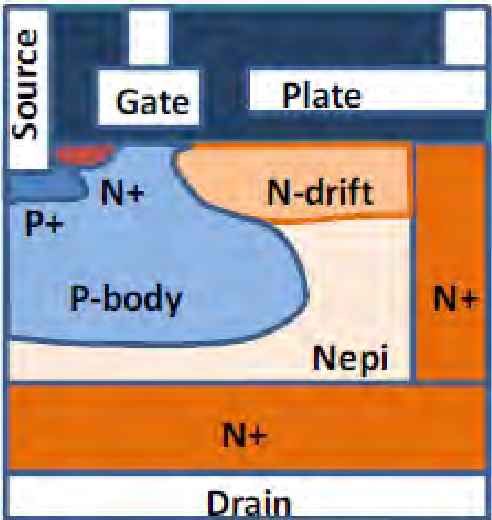


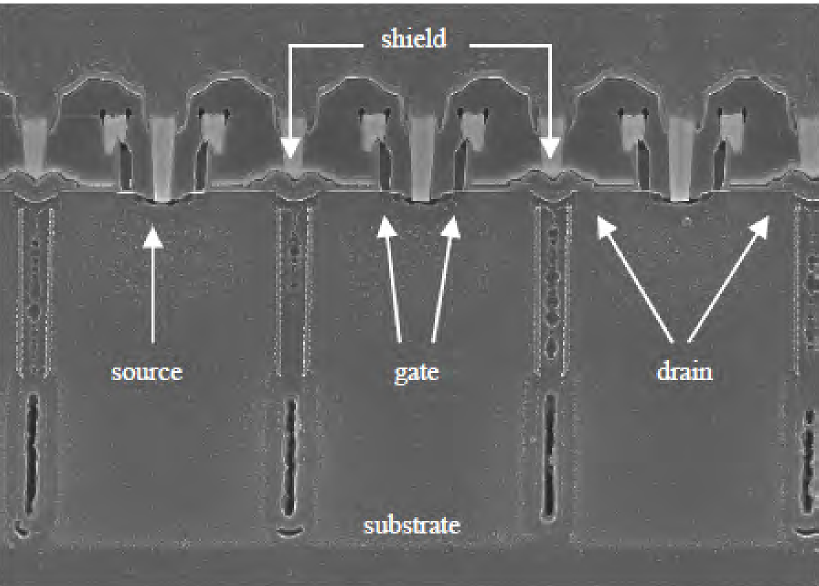
Field Plate (Split Gate)



ＳＪの詳細は後述

横型MOSFET





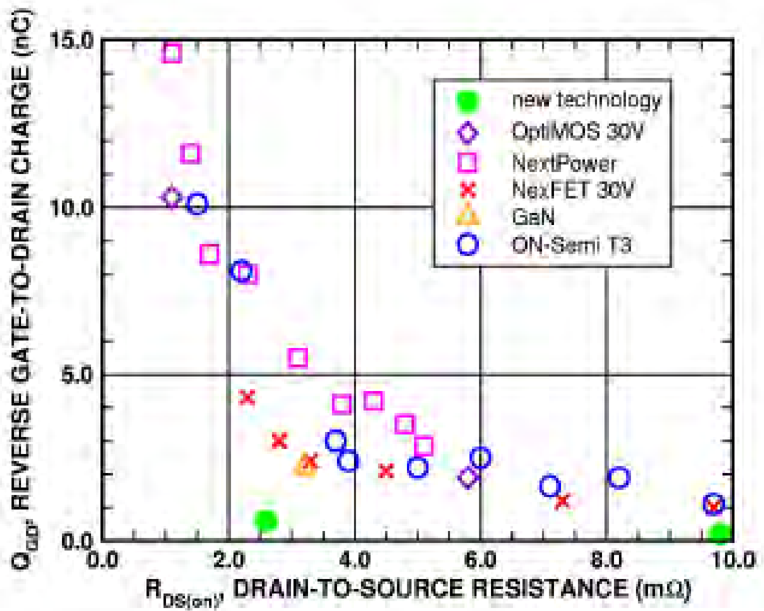
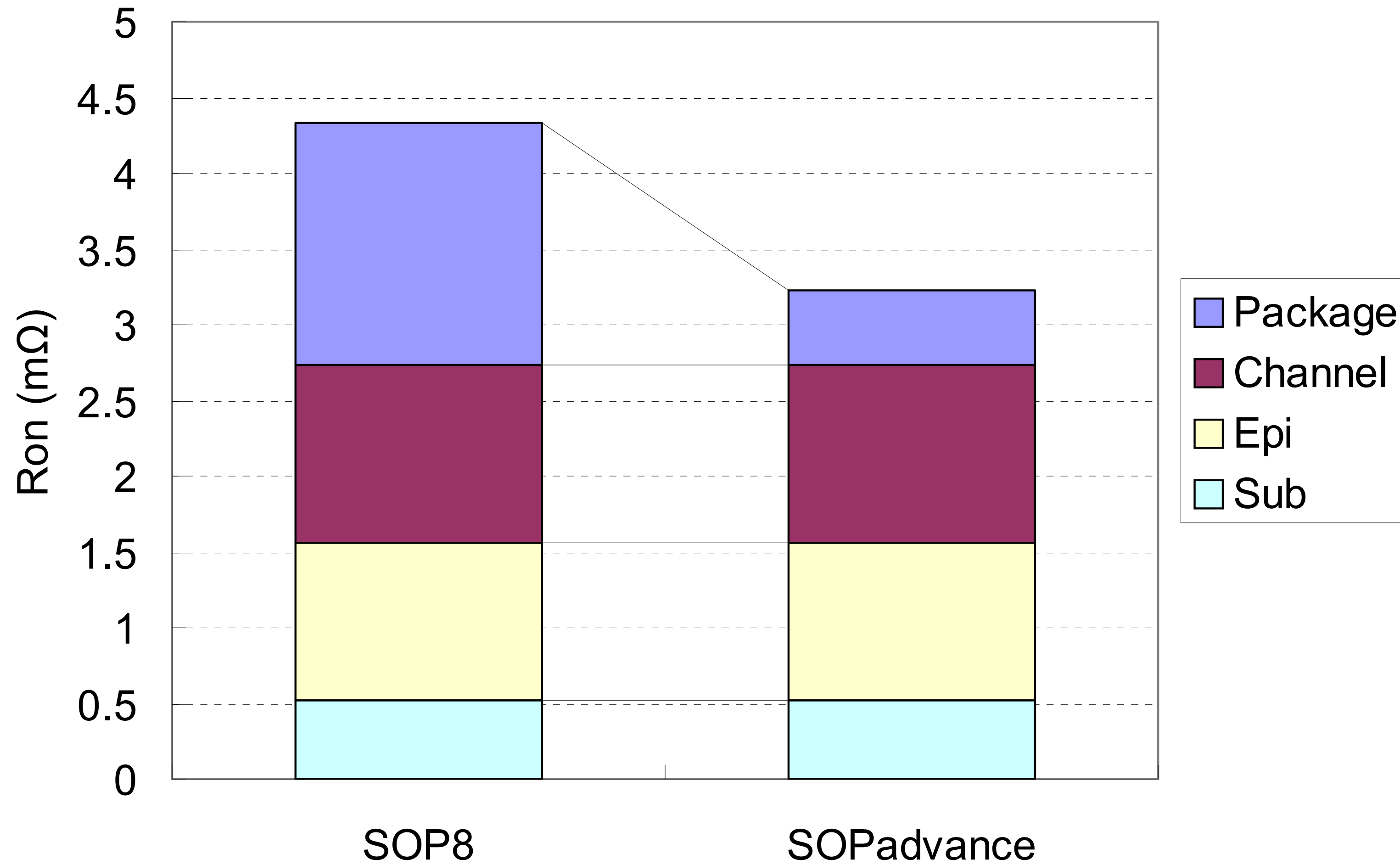


Figure 8. Comparison of the Miller charge (Q_{GD}) to other FET technologies [9-13] including OptiMOS™ (Infineon), NextPower™ (NXP), NexFET™ (Texas Instruments), GaN (IR and Efficient Power Conversion), and T3.

On Semiconductor

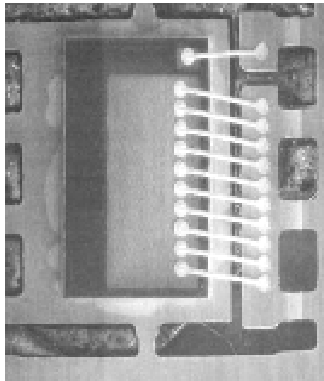
Ronで各部の占める割合

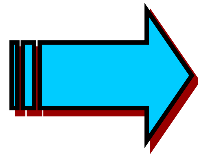


アルミストラップ技術

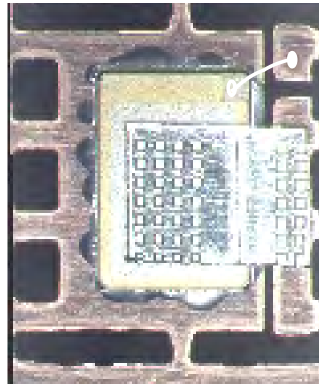
DirectFET

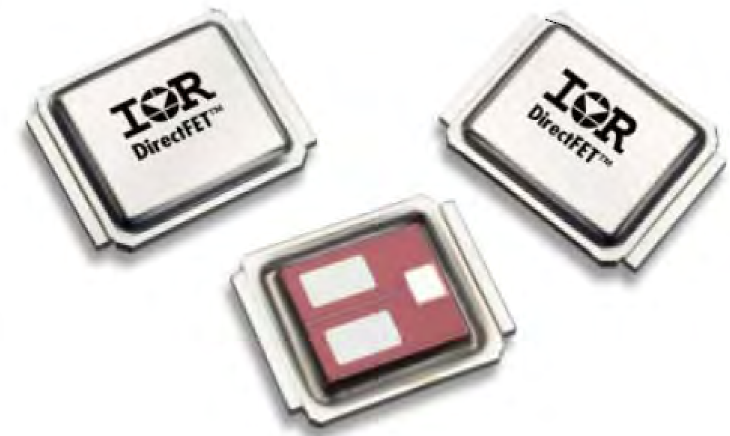
従来Au線B‘g品





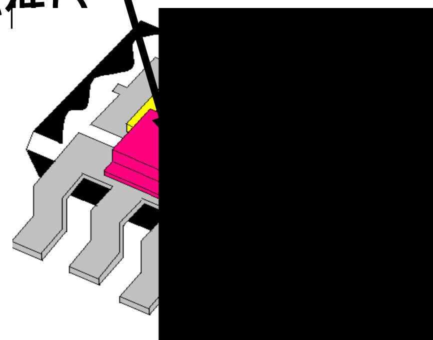
Alストラップ

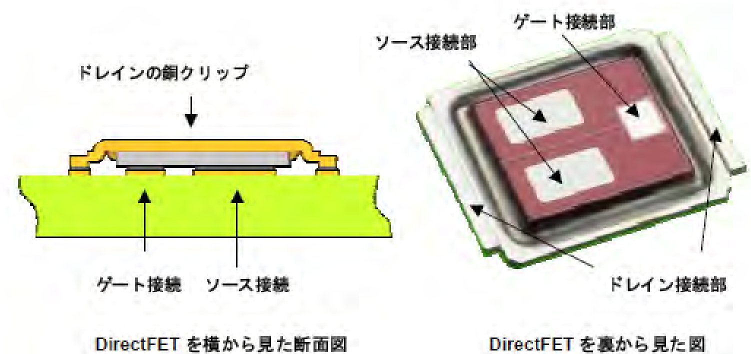




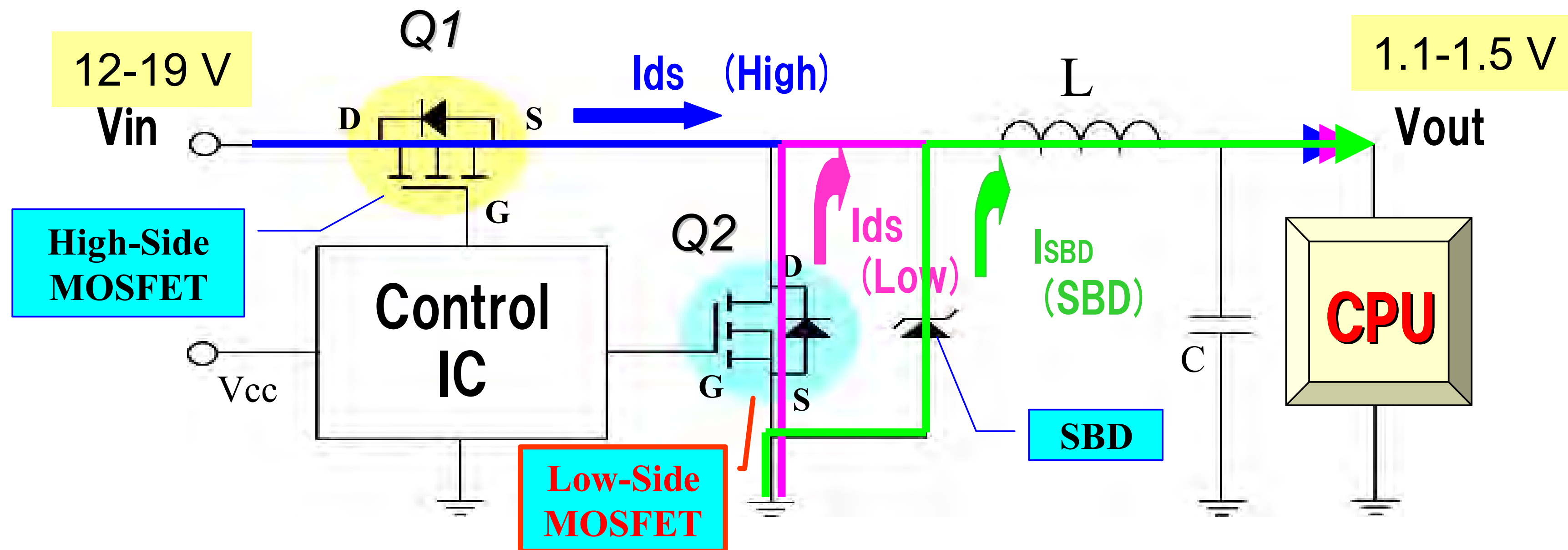
特長

- 抵抗値、インダクタンスが低い
- 高信頼性
- 熱抵抗の改善

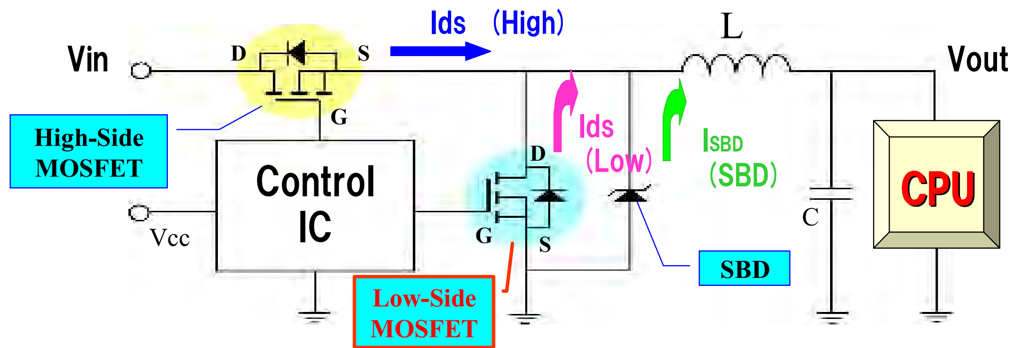


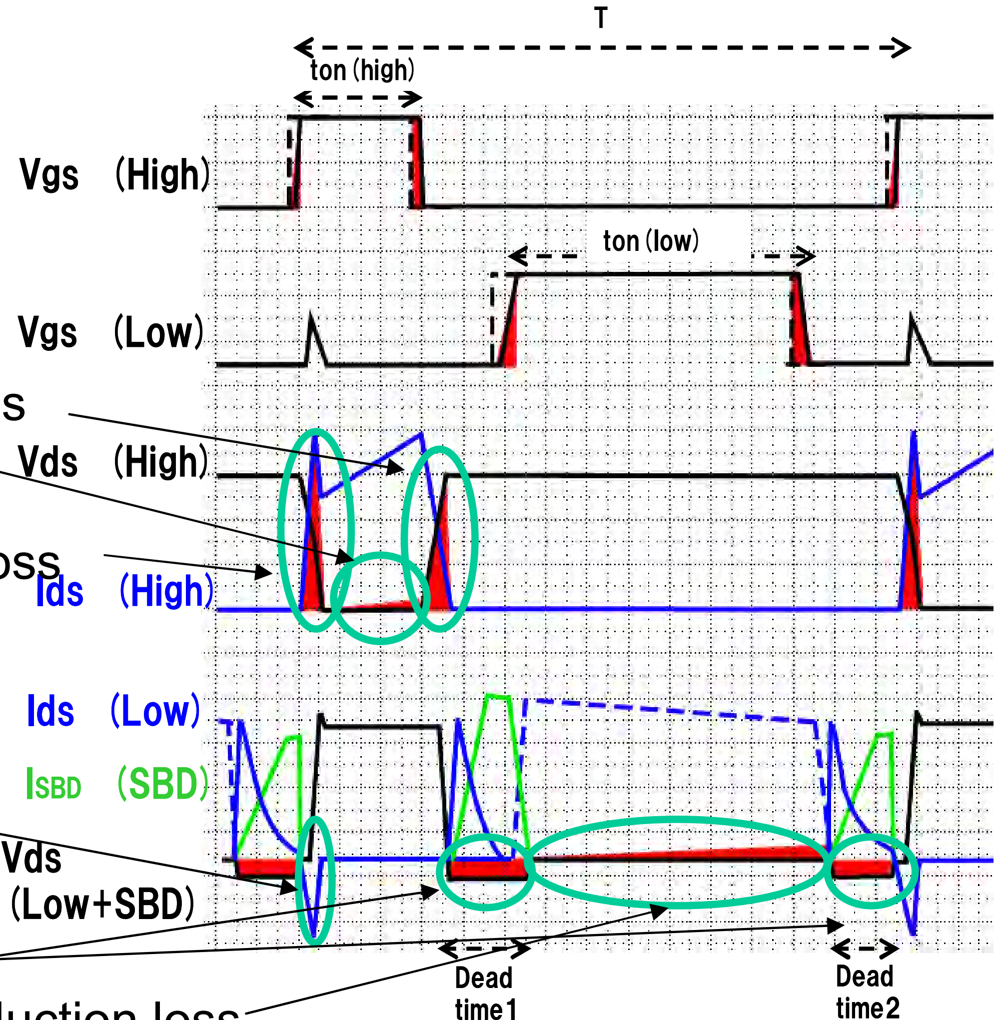


DC-DCコンバータの動作



DC-DCコンバータの動作と主な損失要因





High side turn off loss

high side conduction loss

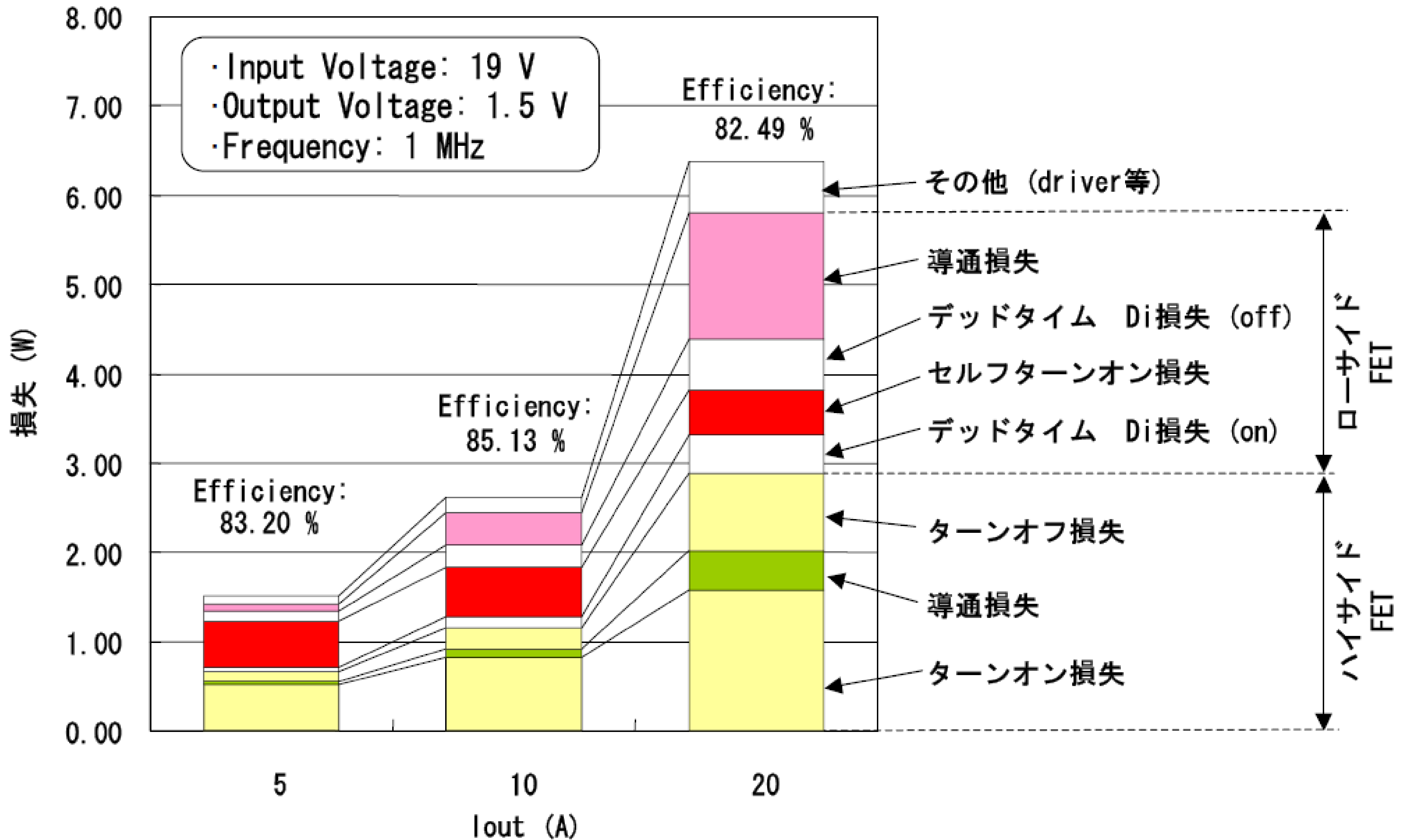
High side turn on loss

Low side MOSFET self turn-on occurs when the high side MOSFET turn on

Dead time diode loss

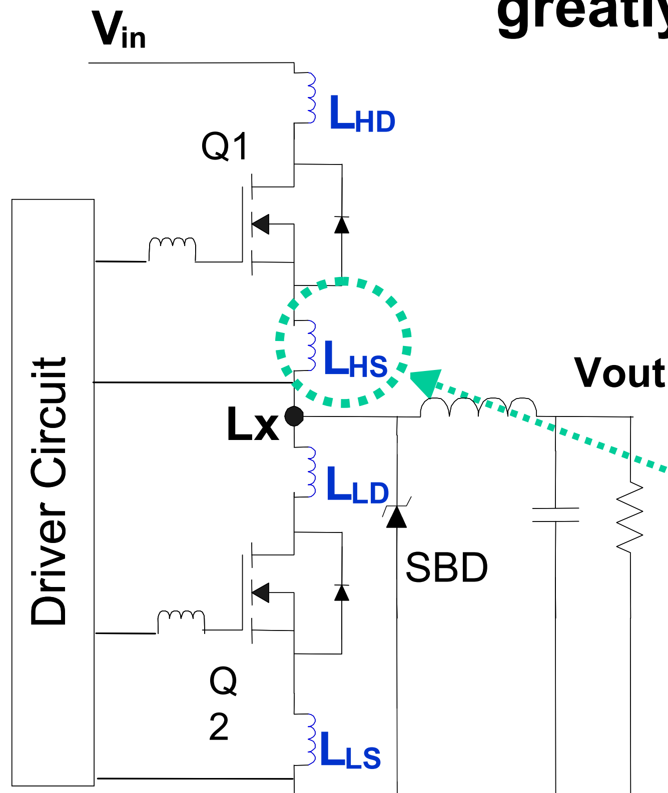
Low side conduction loss

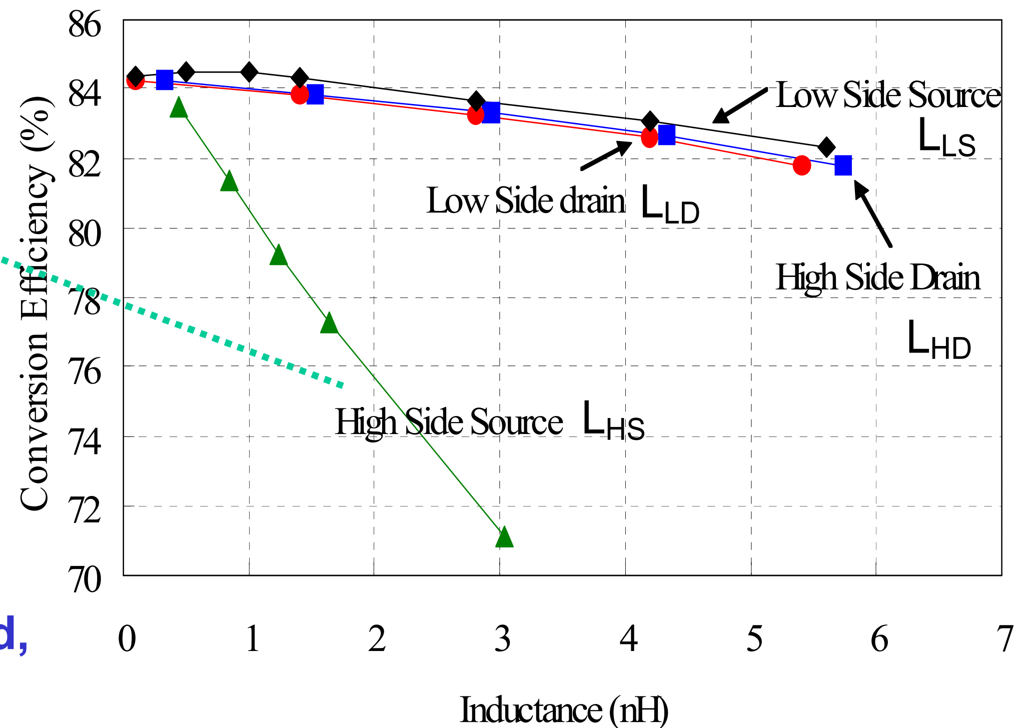
損失分布



Influence of parasitic inductances

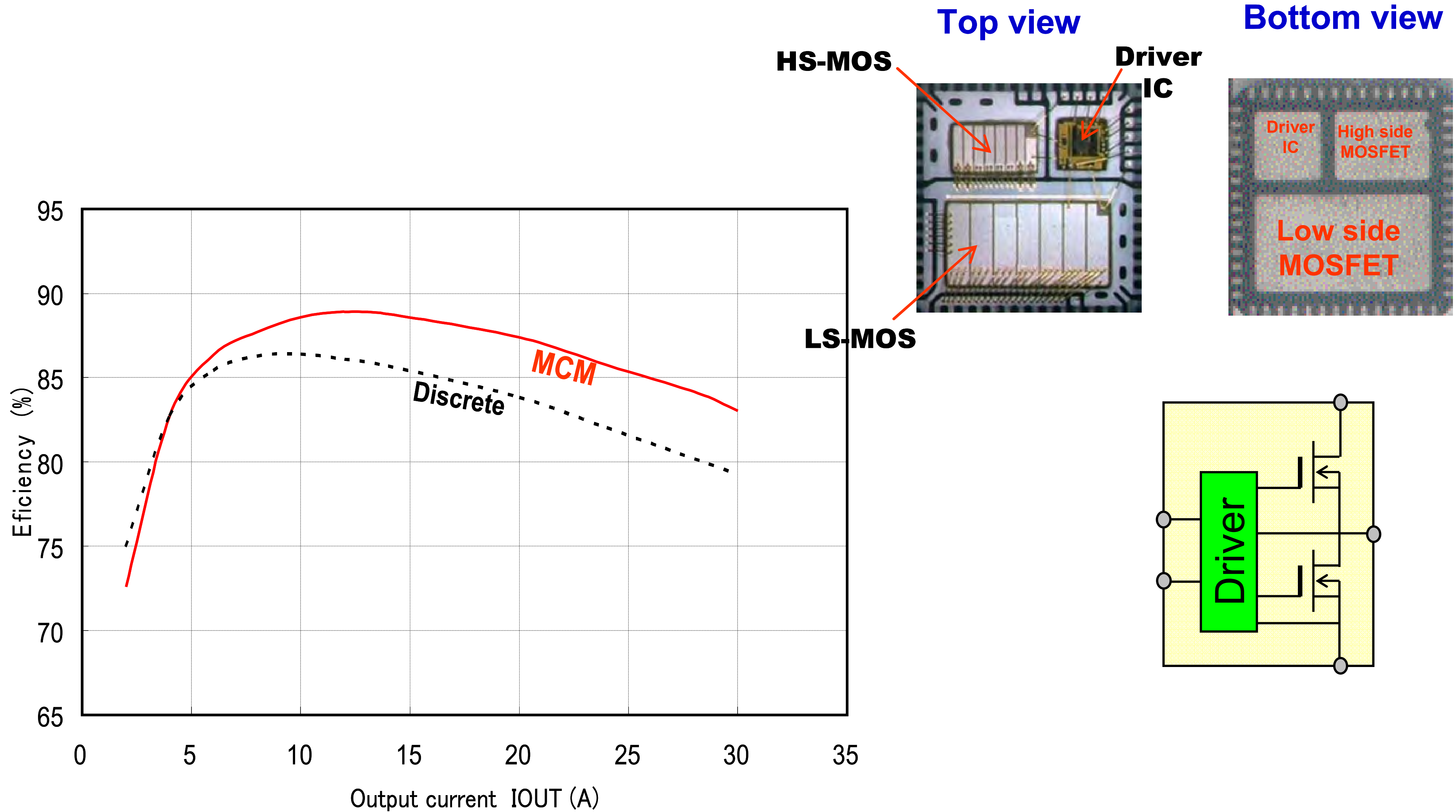
Parasitic inductances in the power stage circuit greatly influence the converter efficiency.





4 parasitic inductances are examined, using circuit simulator.

PWSiP：Multi-Chip-Module



New FOM の導入

$$NFOM = R_{on}Q_{str} = R_{on}J \cdot Q_{str}/J = V_F T_s$$

理想的な場合:

$Q_{str} = \varepsilon E_C$

$Ron = 4V_{BD}^2/\varepsilon\mu E_C^3$

$NFOM = 4V_{BD}^2/\mu Ec^2 = 4V_{BD}^2/BHFOM$

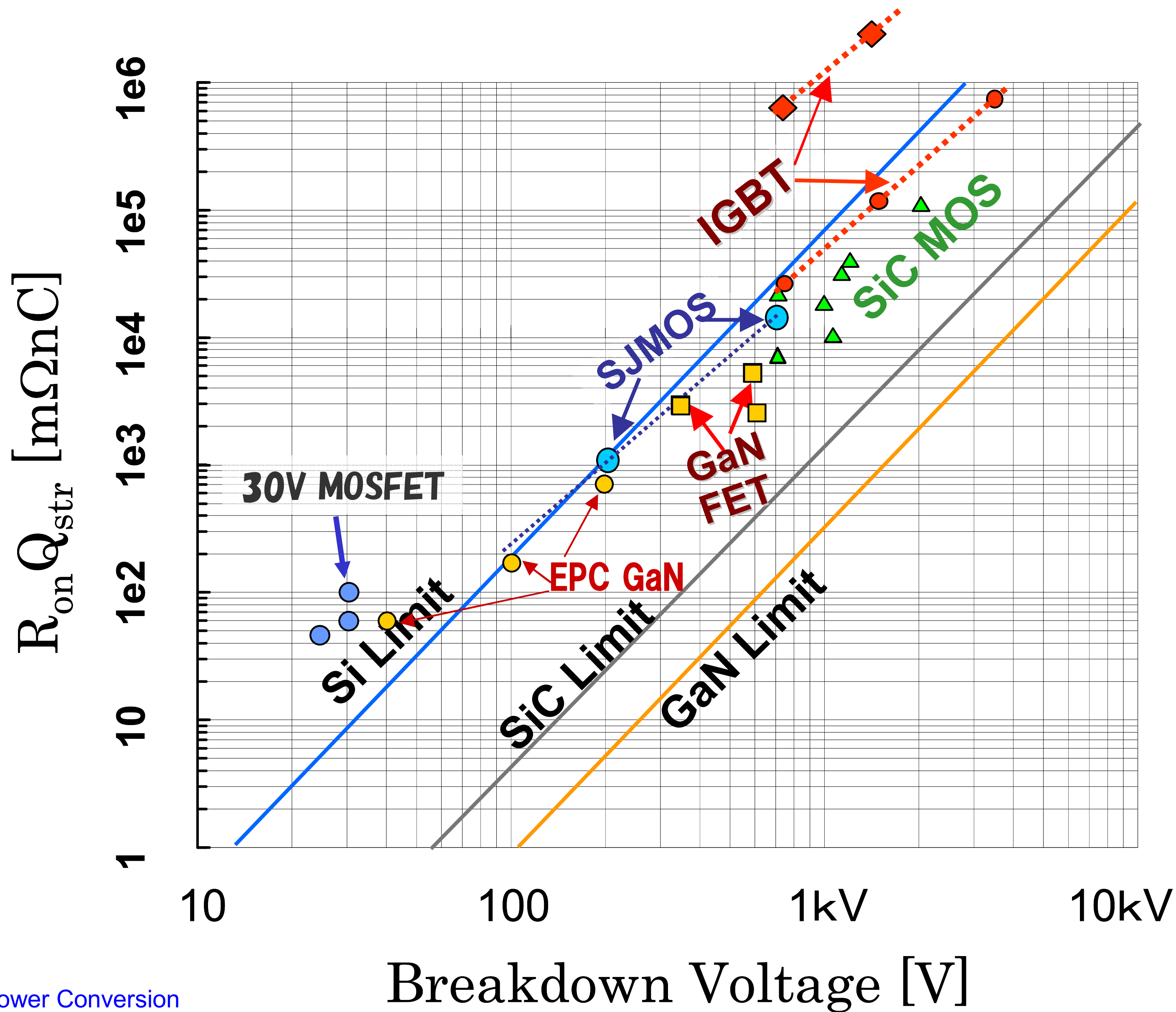
この場合、NFOMはBHFOMと逆比例。

NFOMは個々の素子で定義、BHFOMは材料で定義！

SiC と Si の比較

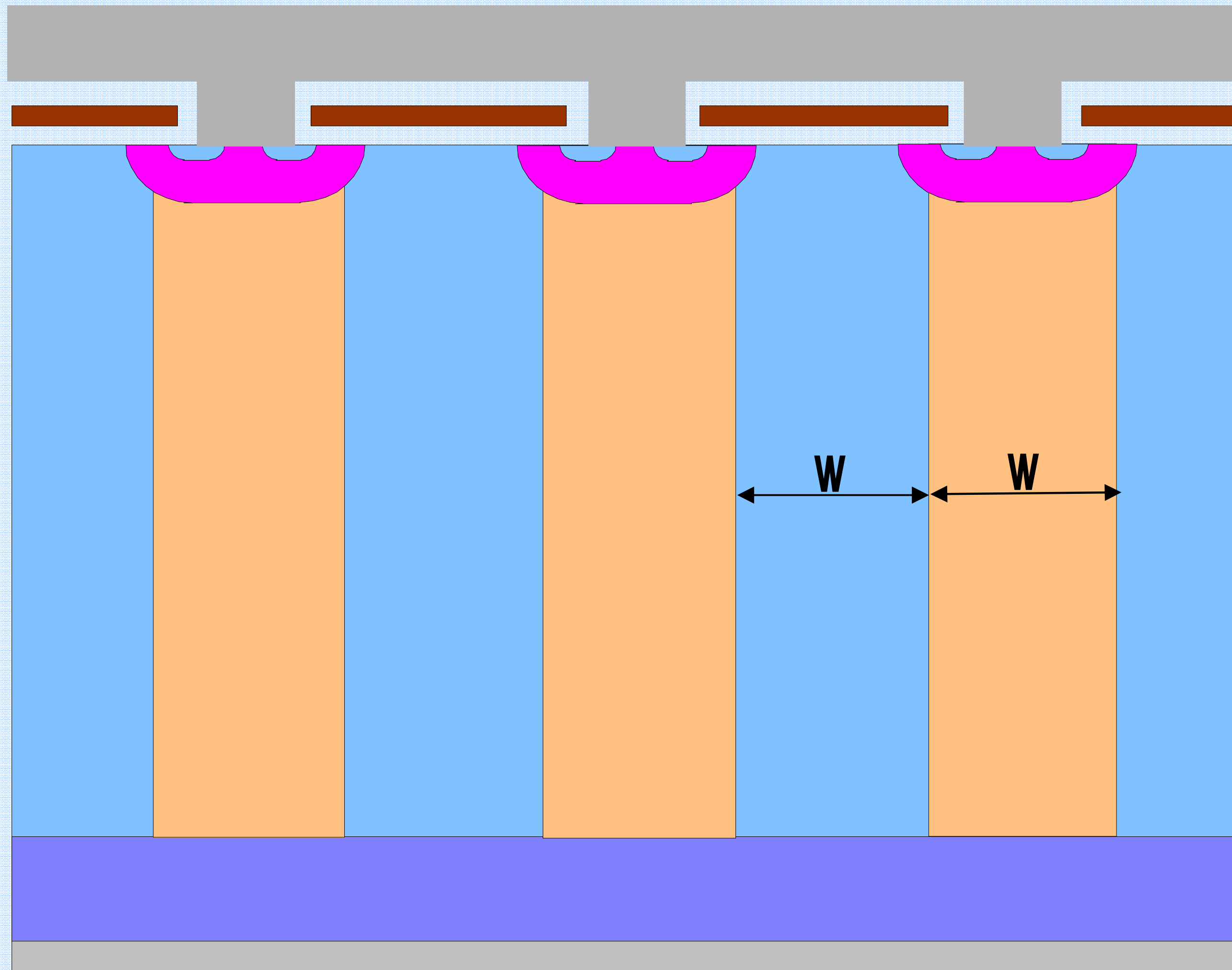
	SiC	Si
蓄積電荷(εEc)	$1.2x10^{13}q$(6倍)	$2x10^{12}q$
Switching速度Tsが同じになる電流密度	Siの6倍	1
R_{on}/V_{BR}^2	Siの280分の1	1
NFOM 同じTsのオン電圧	Siの46分の1	

New FOM: $R_{on}Q_{str}$ for high speed switching



EPC: Efficient Power Conversion

スーパージャンクション MOSFET

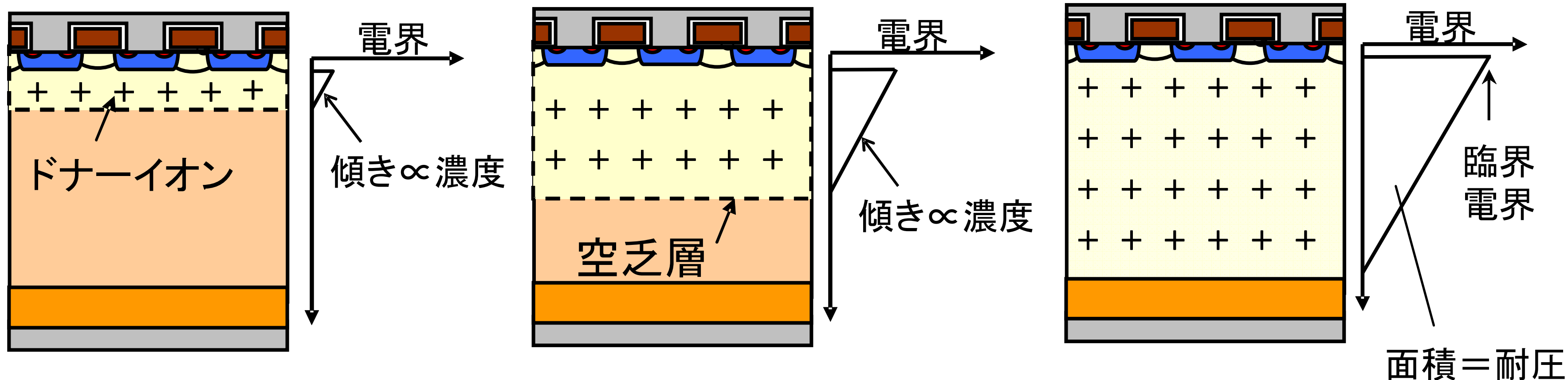


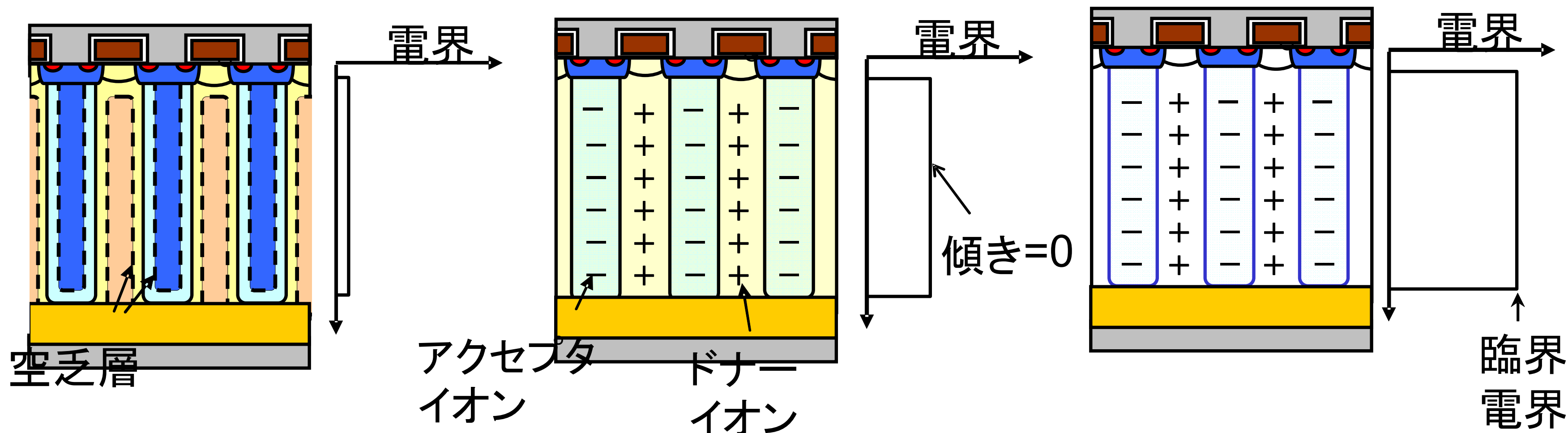
Super Junction 構造

印加電圧
V_{ds}～数V

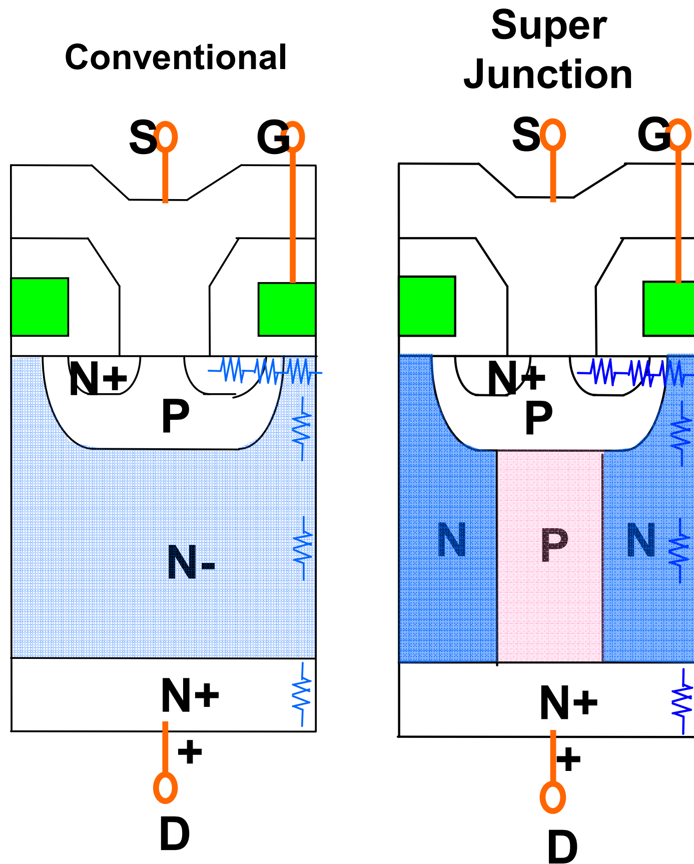
電圧印加

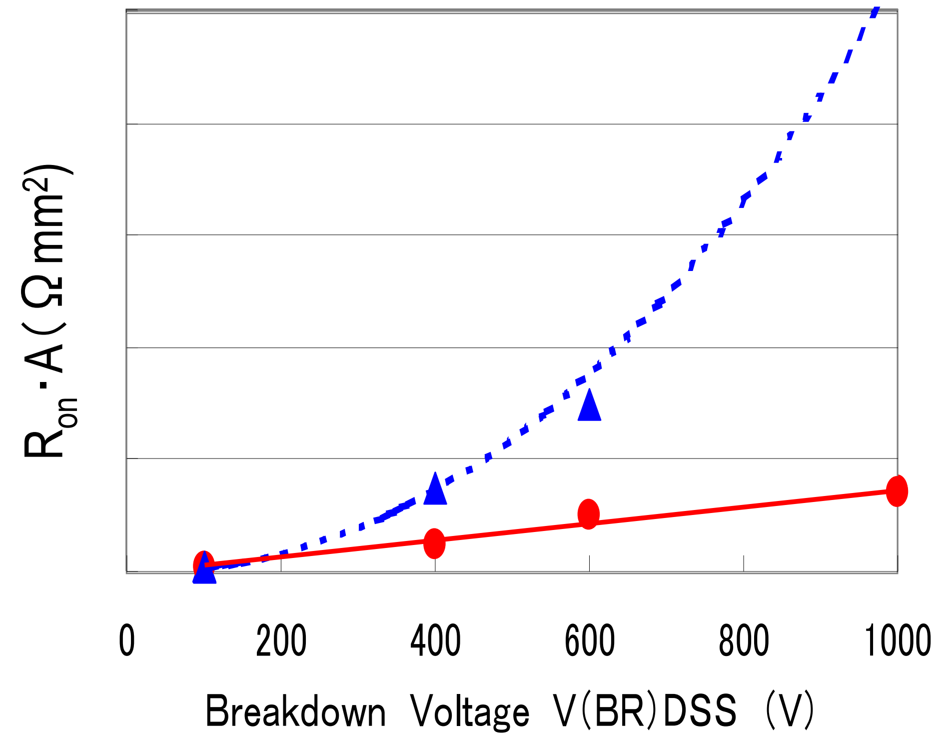
V_{ds}=耐圧





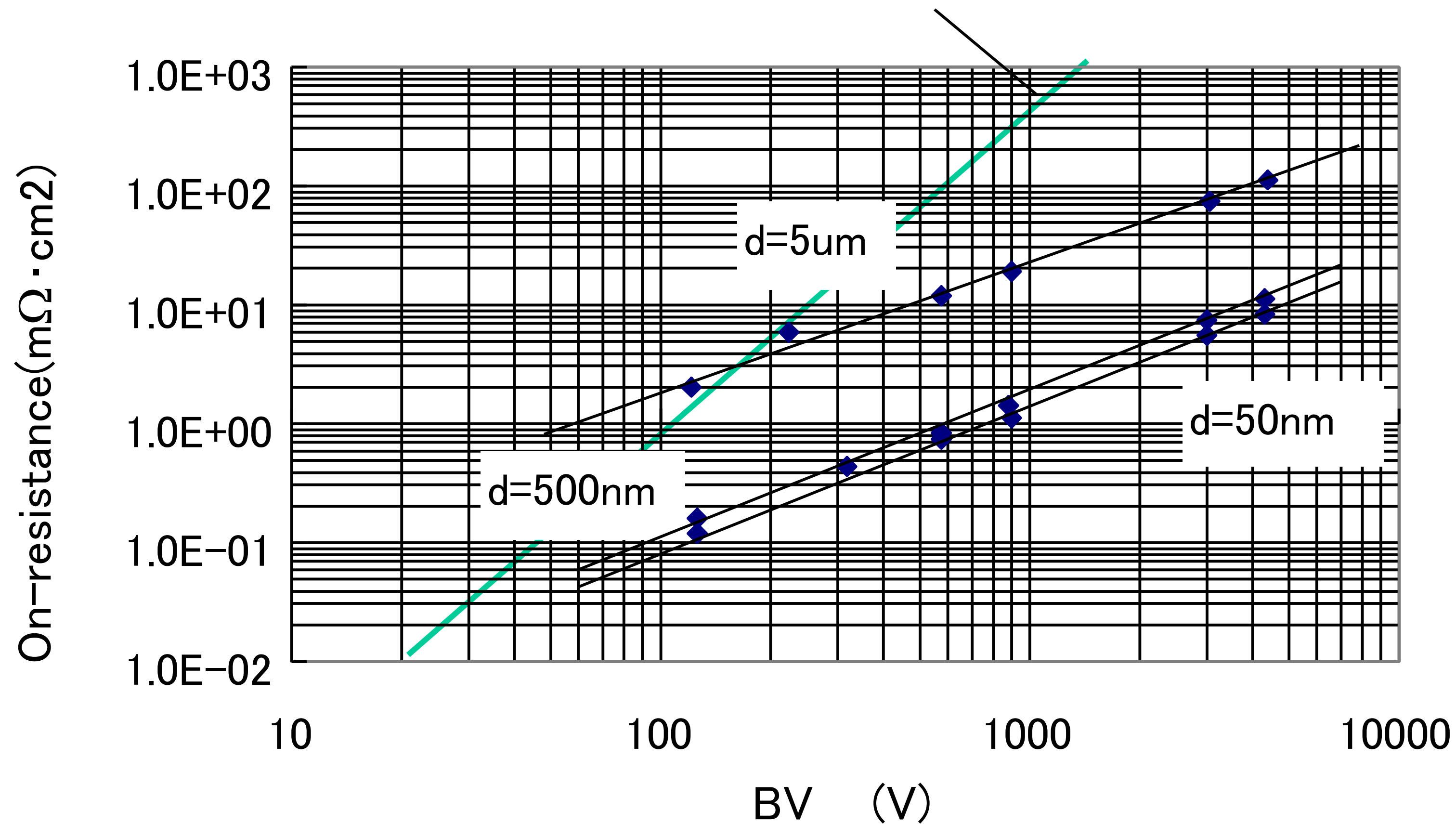
Super Junction MOSの構造比較



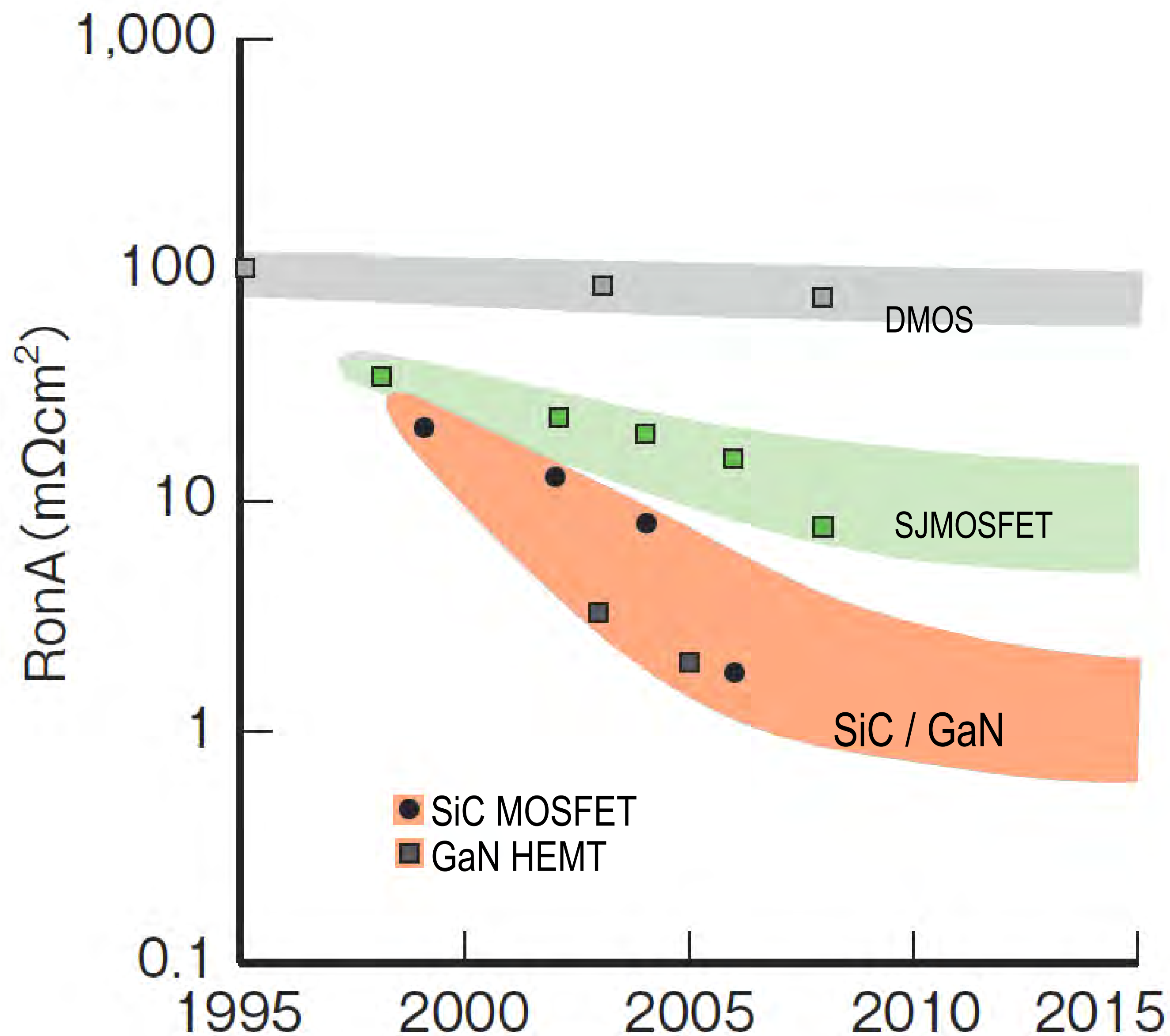


Dependence of the on-resistance on the breakdown voltage

limit of conventional MOSFET



600V系パワーMOSFET



出所: 東芝レビュー 2010年 Vol.65 No.10

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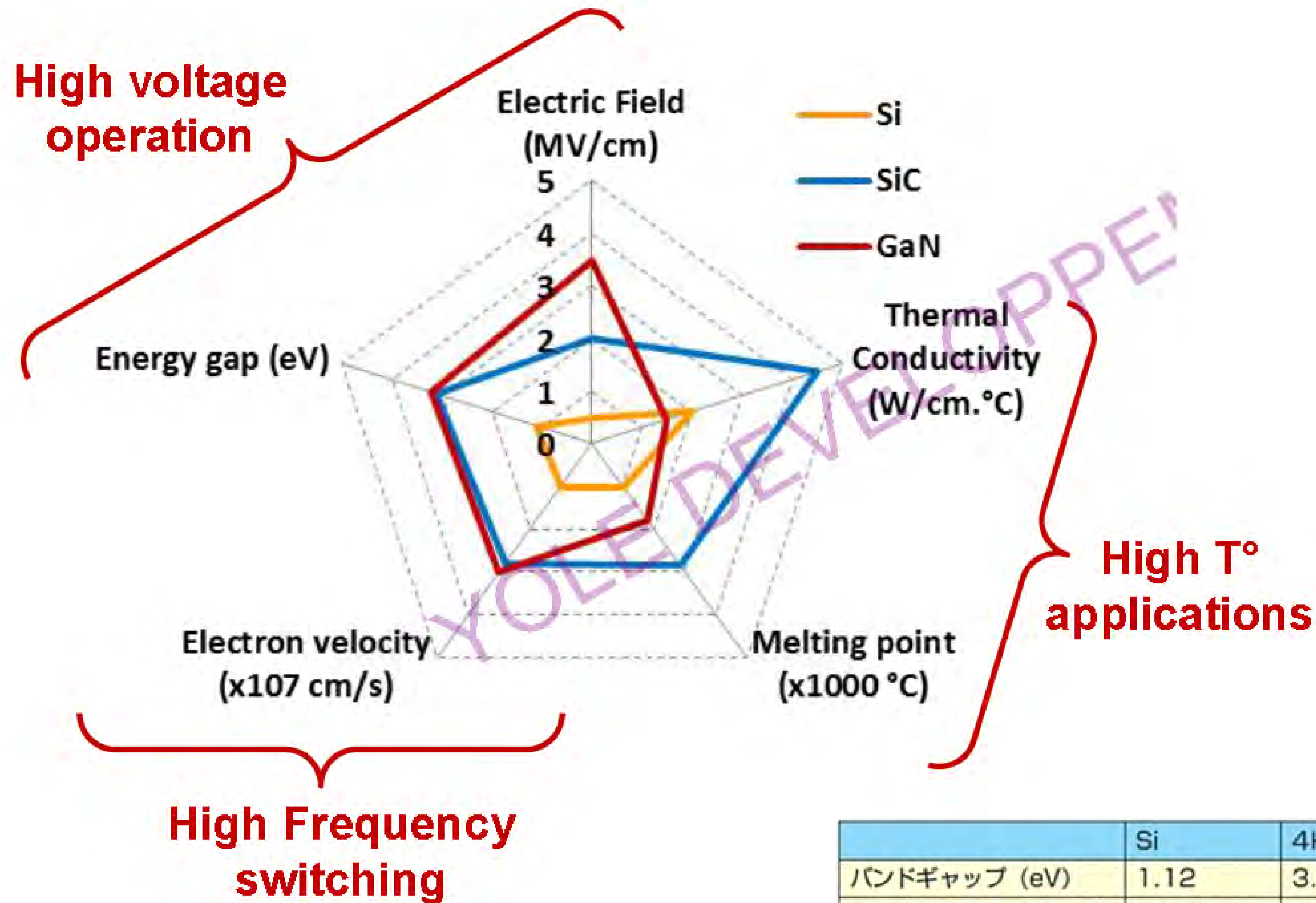
２．電気に依存する社会
３．パワーエレクトロニクス
４．パワーデバイスの市場
５．IGBTとその発展の経緯
６．IGBTのシリコン限界に向けた今後の展開
７．パワーMOSFETの発展の経緯と
今後の可能性
８．新材料デバイス
９．製造プロセス
10. まとめ

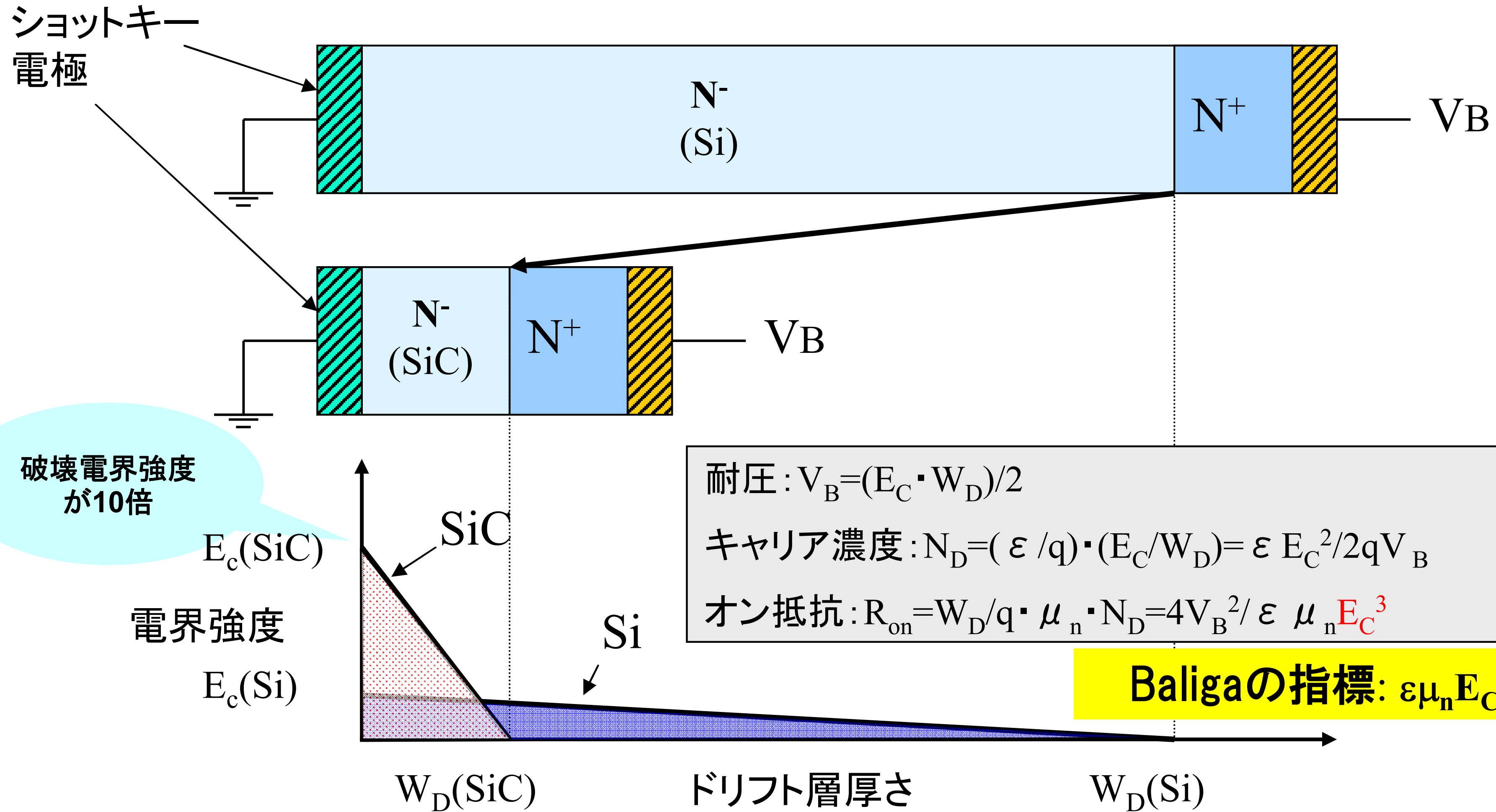
SiC vs. GaN vs. Si
Figure-of-merit



出所:SEMI Forum Japan June 14 2012
Yole Development

	Si	4H-SiC	GaN	GaAs(参考)
バンドギャップ (eV)	1.12	3.26	3.42	1.42
電子移動度 ($cm^2/v \cdot s$)	1350	1000	1200	8500
絶縁破壊電界 (MV/cm)	0.3	2.8	3	0.4
熱伝導率 (W/cm・k)	1.5	4.9	1.3	0.46
飽和ドリフト速度(cm/s)	1.0×10^7	2.2×10^7	2.4×10^7	1.0×10^7

SiCパワーデバイスが低損失になる理由

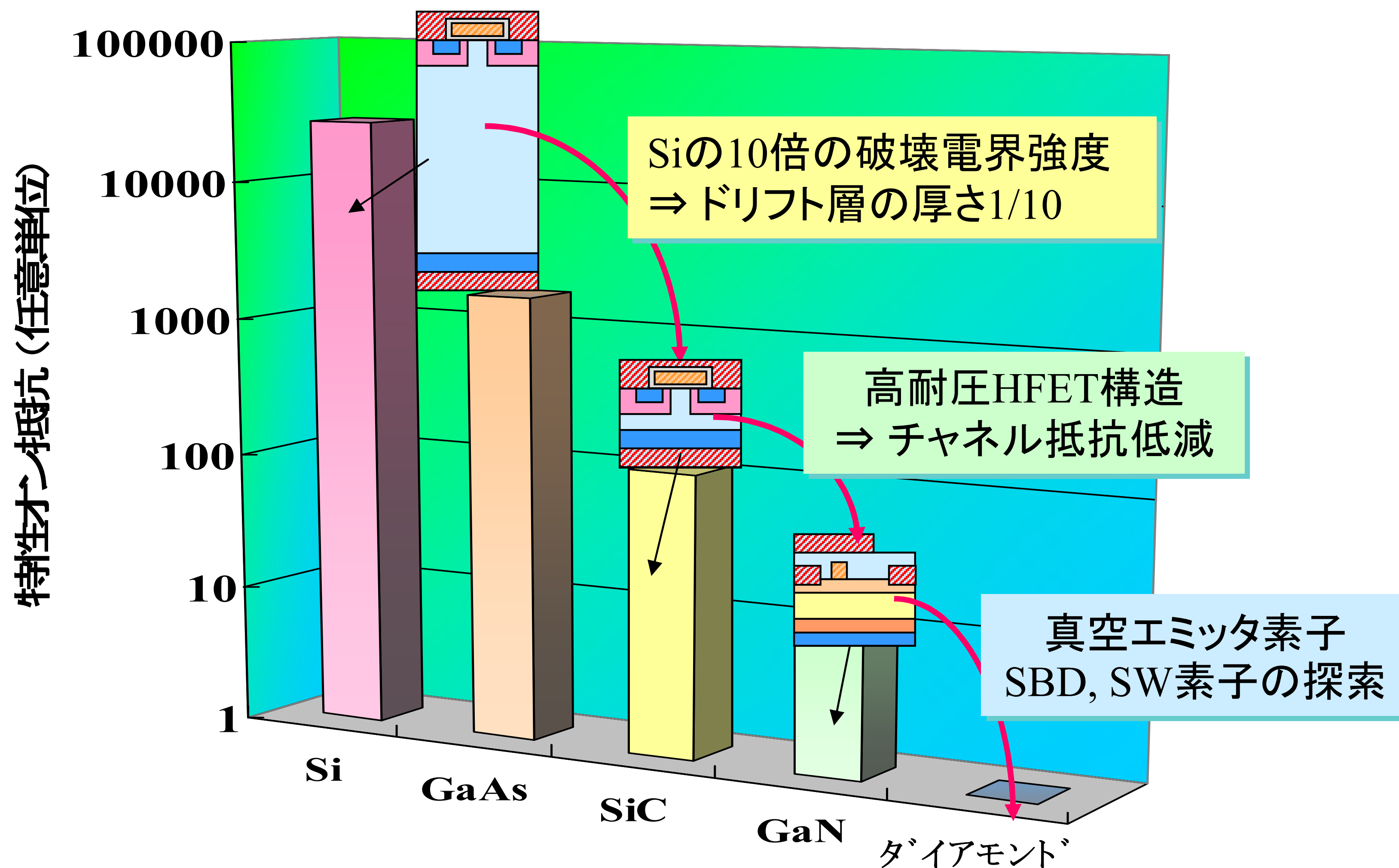


Si素子の約1/10のドリフト層厚さ、オン抵抗は約1/300に減少

耐圧300V以上でもSBD構造が利用可能

逆回復電荷 Qrr～90%減

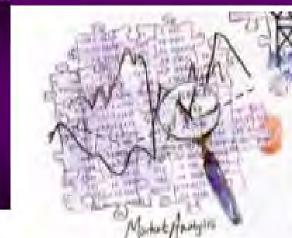
ワイドバンドギャップ半導体による低損失化



材料	ダイヤモンド	GaN on Si	4H-SiC	GaAs	Si
バンドギャップ (eV)	5.47	3.39	3.26	1.43	1.12
BM (対 Si)	27128	653	340	16	1

SiC Devices

Possible applications in silicon power electronics



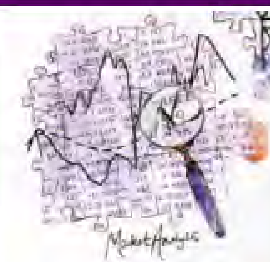
SiC can displace Silicon in:

- **IT & consumer**
  - PFC / power supplies → Electronic appliances & Computing
  - Converter / inverter → UPS
- **Automotive**
  - DC/AC inverter → Hybrid automotive
  - DC/DC Converter → Hybrid automotive
- **Industry**
  - Inverter → Power distribution, Rail transport., P.V., Motor control, UPS, Wind turbines

YOLE DEVELOPMENT

出所:SEMI Forum Japan June 14 2012
Yole Development

SiC Device Application Roadmap
Time to market



SiC diode only → SiC diode & transistor

Application	Start
SiC in Smart Grid, Rail, propulsion, HV apps	~2015 → > 2020
SiC electronics in HEV & EV	~2014 → > 2020
SiC in wind turbines	~2013 → > 2020
SiC in industry motor AC drives	2010 → > 2020
SiC in UPS	2010 → > 2020
SiC in solar inverters	2008 → > 2020
SiC Schottky diodes in Power Factor Correctors	< 2006 → > 2020
HB-LEDs GaN/SiC for lighting	< 2006 → > 2020

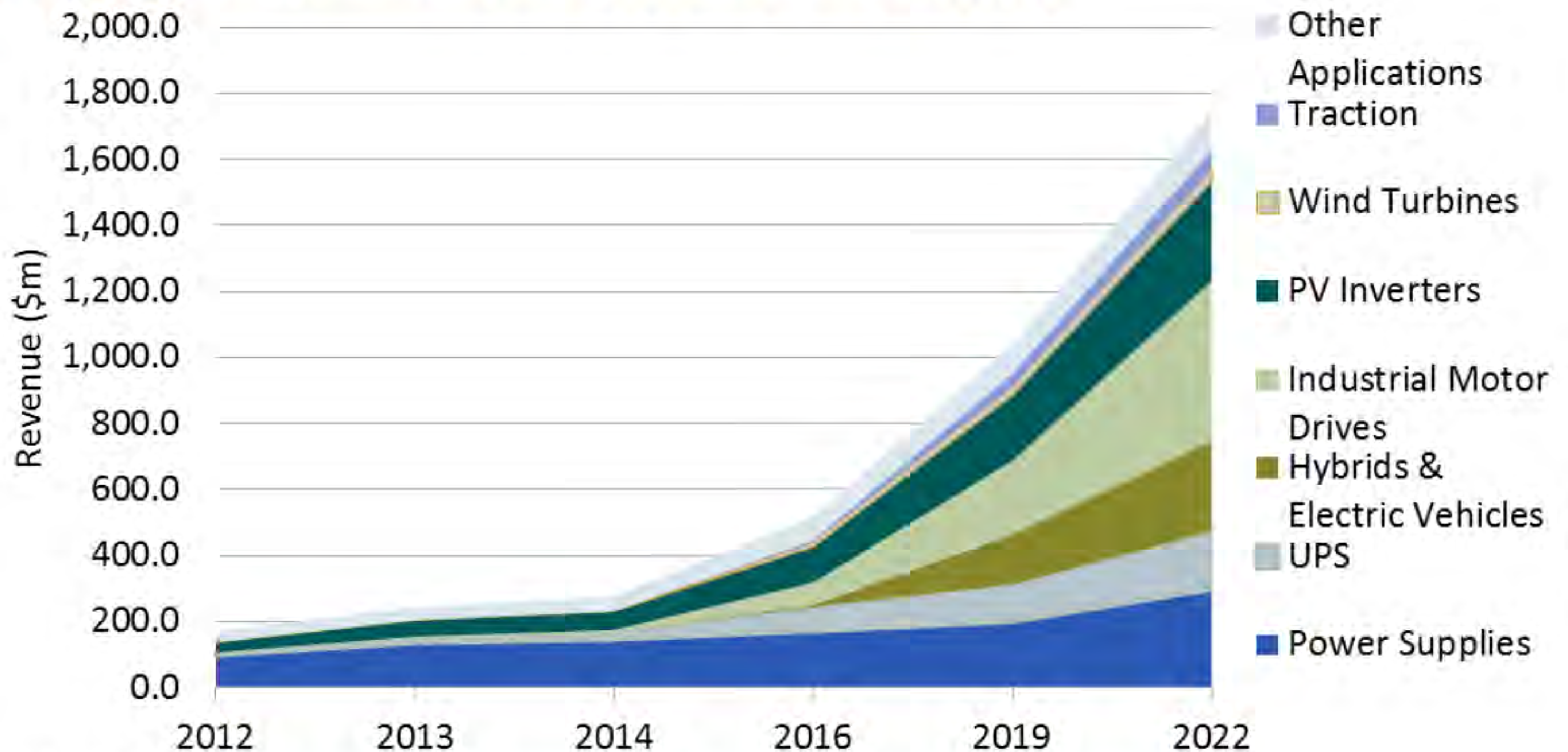
< 2006 2008 2010 2012 2014 2016 2018 > 2020

© 2010 · 10

SiC vs. Si Market

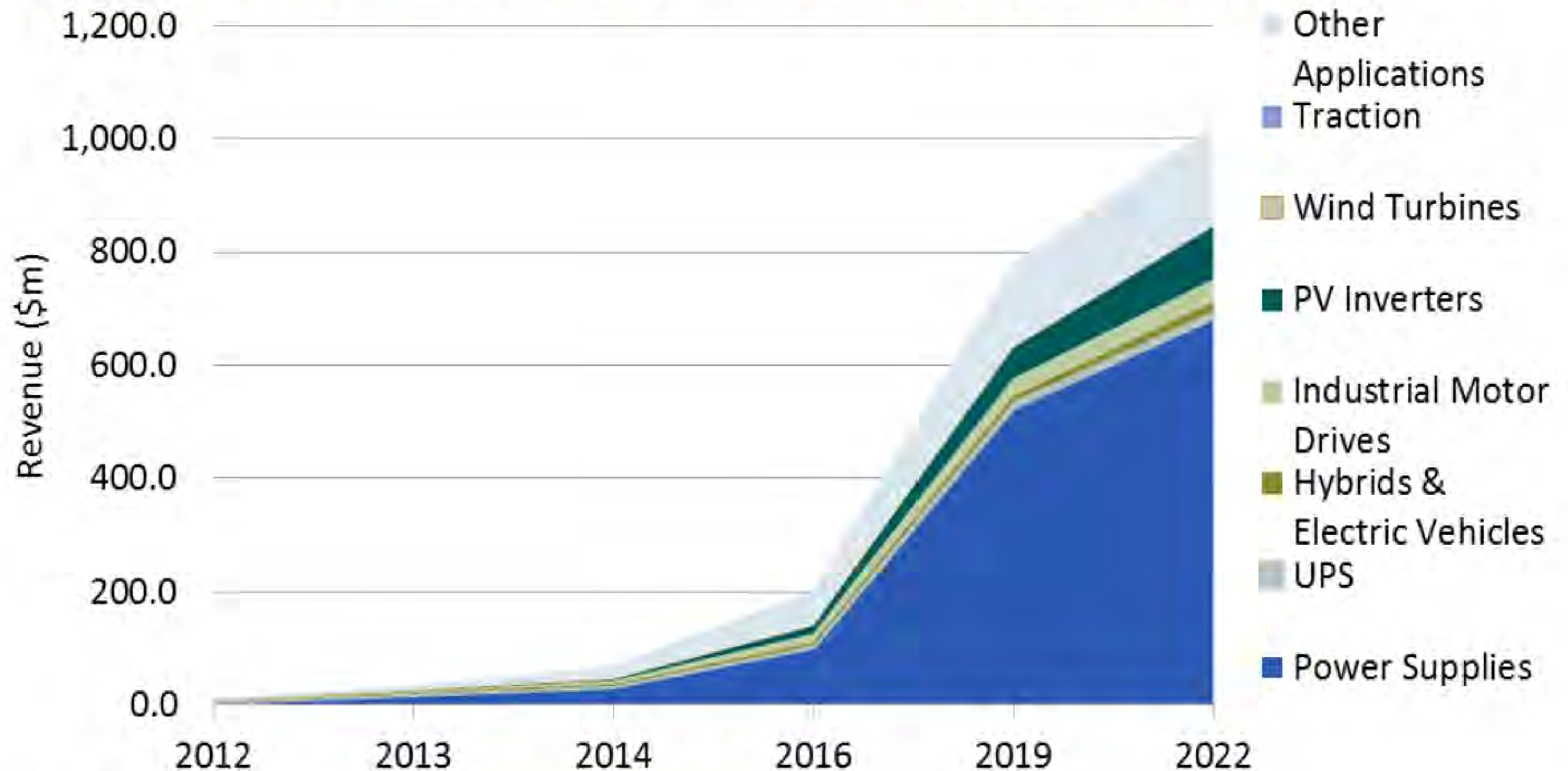
出所:APEC2010 Special presentation 1.2.3
Yole Development

SiC Power Semiconductor Market



Data Source:
The World Market for Silicon Carbide & Gallium Nitride Power Semiconductors – 2013

出所: APEC 2013 Industry Session 1.4.2 IMSresearch



出所: APEC 2013 Industry Session 1.4.2 IMSresearch

Conclusion (1/3)

Comparison of SiC and GaN device market size projection to 2020

SiC and GaN overlap in some applications. Typically, for EV/HEV, PV inverter or Motor Drives, the market can by indifferently fuelled by SiC or GaN. Thus, part of the market value could move from one to the other. So, these values are "as if XX technology would capture 100% of its market potential, with no competition from YY technology"

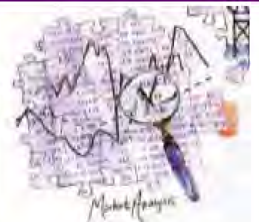
YOLE Développement

出所:SEMI Forum Japan June 14 2012
Yole Development

2012年時点での予測 (Yole Development)

Power Electronics

2011-2020 value-chain analysis: wafer, device, system



2011		2020
Electronics Systems	→	Electronics Systems
Power Inverters $41B	→	Power Inverters > $70B
Semiconductor power devices $17.7B	→ CAGR: +8.1%	Semiconductor power devices $35.7B
Power wafers	→	Power wafers

SiC playground

SiC： 930M$
GaN：1,900M$
Total：2,830M$
(8%)

YOLE DEVELOPPEMENT

出所:SEMI Forum Japan June 14 2012
Yole Development

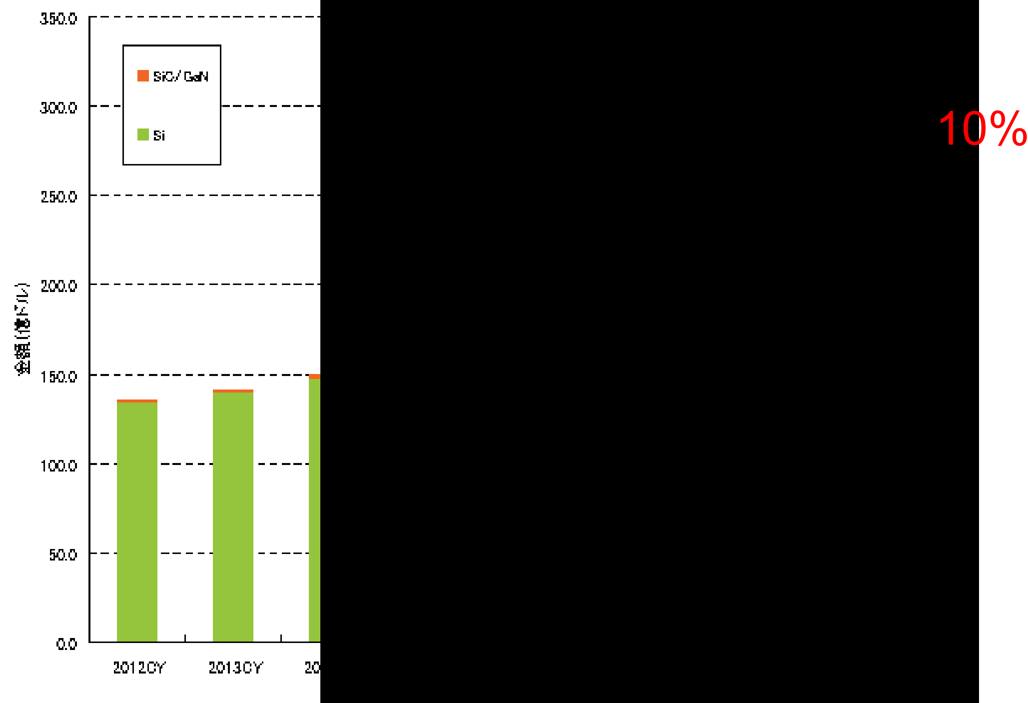
2013年矢野経済研究所

◆今後はパワーモジュールが市場を牽引し、2020年におけるパワー半導体の世界市場は**290億1,000 万ドル**と予測

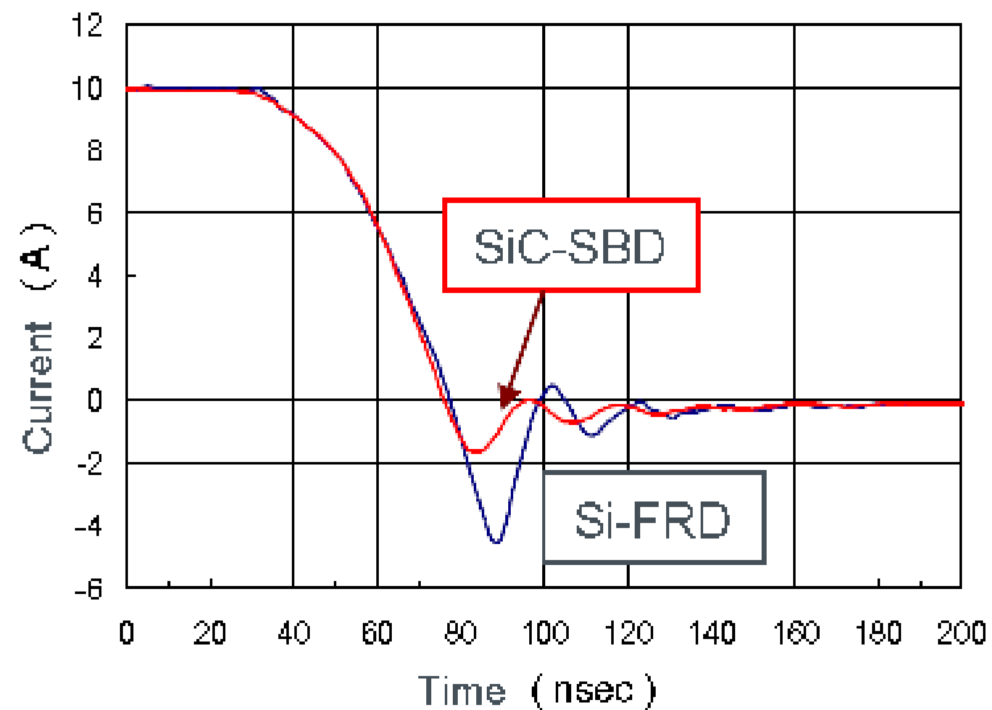
パワー半導体の世界市場は、2013年後半より回復基調に戻る可能性が高い。また、MOSFET、ダイオードなどのディスクリート品から、パワーモジュールに市場の牽引役が移り、2020年におけるパワー半導体の世界市場規模は290億1,000万ドル(メーカー出荷金額ベース)へ成長と予測する。

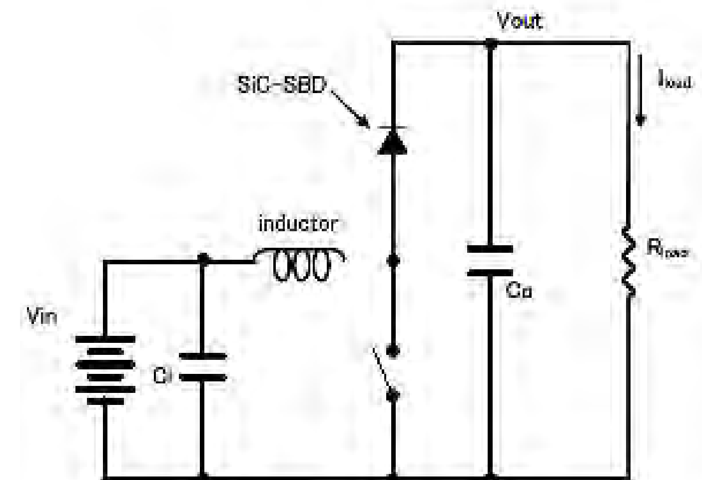
◆SiC、GaNなどを使った次世代パワー半導体世界市場は、2015年以降から本格的に採用拡大が進み、2020年の市場規模は**29億8,000万ドル**に達すると予測

Si(シリコン)よりも低損失、高速スイッチング、高耐熱性が実現可能なSiC(シリコンカーバイド)、GaN(ガリウムナイトライド)を使った次世代パワー半導体は、これまで一部用途に搭載機器は限定されていたが、コストダウンの進む2015年以降から各需要分野での採用が拡大、本格的に市場が立ち上がる。2020年におけるSiC、GaNパワー半導体の世界市場規模は29億8,000万ドル(メーカー出荷金額ベース)と予測する。



600V SiC Schottky Diode（SBD）



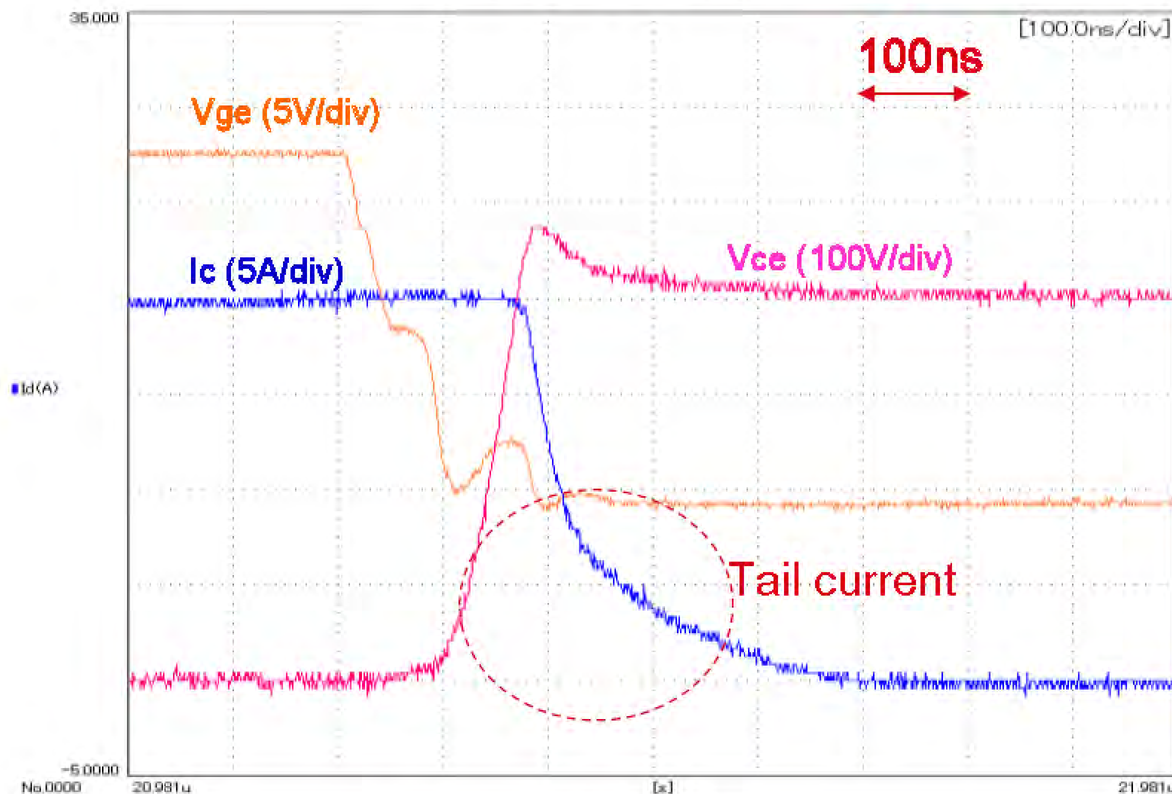


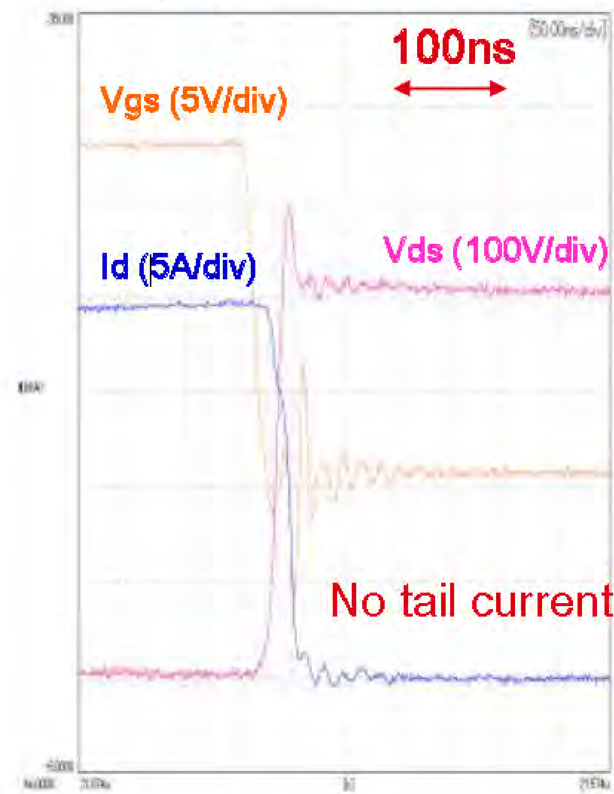
出所: APEC 2013 Industry Session 1.4.1 Rohm

1200V 15A (IGBT+FRD)

Vgs=+18V/0V
Rg external =5.6ohm

SCH2080KE (SiC-MOS+SBD)



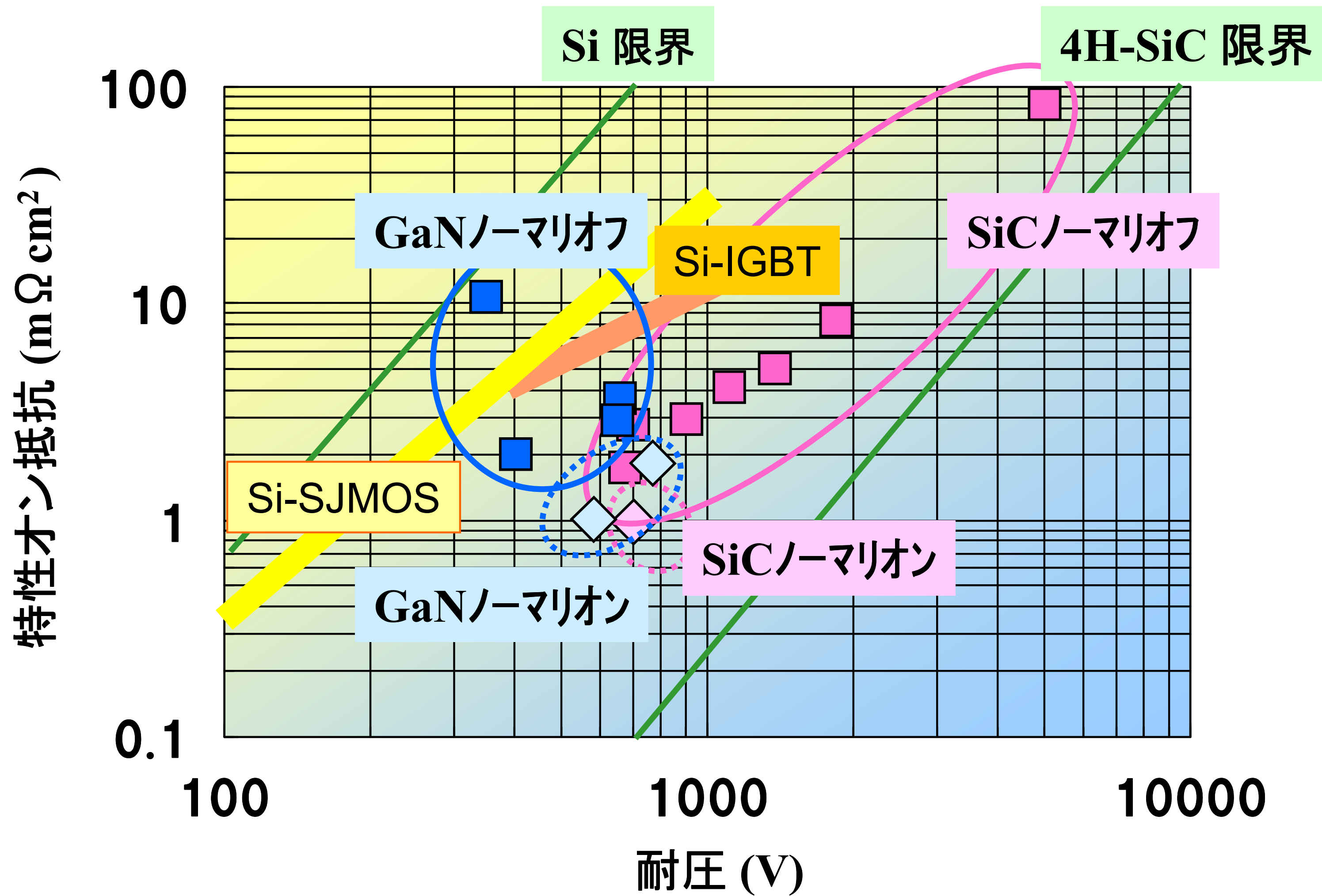


Eoff=890.2uJ

Eoff=109uJ

出所: APEC 2013 Industry Session 1.4.1 Rohm

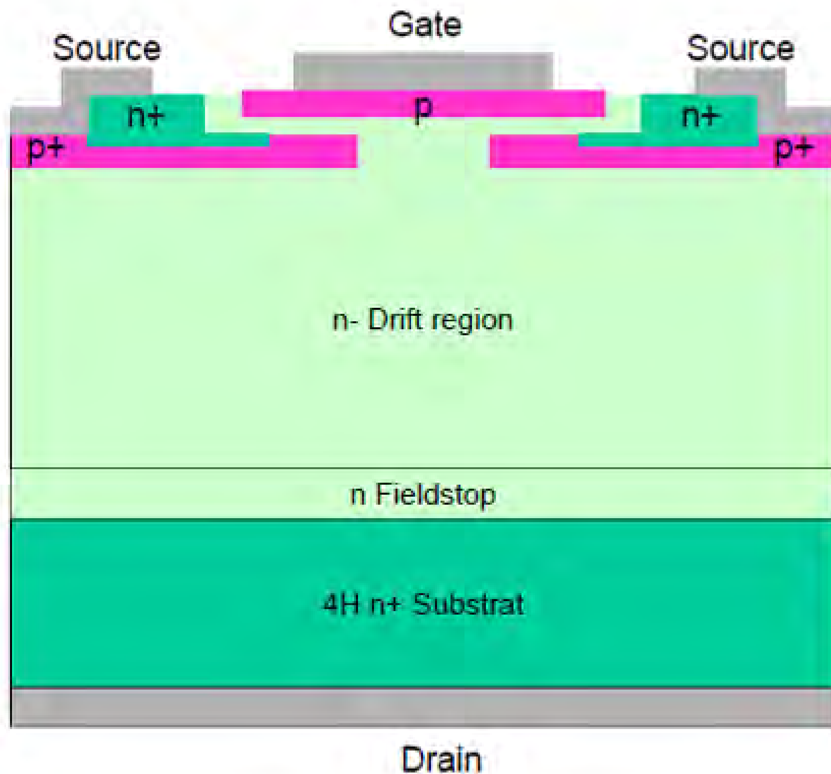
SiC, GaNスイッチング素子のベンチマーク

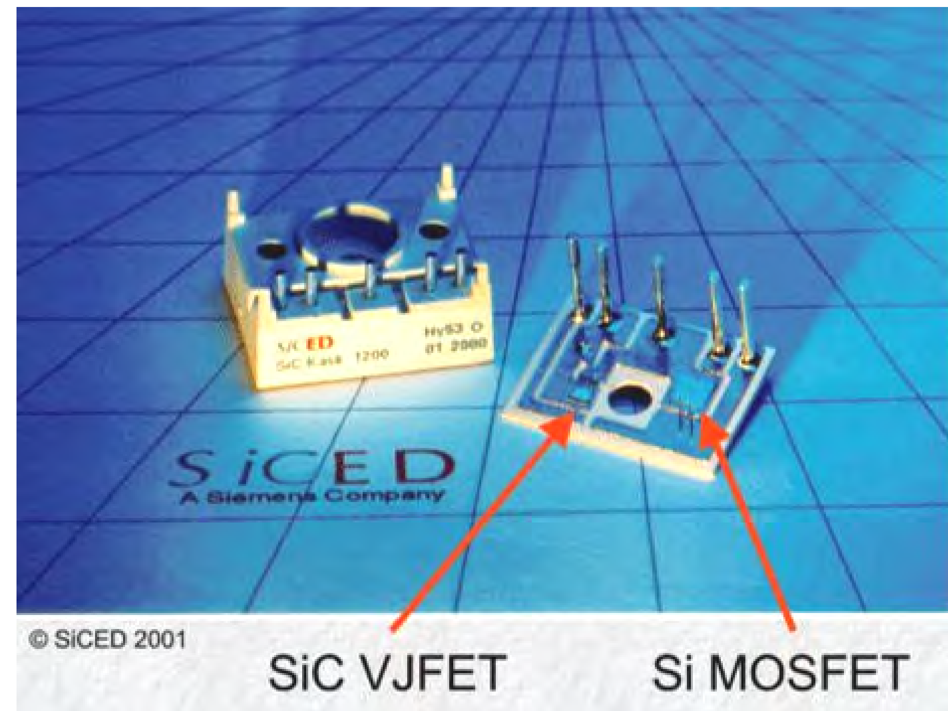


SiC JFET

Sourceが埋め込み層と接続されている

SiCED (ICSCRM'99他)





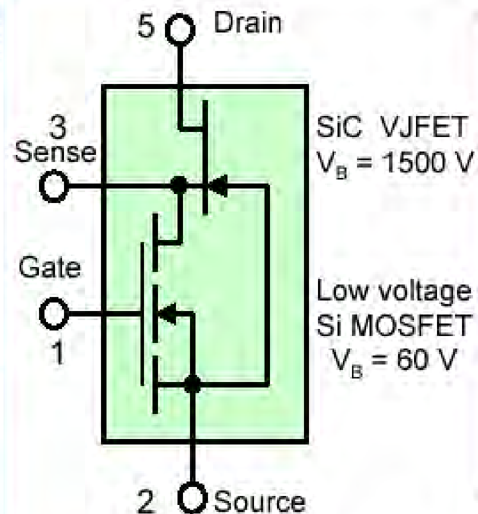
1800V-14.5mΩcm^2 ,3500V-25mΩcm^2

SiCED社資料から引用

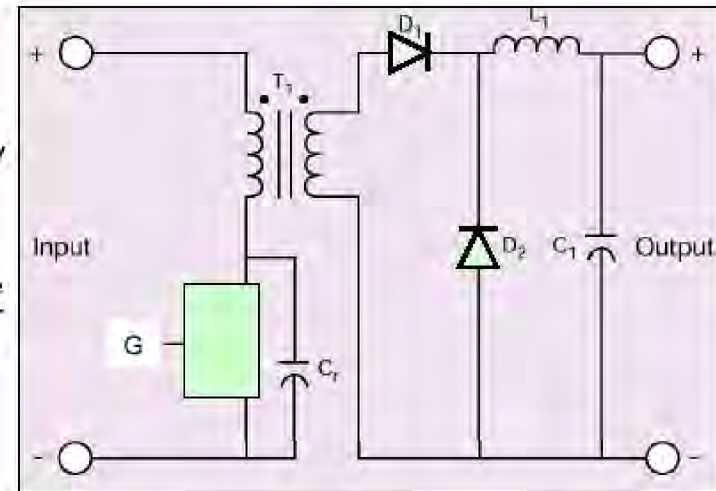
SiC-JFET + Si-MOSFET

Hybrid SiC/Si Cascode　SiCED

The Hybrid SiC/Si Cascode Electronic Switch Aiming at Market Entry 2004



Circuit Diagram



Resonant Reset Forward Converter

- significant increase of power limit for single switch solutions (up to 2 kW)
- simplicity in control
- efficient transformer utilization
- size reduction

- 15 mΩcm² specific on-resistance (25°C)
- High short circuit capability (>200 µs)
- Power almost totally at SiC VJFET
- High T_J capability (175°C)

Other fields of utilization are: auxiliary power supplies, UPS, high speed inverters

SiCED社資料から引用

IEMOS (Implantation & Epitaxial MOSFET)

エピタキシャル面上にMOSチャネル

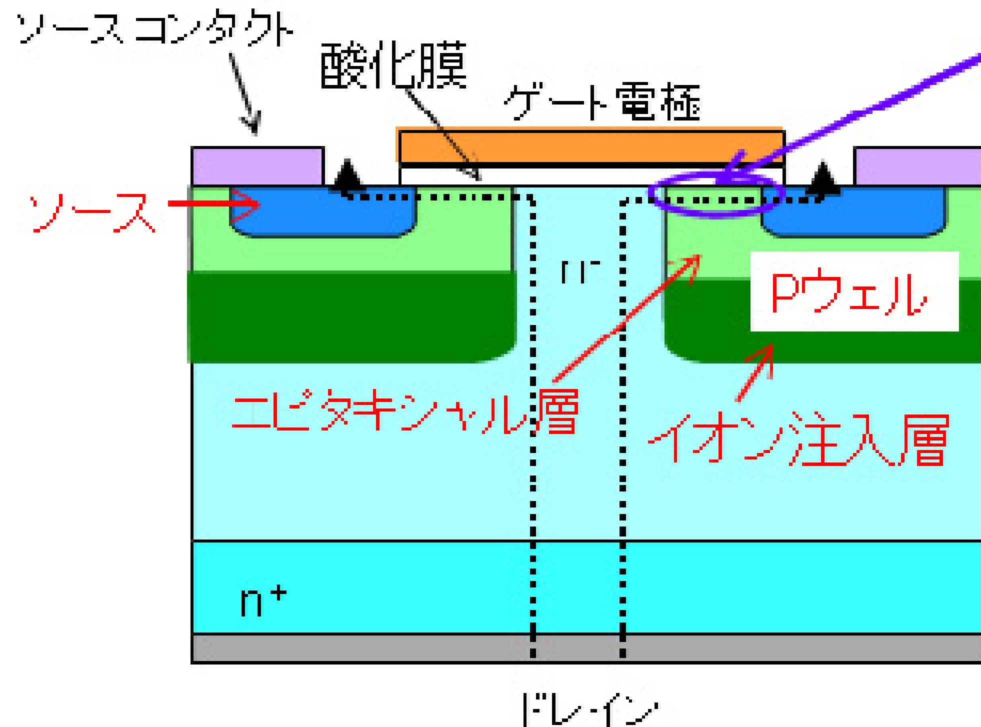


図5　今回開発した、4H-Sic-IEMOS
(Implantation & Epitaxial MOSFET)

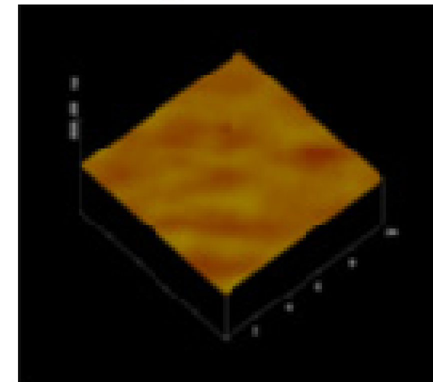


図6　原子間力顕微鏡で測定されたエピタキシャル層で形成されたPウエル表面
アルミニウムはエピタキシャル成長中に導入されるので、1600℃以上の熱処理は必要なく表面は平滑であり、電流が流れやすいので、オン抵抗が下がる。

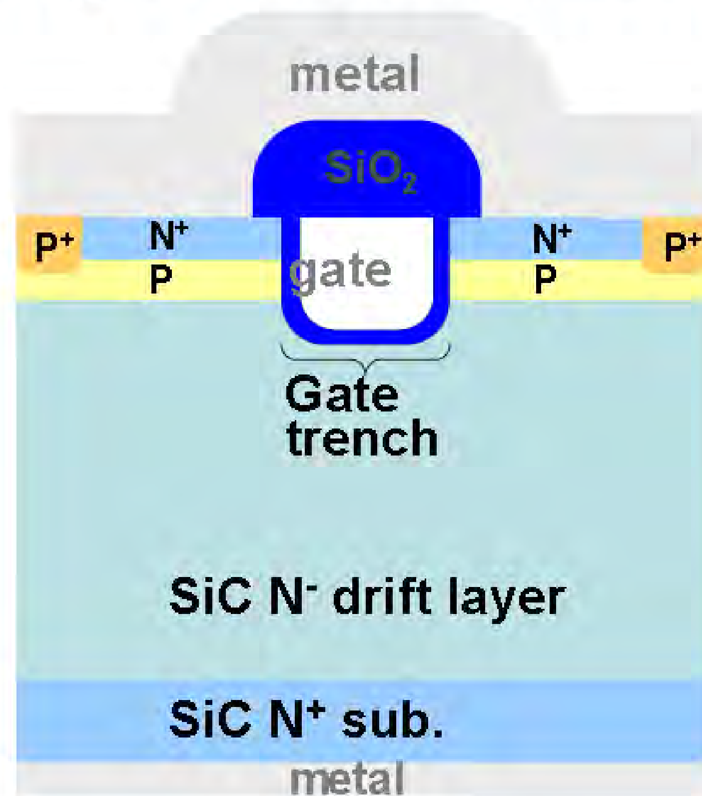
産総研 (応物全国大会'05/3、ISPSD'07)

耐圧1100V, 特性オン抵抗4.3mΩcm²、C面では660V, 1.8mΩcm²

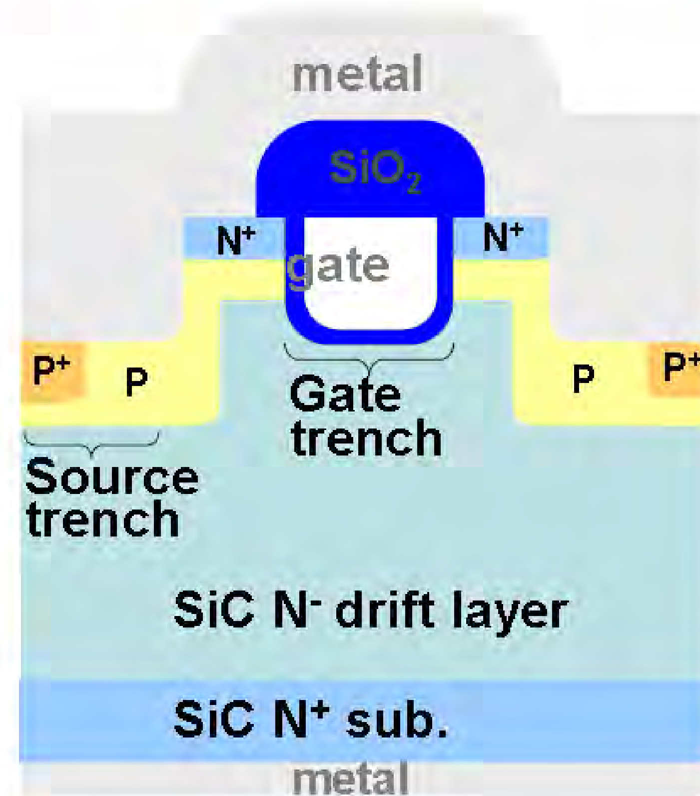
産総研プレス発表資料から引用

Schematic of the SiC double trench MOSFET

Conventional structure (single trench structure)

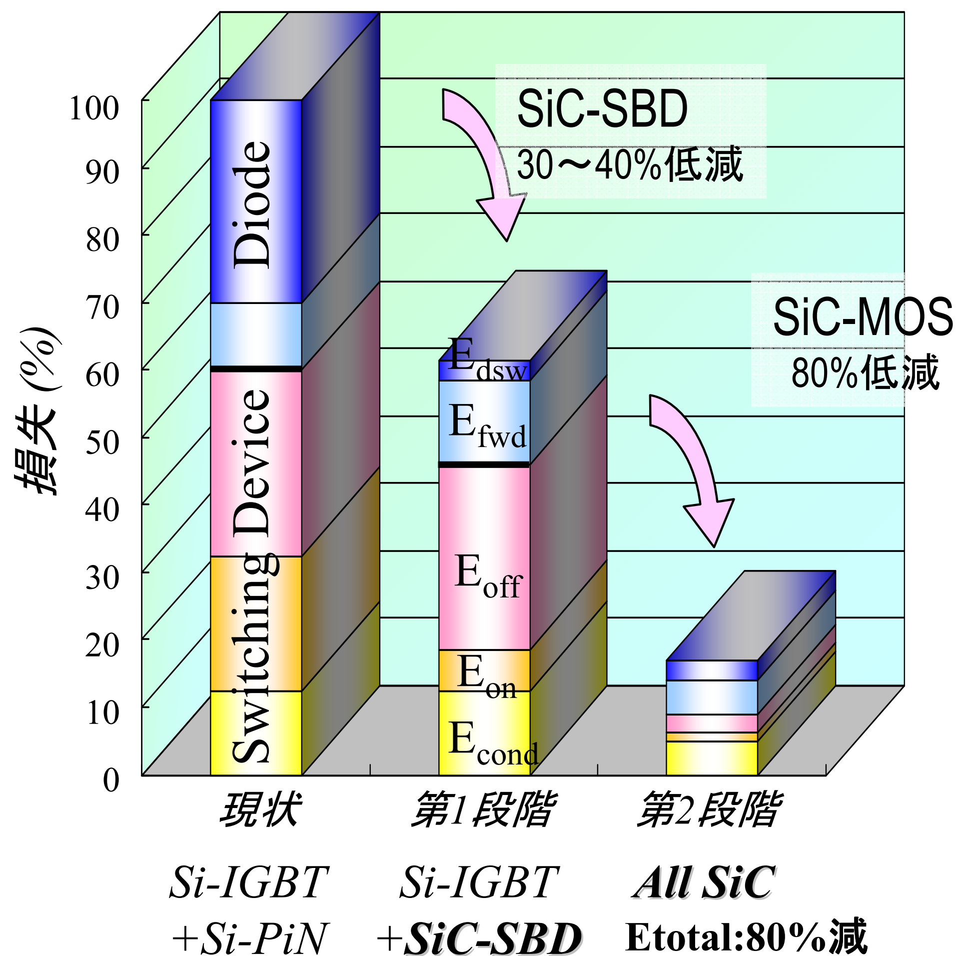


Double trench structure

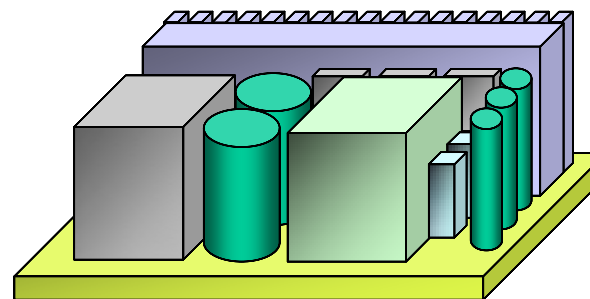


出所: APEC 2013 Industry Session 1.4.1 Rohm

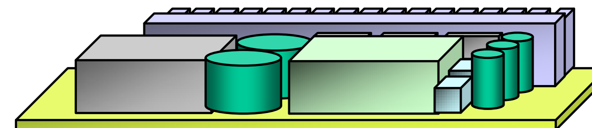
システムへの適用効果：低損失化と小型化



電源の小型化（体積1/5）

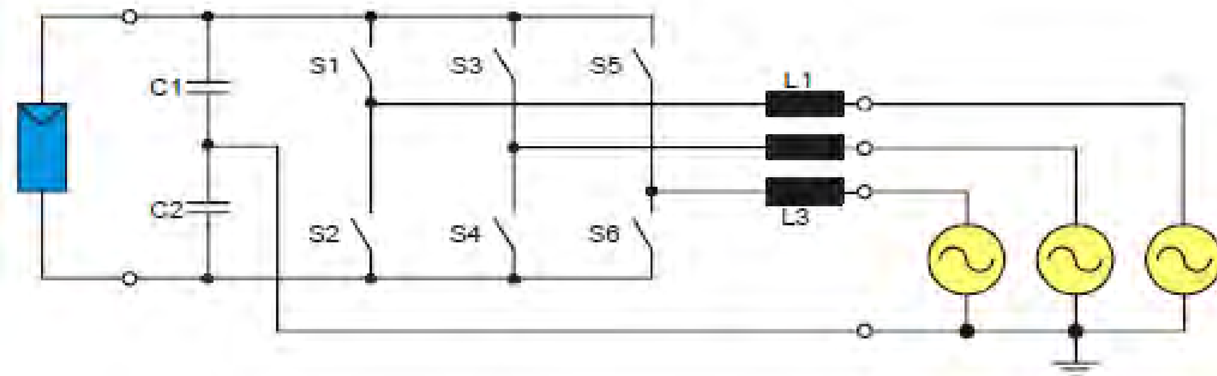


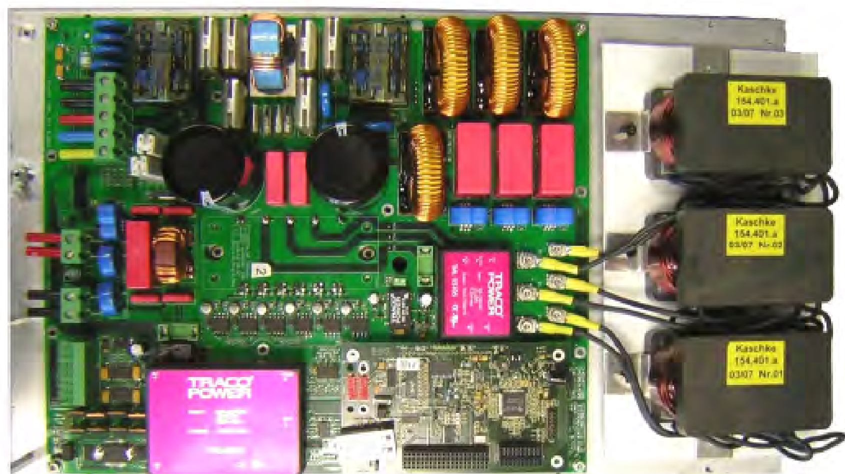
低損失化・高温動作（冷却フィン小型化）
高周波化（受動部品小型化）

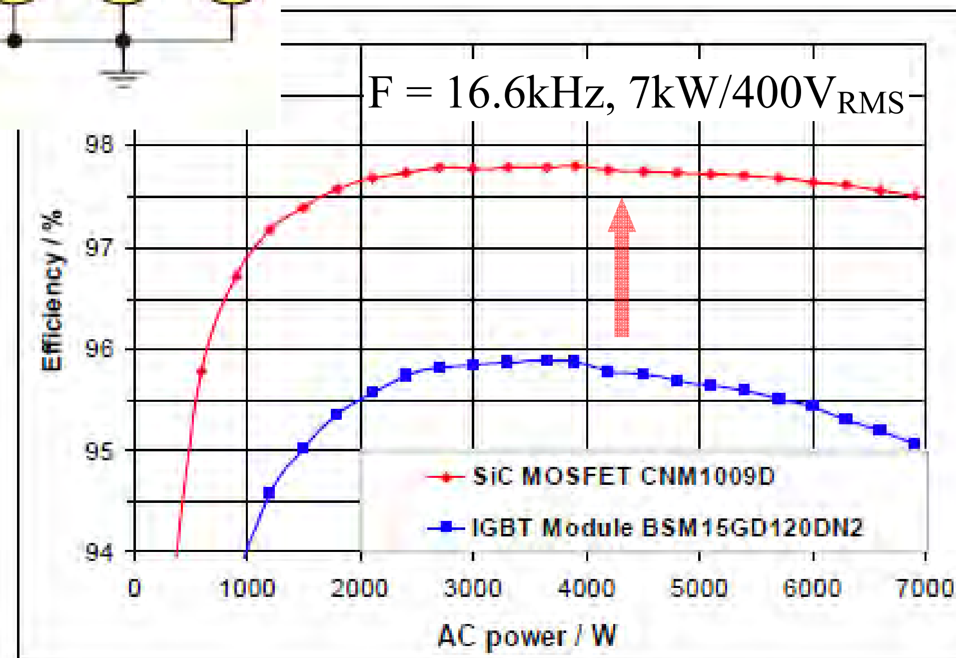


太陽光インバータ

三相インバータ



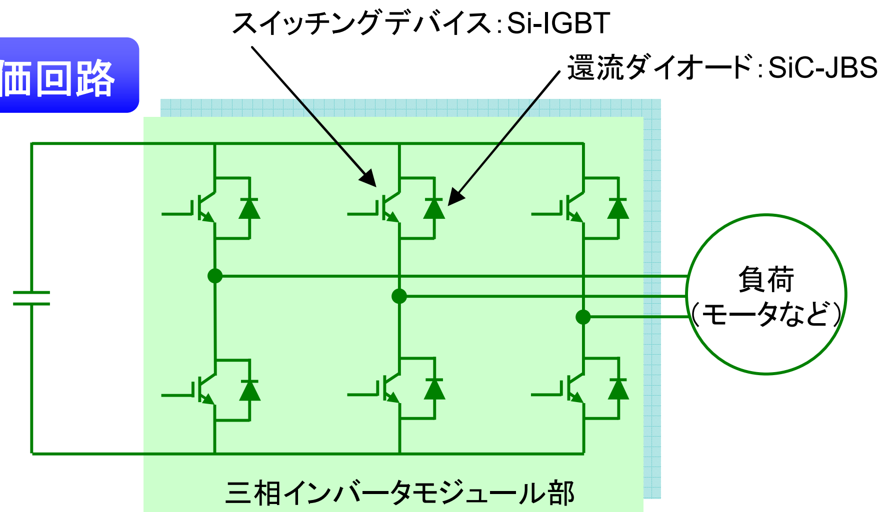


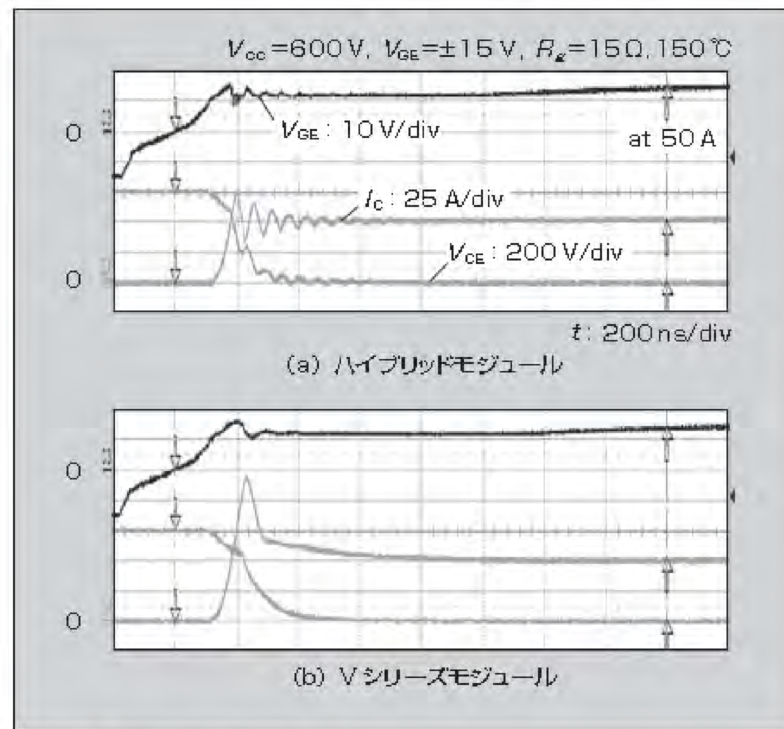


1200V10A SiC-MOSFET + 内蔵diode 効率 **97.8%**、heatsink温度=50℃
1200V15A Si-IGBT + Si PiN diode　効率 **95.9%**、heatsink温度=93℃

ICSCRM'07でのFraunhoferの発表から引用

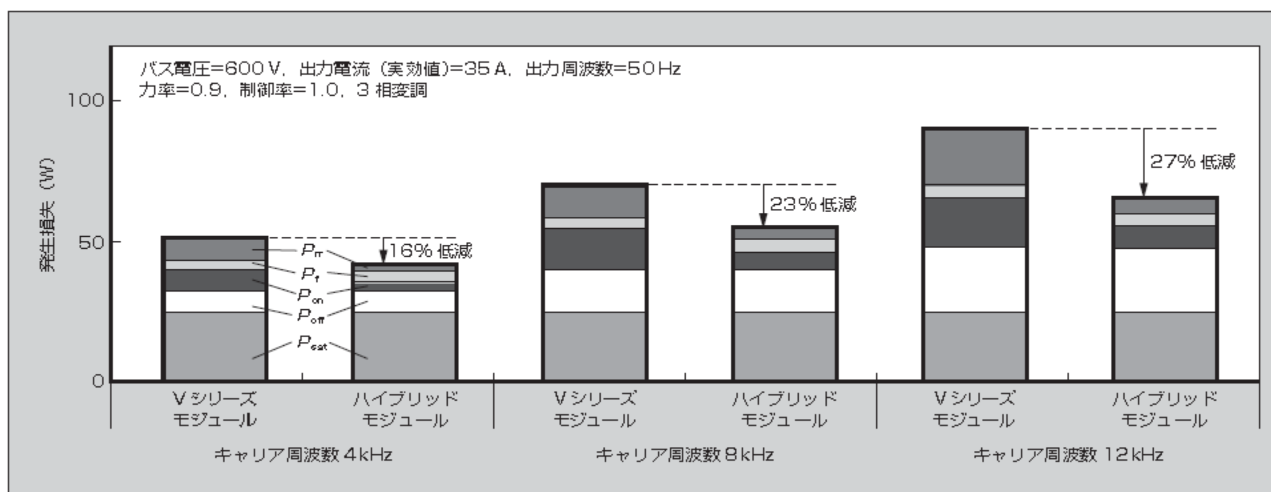
ハイブリッドペアインバータ





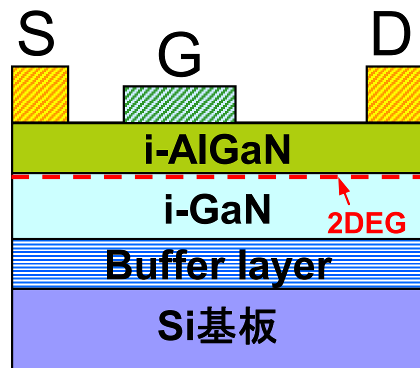
ターンオン波形

ダイオードの置き換えだけで
インバータ損失を30%低減可能

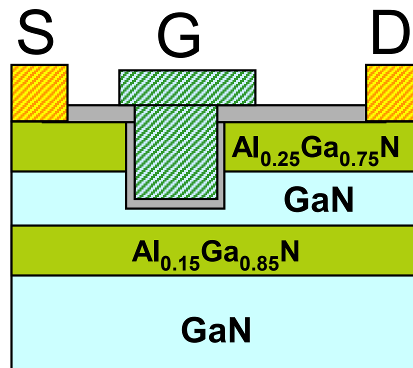


インバータ発生損失

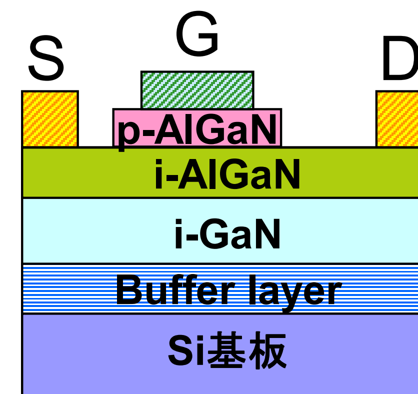
GaNトランジスタの各種素子構造



GaN-HEMTの基本構造



リセスMISゲート4層構造



GIT: Gate Injection Transistor

◆ ノーマリオフ報告例

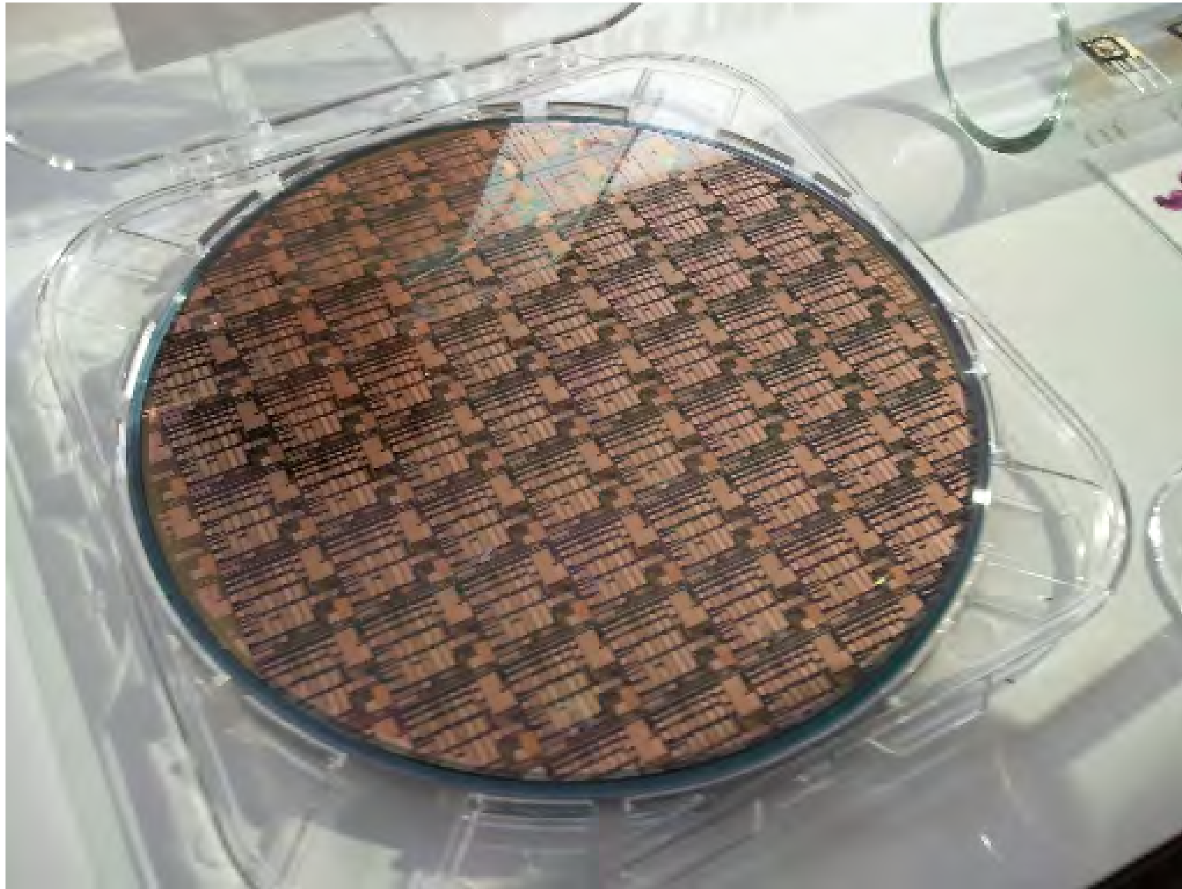
リセスMISゲート4層構造：640V, 3.5mΩcm^2, Vth=0.2～0.4V
GIT（Gate Injection Transistor）：800V, 2.6mΩcm^2, Vth=1V

◆ 課題

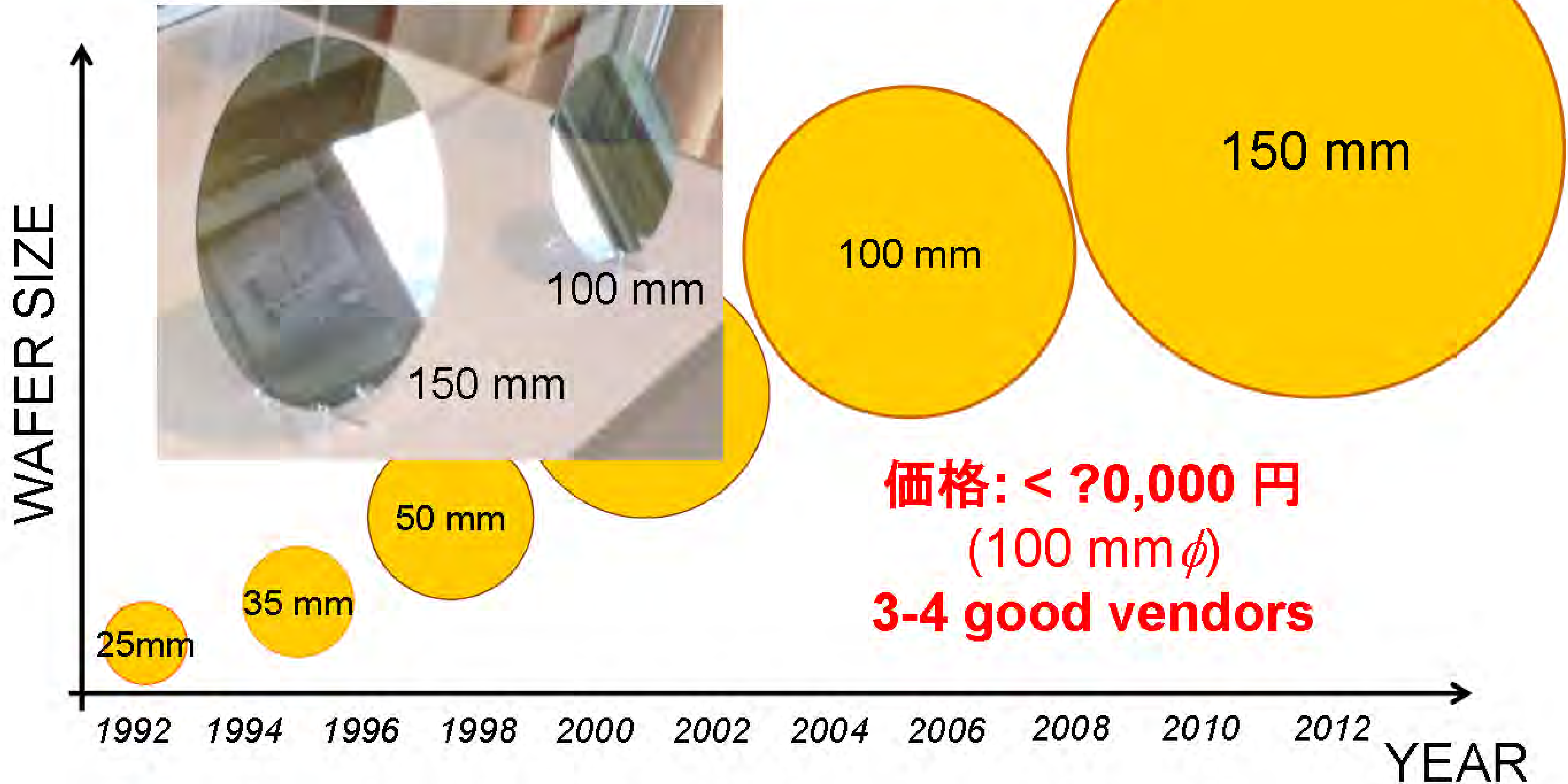
電流コラプス
GaN on Siエピの品質向上、GaN基板開発
ノーマリオフ化（Vth～3V）
長期信頼性、アバランシェ耐量の確認と対策

６インチGaN on Si基板

Au-free CMOS-compatible AlGaN/GaN HEMT（**IMEC**）



SiCウェーハの進展

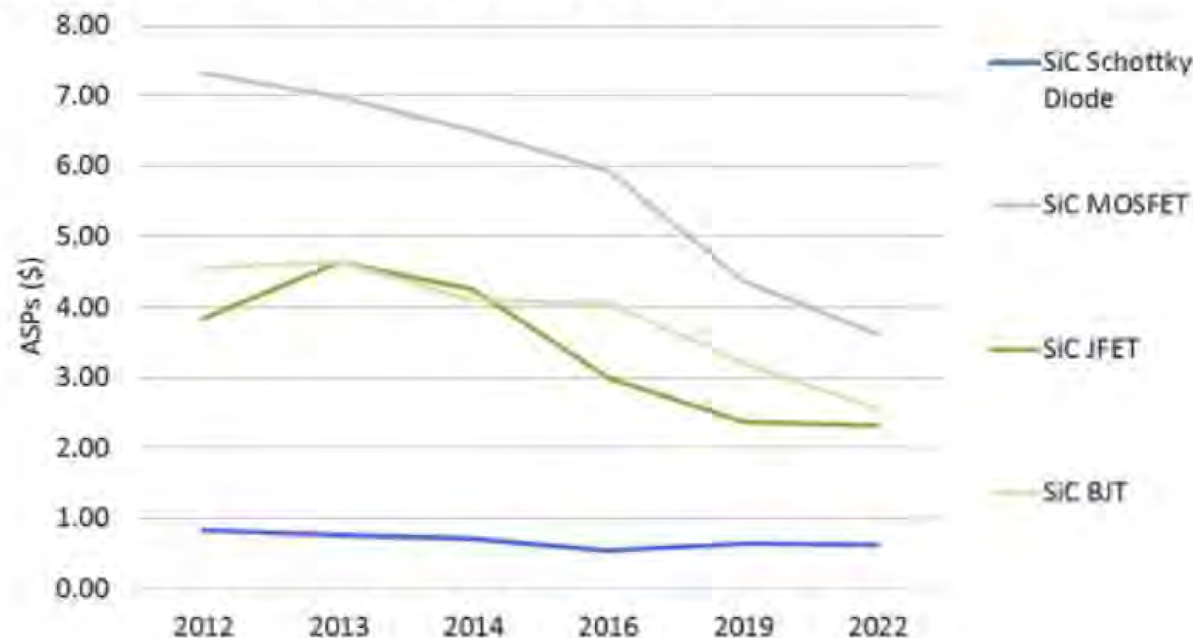


出所 2012. 7. 9窒化物半導体応用研究会 木本先生

SiC素子のコストは2020年でも現在の1/2 High ENDにしか使えない？

SiC Device price trends

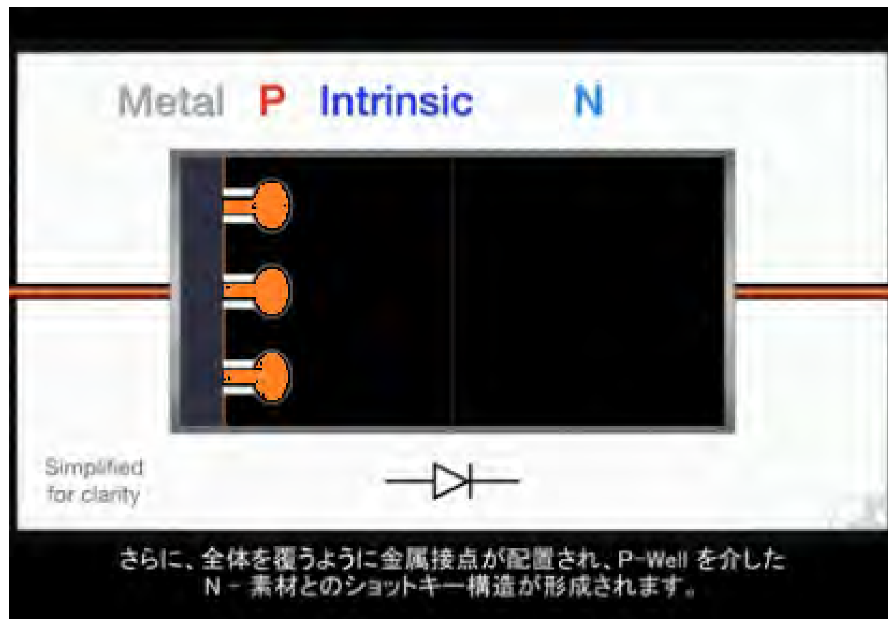
- SiC Diodes currently cost x5 – x7 Silicon Schottky Diodes
- SiC JFETs cost x4 – x7 Silicon MOSFETs
- SiC MOSFETs cost x10 – x15 Silicon MOSFETs

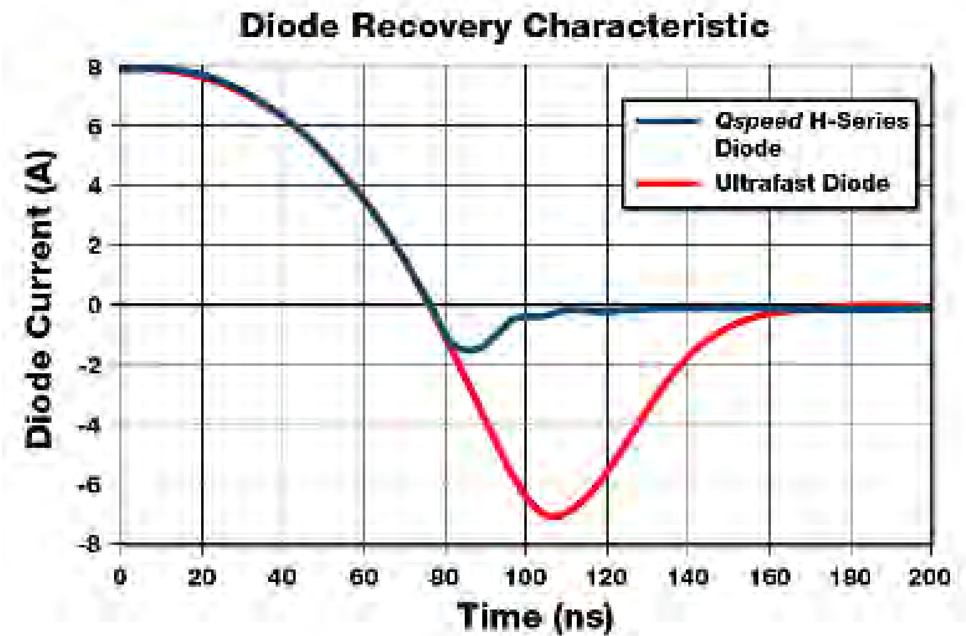


Data Source:
The World Market for Silicon Carbide & Gallium Nitride Power Semiconductors – 2013

出所: APEC 2013 Industry Session 1.4.2 IMSresearch

SiC並のシリコン高速ダイオード QSPEED





出所: http://www.powerint.com/qspeed

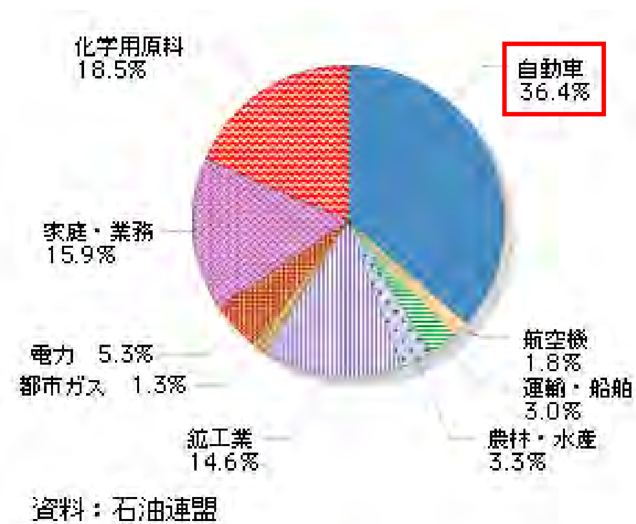
2020年で90%は依然シリコン!!

電力の需給バランスは逼迫し、地球温暖化からエネルギー消費抑制

省エネ、再生可能エネルギーがキー技術

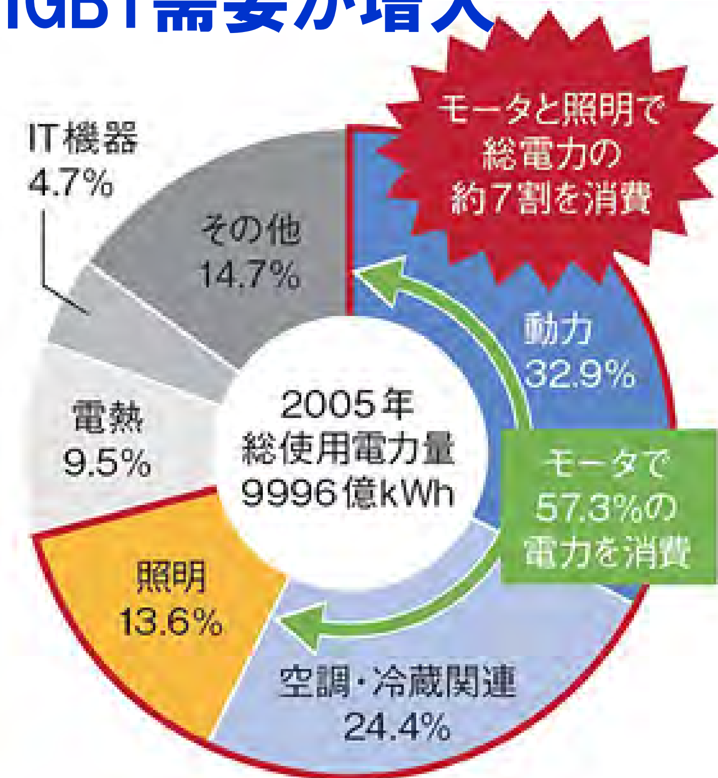
低コスト省エネ(インバータ)家電、EV/HEVが重要

IGBTは2極化(SiCと低コストSi)、Si-IGBT需要が増大



石油製品の用途別需要量

(エネルギー白書2004)



日経エレクトロニクス2011年5月2日号)

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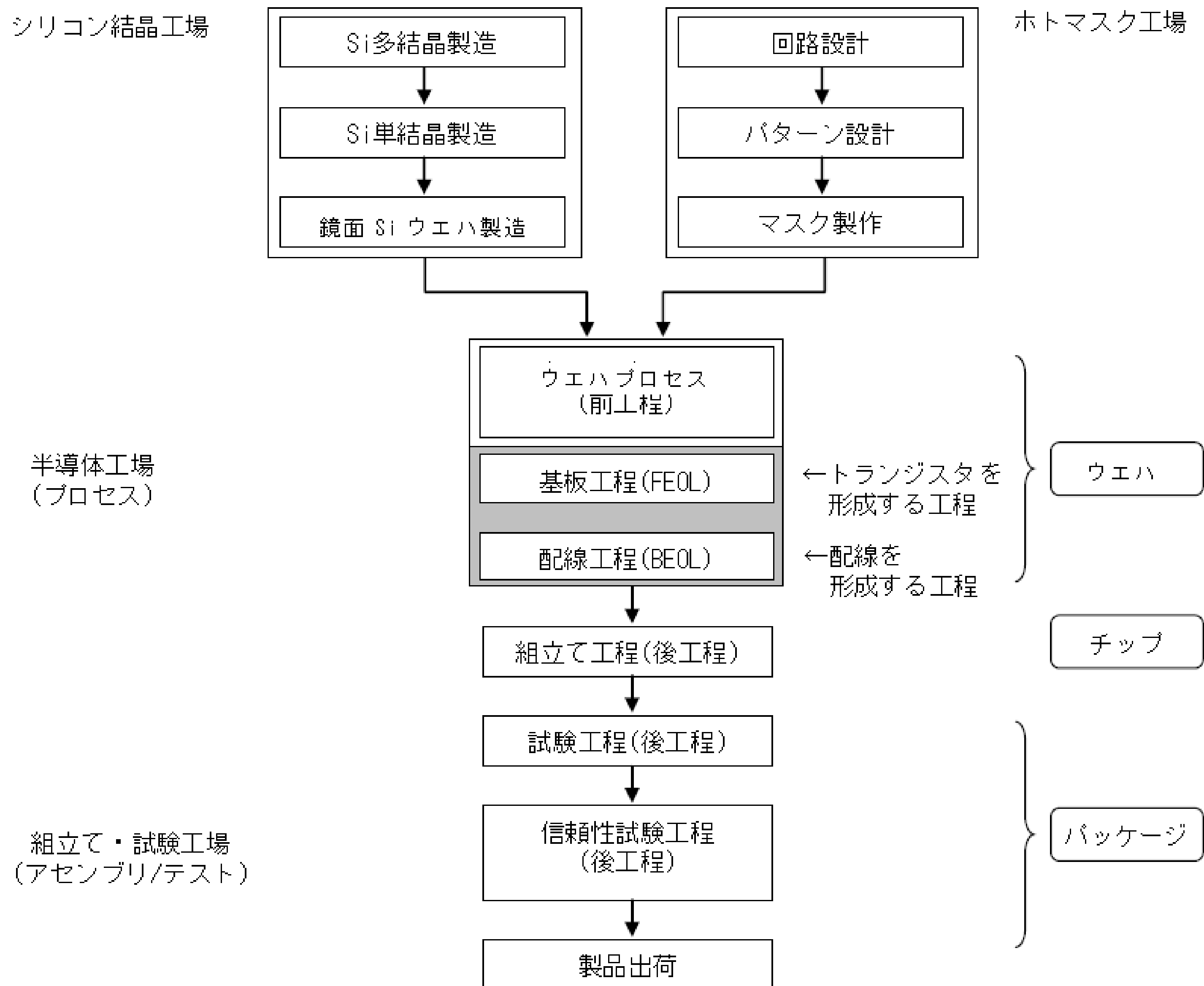
シリコンパワーデバイスの製法



出典：前田和夫、はじめての半導体プロセス、技術評論社、2011 年 8 月

LSIプロセスとSiパワーデバイスプロセスの違い

１．パワーデバイスの製造装置はLSI製造装置と
　　基本的に変わらない。

（写真・エッチング・インプラ・アニール・酸化膜炉・CVD・スパッタ）

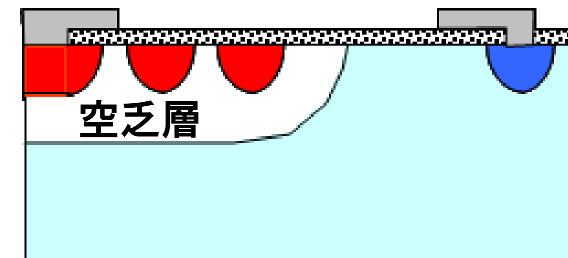
２．LSI製造との違い：縦に電流を流す構造

FZウェーハ、薄いウェハ、ライフタイム制御が重要

パワーデバイス特有のプロセス技術

１．終端技術およびパシベーション技術

高耐圧を確保



２．ライフタイム制御技術

高速スイッチングタイム

３．トレンチ技術

順方向電圧ドロップ改善

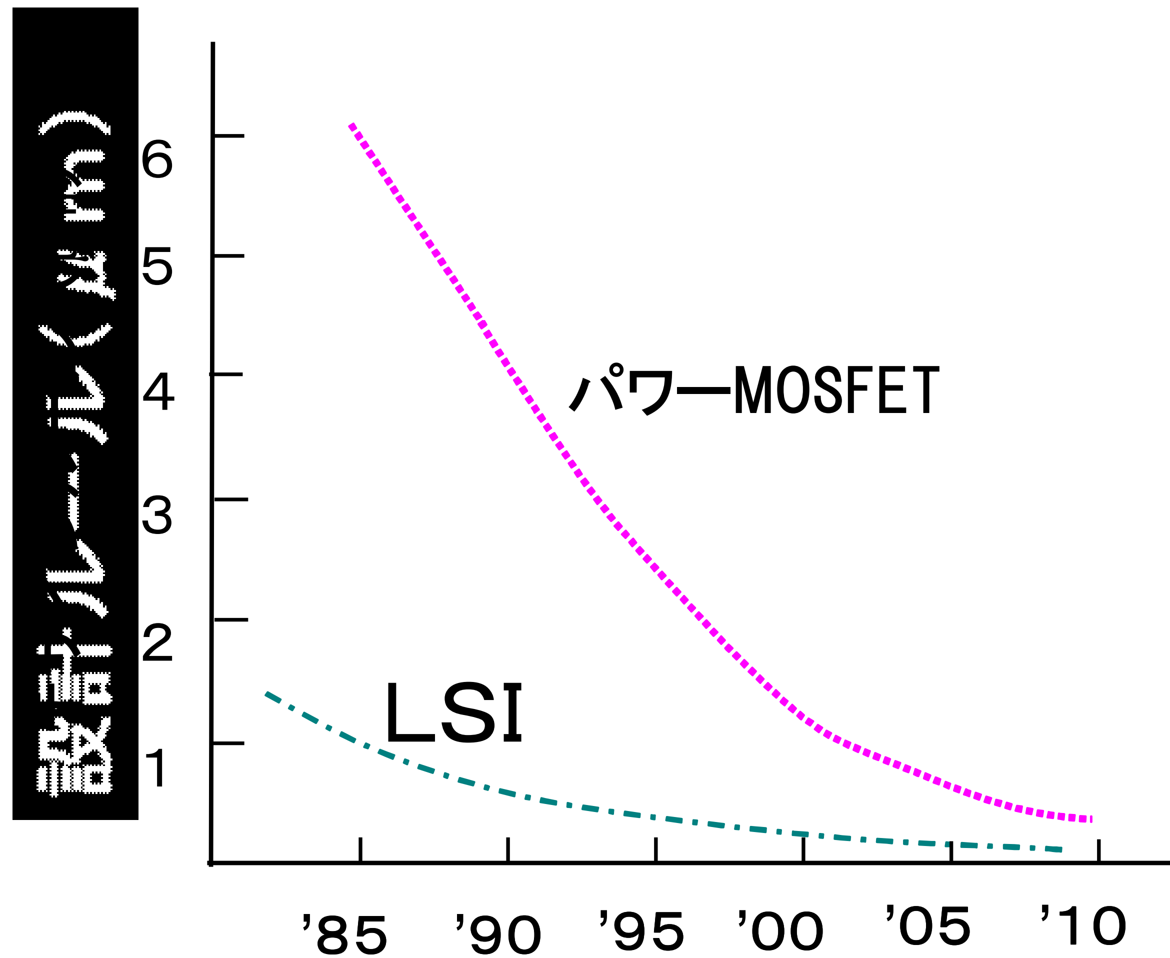
４．微細加工技術

順方向電圧ドロップ改善

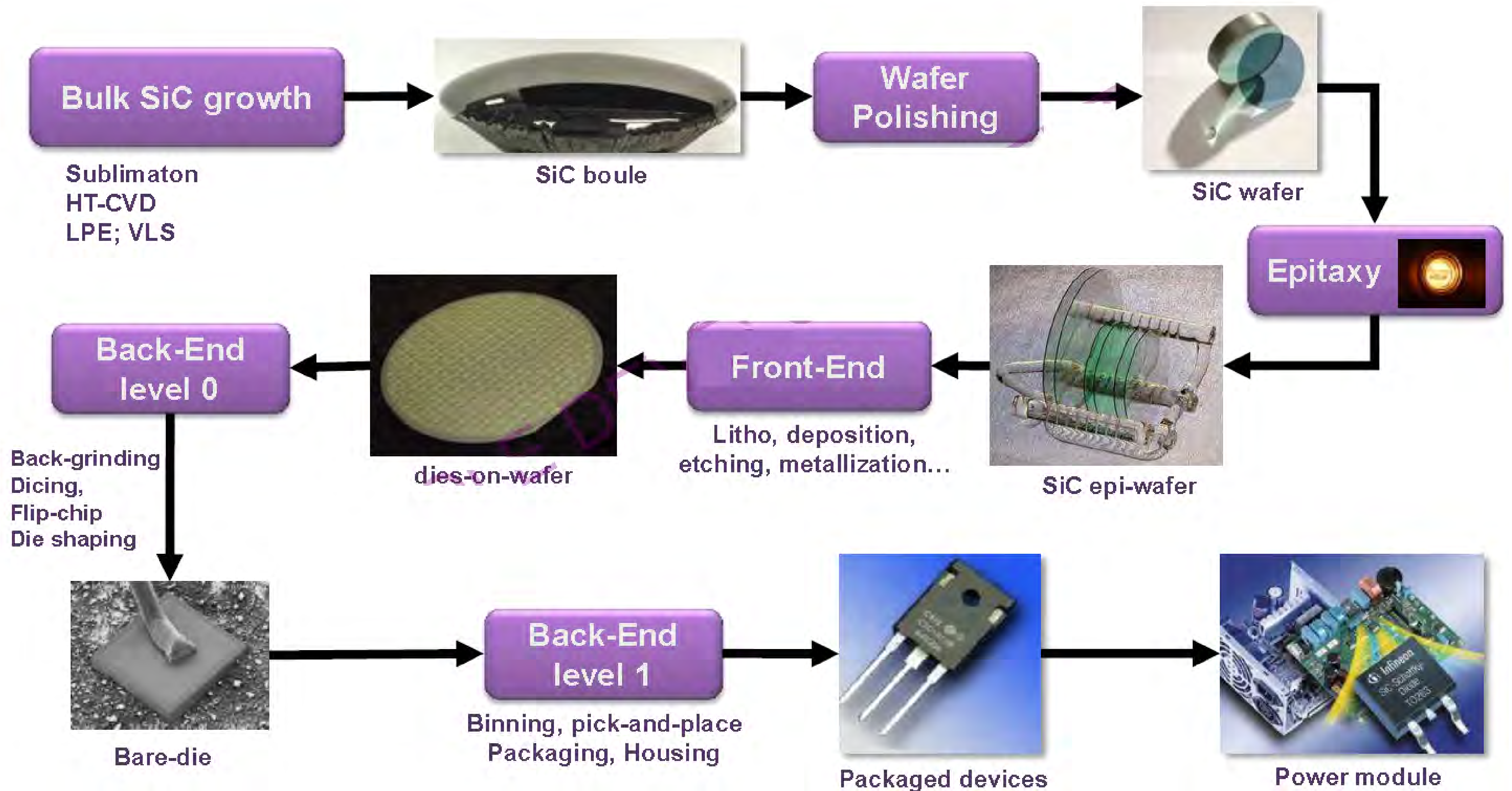
５．薄ウェハ技術

特性改善、基板抵抗低減

設計ルールの変遷



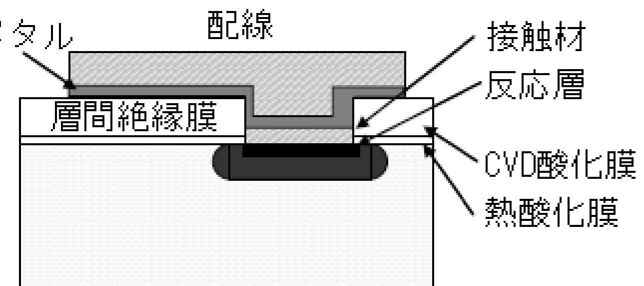
SiC結晶からインバータの製造工程



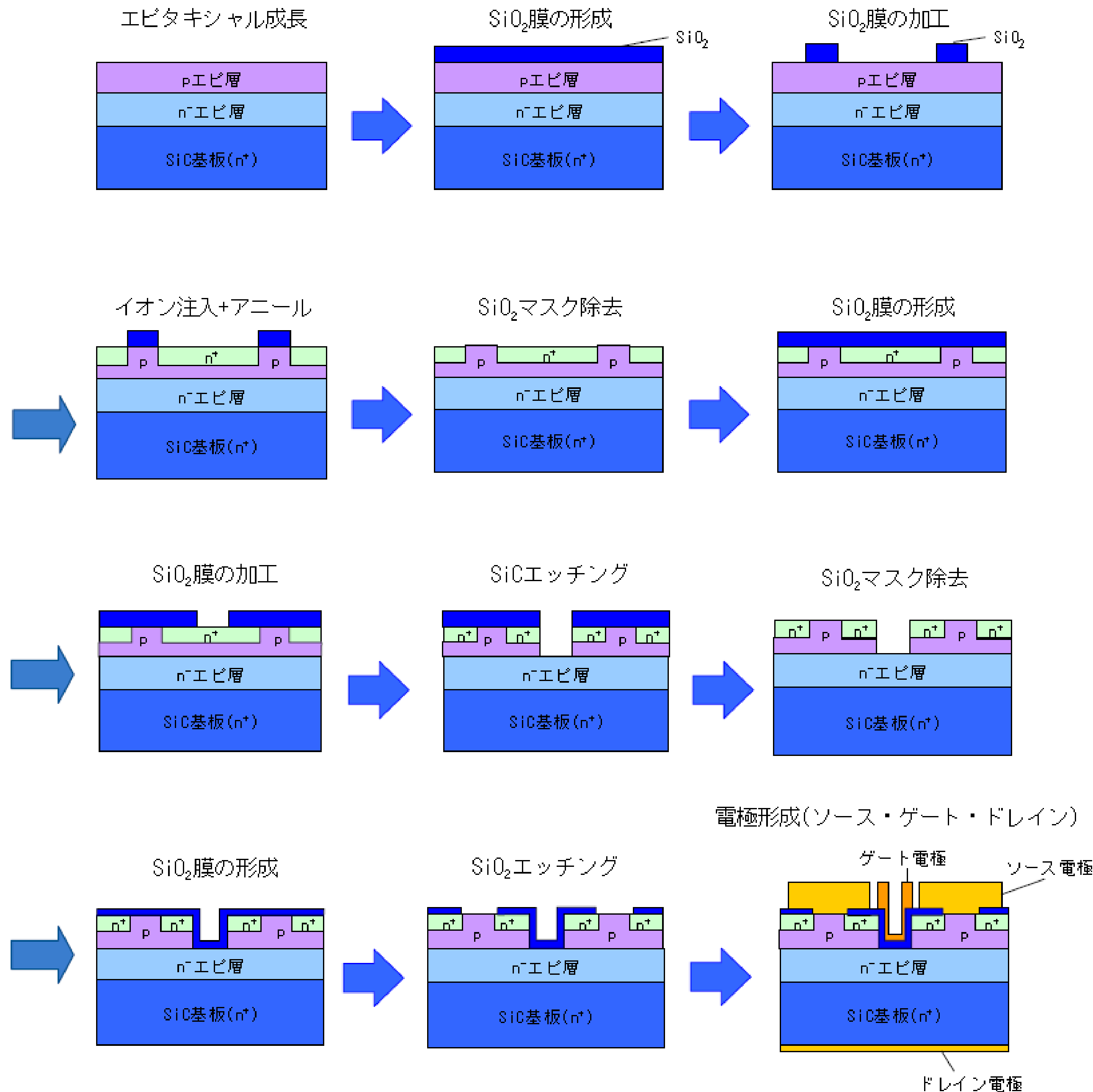
出所:SEMI Forum Japan June 14 2012
Yole Development

SiCプロセスの特徴と課題

1. 昇華法による結晶成長…結晶欠陥が多く欠陥低減、大口径化とコスト低減が課題
2. 不純物拡散が困難なのでエピ成長、イオン注入が用いられる。
3. イオン注入：結晶欠陥低減のため1500~1800度の高温イオン注入が用いられる。
4. エッチング；プラズマエッチングが主体
5. 酸化：シリコン同様に熱酸化可能。ゲート酸化膜としては移動度向上と界面電荷制御が課題
6. 電極：1000度高温で急速熱処理が必要で
   ｎ型層にNi、ｐ型層にAl・Ti合金



SiC MOSFETの製造プロセスの例



出所: http://www.samco.co.jp/products/app/05_power.php

S

製造プロセス	
材料技術	基板技術
	エピタキシャル成長技術
プロセス技術	イオン注入技術
	ゲート形成技術
	電極形成技術
	ダイシング技術
実装技術	

出典：住化分析セン

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まとめ

１．パワーデバイスは、ＩＧＢＴを筆頭として、省エネ化の流れに乗り、市場を拡大している。

２．ＩＧＢＴはハイブリッド車、太陽電池、新幹線等の大電力インバータ回路用の主スイッチデバイス。パワーＭＯＳＦＥＴは電源やモータの主スイッチデバイスである。（ＩＧＢＴより小電流の用途）

３．ＩＧＢＴとパワーＭＯＳＦＥＴの概要を紹介した。

４．パワーデバイスに特徴的な製造プロセスを示した。

５．ＳｉＣやGaNはパワーデバイスとしての優れた材料であり、高耐圧パワーデバイスの性能を格段に向上できる。