シリコンパワー素子IGBTの現状と未来

中川 明夫
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   特許から見たIGBTの定義

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3. IGBTのシリコン限界に向けた
   今後の展開

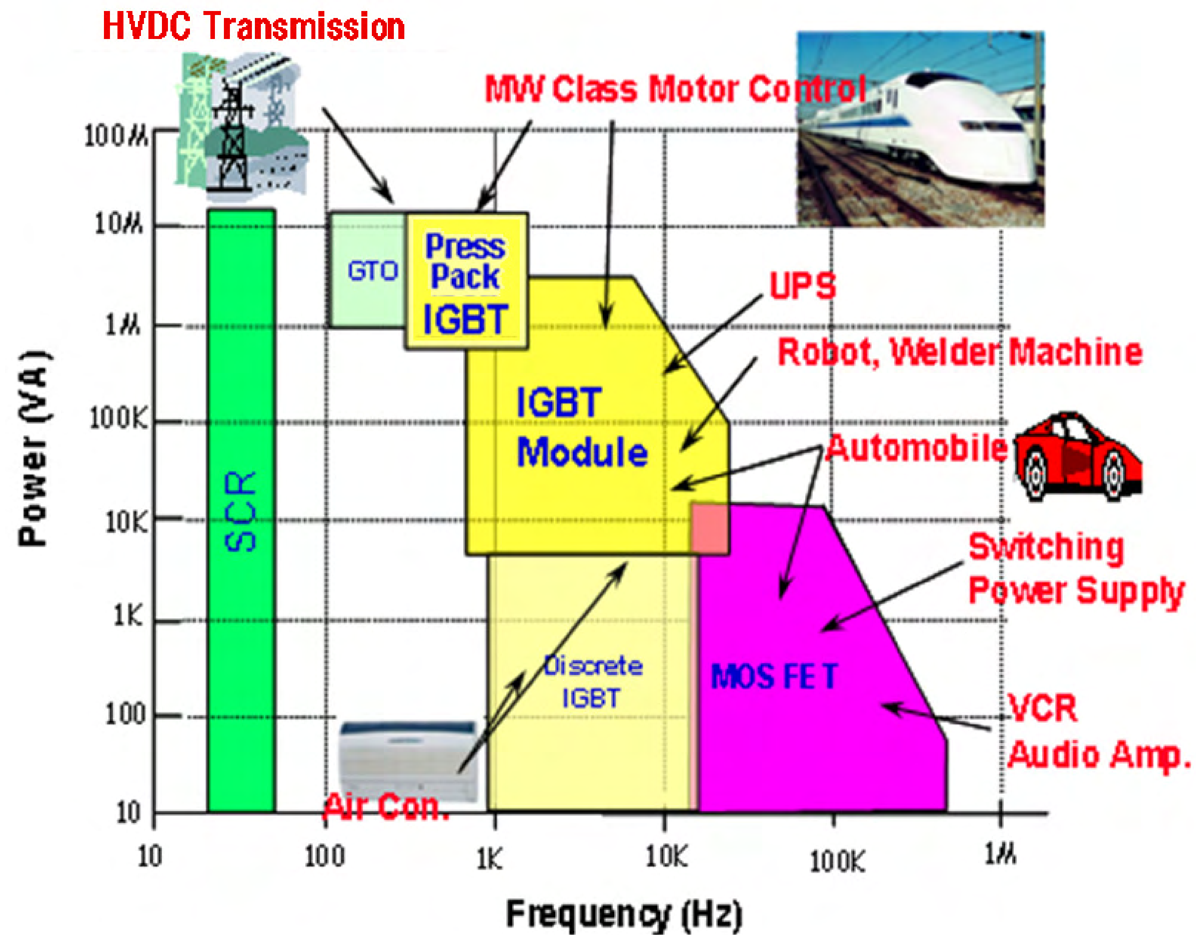
Non-Latch-Up IGBTから

薄ウェハFS-IGBTへ

特許から見たIGBTの定義

Nakagawa Consulting Office, LLC.

応用分野と主力パワー素子



IGBTの特許

1972 Yamagami -- He invented the basic structure of IGBT
(He filed patent only in Japan)

1978 J.D. Plummer discovered " IGBT mode operation in thyristor"
and was grated a patent.

1980 Hans Becke invented basic idea of IGBT.
He claimed "no thyristor action occurs
under any device operating conditions"

1984 Nakagawa invented the design concept of Non-Latch-Up IGBT.
Saturation current ＜ Latch-up current

ISSCC 78

SESSION XVI: LSI DESIGN, TESTING AND INTERFACING

FAM 16.6: A MOS-Controlled Triac Device*

Brad W. Scharf and James D. Plummer

Stanford University

Stanford, CA

A MERGED DEVICE based upon double-diffused MOS (DMOS) technology and combining the MOS and thyristor families has been developed, resulting in an insulated gate triac structure applicable to areas now served by current-controlled PNPN switches. The device – MOS-controlled Triac (TRIMOS) – may be integrated with other MOS components, for use in crosspoint switching, output stages and power control.

Although it is a single regenerative device, TRIMOS can be viewed, as can I^2L, as several merged conventional components, MOSFETs, BJTs, and resistors. Such a partitioning gives rise to a circuit which can be analyzed by a nonlinear circuit analysis program to provide physical insight into the three modes of TRIMOS operation.

Figures 1 and 2(*a*), cross section and photomicrograph of TRIMOS, show that the device is formed by merging two high-voltage DMOS transistors[1] around a common drain. Contact is made to the source and diffused channel of each DMOS, forming symmetrical anode and cathode contacts, and to the shared gate metal, forming the TRIMOS control electrode.

With the cathode grounded and the gate held below the positive DMOS threshold voltage, the PN^- junction at the cathode end blocks any applied positive anode voltage, holding the switch off up to its breakdown voltage; 200V at present.

For gate potentials above threshold, there are three distinct regions of operation. In the low-level realm, anode potentials of less than about 1.5V allow both DMOS channels to become inverted. Both transistors are in their linear regions and all the anode-to-cathode current is carried by electrons at the surface. The device exhibits the low on-resistance and I-V characteristics of two short channel (2.5μ) DMOS transistors in series.

The intermediate level of operation occurs for increasing anode bias which causes the P^+N^- anode junction to become forward biased as indicated in Figure 1, serving as the emitter of a wide base PNP lateral transistor. Its injected holes drift and diffuse to the cathode P region where they are collected and contribute an added component to the device current. The result is an increase in transconductance in this region. Figure 3(*a*) shows the measured characteristics of these first two modes of operation.

As the PNP collector current increases with anode or gate potential, its flow through the pinched resistor R_p raises the potential of the cathode's P region beneath the gate and begins to turn on the vertical NPN transistor inherent in the DMOS structure. This NPN, which can be identified in Figure 4, forms with the PNP a four-layer diode which regeneratively switches when $(\alpha_{NPN} + \alpha_{PNP})$ equals unity. In its *on* state, TRIMOS exhibits a dynamic resistance of less than 10Ω and can pass currents on the order of amperes; Figure 2(*a*).

Control of the switching point by the $I_{CPNP}R_P$ product has been demonstrated by fabrication of devices with anode switching currents varying from tens of microamps to hundreds of milliamps by varying the geometrical layout. By shunting R_P with a switch (Figure 4), the TRIMOS may be switched out of its on state or inhibited from triggering. This type of shunt switch has been realized by an MOS transistor fabricated adjacent to the TRIMOS. Without such a bypass structure, a TRIMOS typically has turn-on and turn-off times on the order of 200ns and its single pulse dv/dt capability exceeds 1000V/μs.

As the discussion of operation has indicated and as Figure 4 illustrates, several bipolar and MOS transistors and resistors can be identified within the TRIMOS structure. Analysis of the circuit formed by these components has resulted in a model for operation below regeneration. A circuit analysis program containing sophisticated models of both bipolar and MOS devices must be used to obtain accurate simulation of device characteristics. This has been done on the Mini-MSINC[2] program using a DMOS model developed earlier[3] and an integral charge-control bipolar model[4,5]. The comparison of measured and modelled characteristics in Figure 3 delineates the two regions of operation and shows quantitative agreement over a rather large operating region. The apparent increase in g_m for $V_{DS} > 1.5V$ as the lateral PNP turns on is visible in both the experimental and simulated curves.

There are several advantages to the discretized model. First, it corresponds to the physical structure and aids in an intuitive understanding of the different modes of TRIMOS operation since the individual building blocks are familiar devices. Secondly, the parameters required for the model are those routinely measured on the BJT and MOSFET. Many of these can be measured directly from the TRIMOS component of interest and the others may be inferred from ordinary test structures or process characteristics. Lastly, process variations affecting the component parameters are well understood and the partitioned model translates such variations into TRIMOS performance. Thus, the impact of structure changes can be evaluated, making the model valuable for design as well as analysis.

For modeling the high current operation, after regenerative switching, common thyristor models[6] can be expected to apply within the rather stringent limitations of their approximations and the added constraints of a two-dimensional planar structure rather than one dimensional discrete devices.

*Project performed under NIH Grant No. 1 P01 GM17940-5 and NSF Grant No. ENG74-18419.

[1] Plummer, J.D. and Meindl, J.D., "A Monolithic 200-V CMOS Analog Switch", *IEEE J. Solid State Circuits*, Vol. SC-11, p. 809-817; Dec., 1976.

[2] Young, T.K. and Dutton, R.W., "Mini-MSINC – A Minicomputer Simulator for MOS Circuits with Modular Built-In Model", *IEEE J. Solid State Circuits*, Vol. SC-11, p. 730-732; Oct., 1976.

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[4] Gummel, H.K. and Poon, H.C., "An Integral Charge Control Model of Bipolar Transistors", *Bell System Technical Journal*, Vol. 49, p. 827-852; May/June, 1970.

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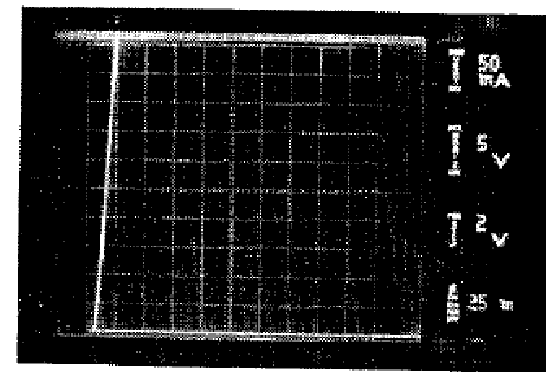
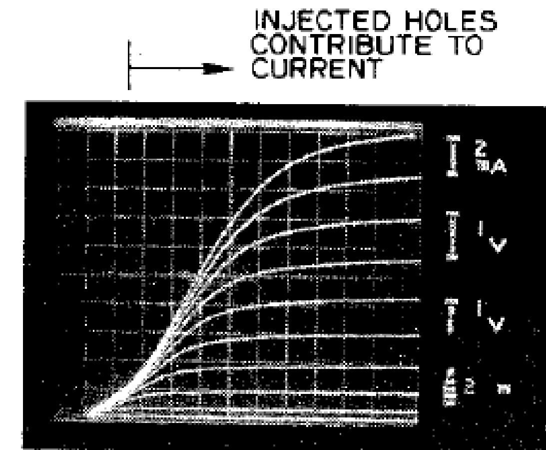
[6] Blicher, A., "Thyristor Physics" (Ch. 7), *Springer-Verlag*; 1976.





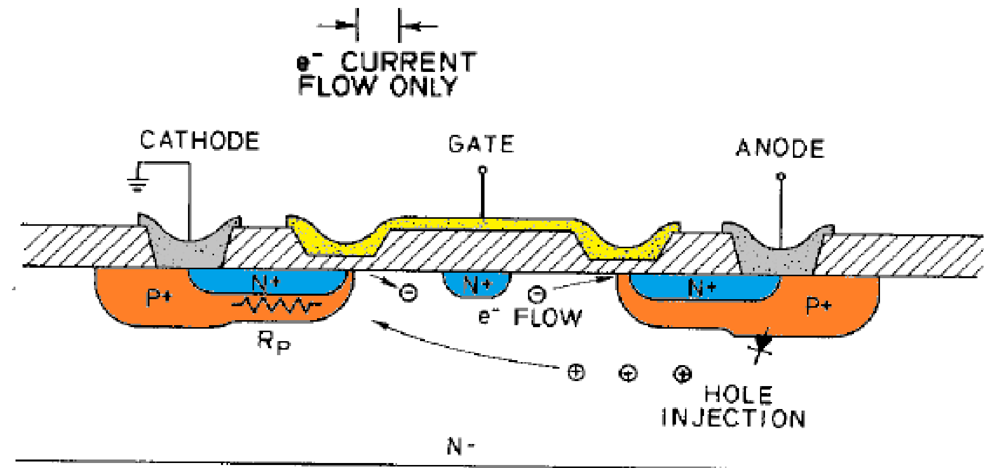


FIGURE 1–TRIMOS structure; two DMOS transistors merged around a common drain.

PlummerのラッチアップするIGBT特許

United States Patent [19] Plummer

[11] 4,199,774
[45] Apr. 22, 1980

[54] MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE

[75] Inventor: James D. Plummer, Mountain View, Calif.

[73] Assignee: The Board of Trustees of the Leland Stanford Junior University, Stanford, Calif.

[21] Appl. No.: 943,200

[22] Filed: Sep. 18, 1978

[51] Int. Cl.[2] H01L 7/02

[52] U.S. Cl. 357/41; 357/23; 357/55; 357/48; 307/304

[58] Field of Search 357/41, 48, 55, 23; 307/304

[56] References Cited

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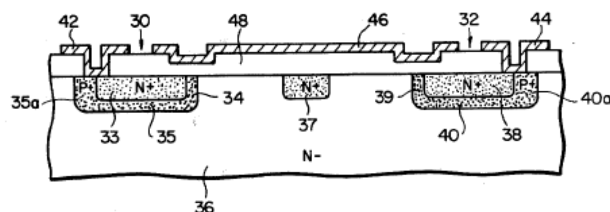
4,119,996	10/1978	Jhabrola	357/23
4,145,703	3/1979	Blanchard	357/55

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

[57] ABSTRACT

An electrical circuit device made in integrated monolithic form has low level operating characteristics of a MOS device and high level operating characteristics of a Triac. The structure includes two double diffused MOS transistors which have merged drain regions. At higher voltage and current levels a lateral Triac structure is triggered by the MOS devices. Alternatively, separate terminal contacts can be made to the P and N regions comprising the MOS transistor source and channel regions with the Triac triggered conventionally by an externally applied control voltage.

25 Claims, 20 Drawing Figures



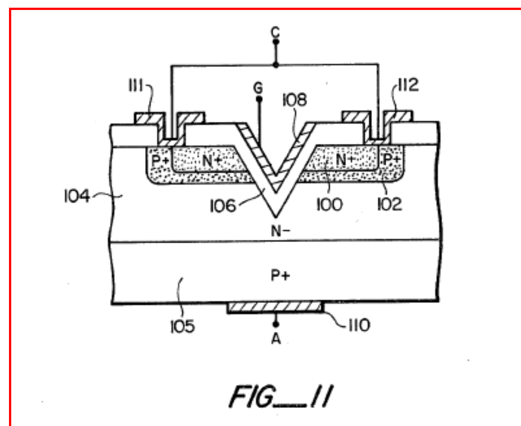


FIG_11

United States Patent [19] Plummer

[11] E Patent Number: Re. 33,209
[45] Reissued Date of Patent: May 1, 1990

[54] MONOLITHIC SEMICONDUCTOR SWITCHING DEVICE

[75] Inventor: James D. Plummer, Mt. View, Calif.

[73] Assignee: Board of Trustees of the Leland Stanford Jr. Univ., Stanford, Ill.

[21] Appl. No.: 539,111

[22] Filed: Dec. 5, 1983

Related U.S. Patent Documents

Reissue of:
[64] Patent No.: 4,199,774
Issued: Apr. 22, 1980
Appl. No.: 943,200
Filed: Sep. 18, 1978

[51] Int. Cl.[5] H01L 29/78

[52] U.S. Cl. 357/23.4; 357/23.9; 357/39; 357/48; 357/55; 357/41

[58] Field of Search 357/23.4, 23.9, 55, 357/48, 41, 39

[56] References Cited

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4,145,703	3/1979	Blanchard	357/23.4 X

Primary Examiner—Martin H. Edlow
Attorney, Agent, or Firm—Flehr, Hohbach, Test, Albritton & Herbert

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20 Claims, 4 Drawing Sheets

1. A monolithic semiconductor SCR device comprising:

a semiconductor [body] *substrate of one conductivity type and an epitaxial layer of opposite conductivity type, said epitaxial layer* having at least one major surface, and

[a body region adjacent to said surface of one conductivity type,] first and second spaced regions of [opposite] *said one* conductivity type formed in said [body region] *epitaxial layer* and abutting said major surface, third and fourth regions of said [one conductivity] *opposite conductivity* type formed in said first and second regions, respectively, abutting said major surface and defining first and second channel regions in said first and second regions, respectively,

a layer of insulation on said major surface,

a gate electrode formed on said layer of insulation and above said first and second channel regions, an ohmic contact to said first and third regions, and an ohmic contact to said second and fourth regions, *and*

an ohmic contact to said semiconductor substrate.

BeckeのIGBT特許

United States Patent [19] — Becke et al.

[11] 4,364,073
[45] Dec. 14, 1982

[54] POWER MOSFET WITH AN ANODE REGION

[75] Inventors: Hans W. Becke, Morristown; Carl F. Wheatley, Jr., Somerset, both of N.J.

[73] Assignee: RCA Corporation, New York, N.Y.

[21] Appl. No.: 133,902

[22] Filed: Mar. 25, 1980

[51] Int. Cl.³ H01L 29/00
[52] U.S. Cl. 357/23; 357/37
[58] Field of Search .... 357/37, 38, 23, 23 R

[56] References Cited

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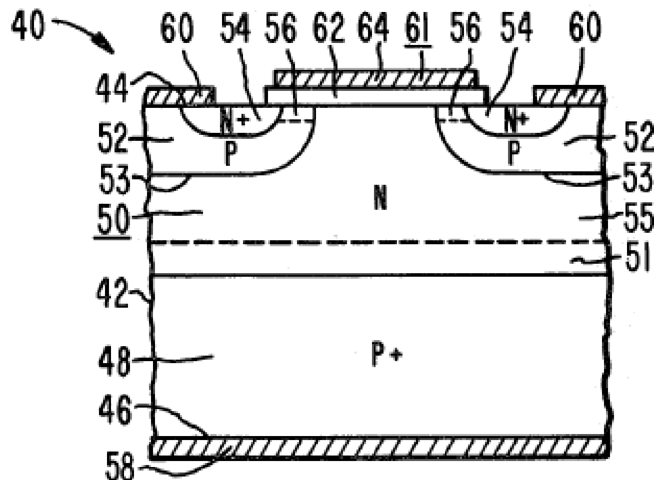
1367325 9/1974 United Kingdom .
2034114 5/1980 United Kingdom .

Primary Examiner—R. A. Rosenberger
Attorney, Agent, or Firm—Birgit E. Morris; Donald S. Cohen; Kenneth R. Glick

[57] ABSTRACT

A vertical MOSFET device having source, body and drain regions, includes an anode region in series with the drain region. The source, body and drain regions have a first forward current gain and the anode, drain and body regions have a second forward current gain, such that the sum of the current gains is less than unity. The anode region provides minority carrier injection into the drain region, enhancing device performance in power applications.

17 Claims, 5 Drawing Figures



1. A vertical MOSFET device, comprising:

a semiconductor substrate, including in series, adjacent source, body, drain and anode regions of alternate conductivity type;

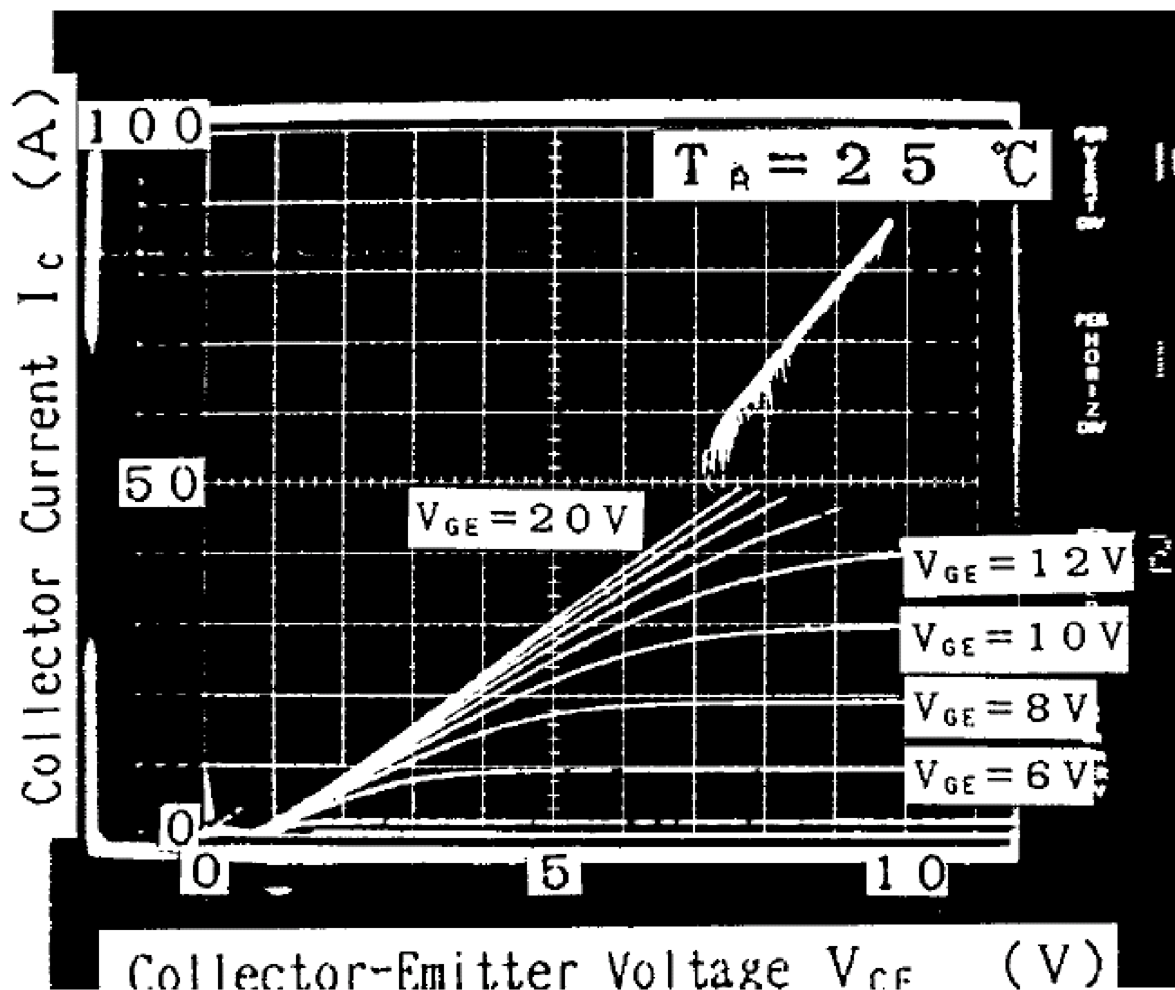
the body region being adjacent to a surface of the substrate;

the source and drain regions being spaced so as to define a channel portion in the body region at said surface;

the source, body and drain regions having a first forward current gain α_1 and the anode, drain and body regions having a second forward current gain α_2, such that the sum $\alpha_1+\alpha_2$ is less than unity, and no thyristor action occurs under any device operating conditions.

１９８３年

ＩＧＢＴは壊れやすく、ラッチアップを防ぐことは不可能に近いと考えられた!!!



GEの素子

Non-Latch-Up IGBT

1984年

Non-Latch-Up 1200V 75A Bipolar-Mode MOSFET with Large ASO

Akio Nakagawa, Hiromichi Ohashi, Mamoru Kurata
Hoshihiro Yamaguchi, Kiminori Watanabe

Toshiba R&D Center
1 Komukai Toshibacho, Saiwaiku
Kawasaki, Japan

In 1984 ICSSDM, Kobe, we already reported the development of 1200V, 75A bipolar-mode MOSFETs(BIFET[1], or called IGT, COMFET [2,3]), which could turn-off 75Amps drain current with 1000V applied drain voltage at the elevated temperature, 125 C(see Fig. 1).

This paper presents improved BIFETs with non-latch-up structure as well as a large ASO. Figure 2 shows a cross section of a new BIFET. A part of the source layer is periodically eliminated, providing a low resistance bypass for holes to the source electrode without biasing the source-base junction. The maximum drain current was substantially limited by the channel pinch-off effect before ti reached the increased latch-up current level, which was attained by the vertical BIFET structure and the optimized source pattern. Thus, the latch-up mode was not observed under any driving conditions unless gate voltage exceeds 20V.

It was found that the latch-up current density J_L depends gate width L_G through the following equation [1]:

$J_L = V_{bi}/(L_G R_b)$ ----- L_G: gate width; V_{bi}:built-in voltage for sourcebase junct.;
R_b:channel to source electrode p-base resistance for unit channel width.

New BIFET structure provides a lower R_b, which enables to use a larger L_G than the original BIFET with attaining a high latch-up current density. Thus, new BIFETs exhibit low forward voltage regardless of reduced channel width.

BIFETs should have a sufficiently large ASO so that BIFETs can be used as a key switching device in place of bipolar transistors in a power application system. If the external load is caused to be short-circuited due to system failure, drain current is limited only by the device resistance itself with the drain voltage being the same as the external power supply voltage. The device should dissipate a large heat until a protection circuit works, reducing gate voltage to zero. Figure 3 shows the measured 25 μsec forward conduction ASO limit. The improved BIFETs can sustain more than 65Amps drain current with 600V forward voltage drop and 20V gate voltage during 25 μsec, which is sufficient for sensing and device protection. Measured switching ASO is also included in Fig. 3. Voltage and current density product exceeds $3X10^5 VA/cm^2$, which suggests avalanche multiplication for a failure cause.

Neither snubber nor clamp circuit is necessary for the inductive load switching. Figure 4 shows 48Amps switching waveforms, wherein voltage surge is clamped by the device itself. The electrical characteristics for the improved BIFETs are given in Table. BIFETs are now ready for applications.

References [1] A. Nakagawa et al, in Extended Abstracts of the 16th (1984 International) Conference on Solid State Devices and Materials, Kobe, 1984, pp.309-312

[2] M.F. Chang et al, 1983 IEEE IEDM Tech. Digest, pp. 83

[3] A.M. Goodman et al, 1983 IEEE IEDM Tech. Digest, pp. 79

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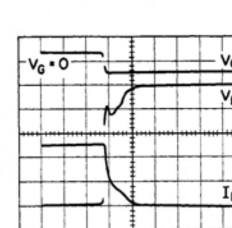

Fig.1 Typical turn-off waveforms for a BIFET. I_D:30A/Div, V_D:200V/Div, Time:2μsec/Div, Temp:125°C.

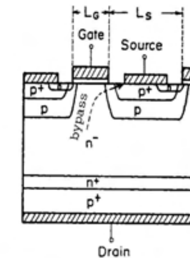

Fig.2 A cross section of a new BIFET

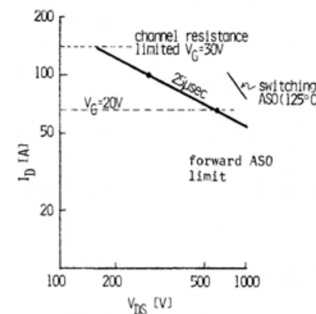

Fig.3 Measured 25μsec forward conduction ASO limit, which actually means device destruction.

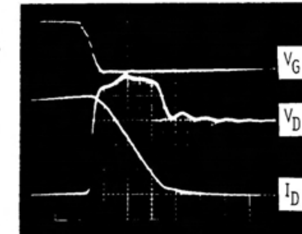

Fig.4 Typical inductive load switching waveform. I_D:12A/Div, V_D:200V/Div, Time:0.5μsec/Div.

Breakdown voltage	1200V	Turn-off delay time	0.3μsec
Continuous drain current	20A	fall-time	1.8μsec
Forward voltage drop	3V(20A)	Device active area	$20mm^2$
Turn-on time	120nsec	Maximum turn-off current (V_D=1000V, Temp=125°C)	more than 75A

Table electrical characteristics

16.8

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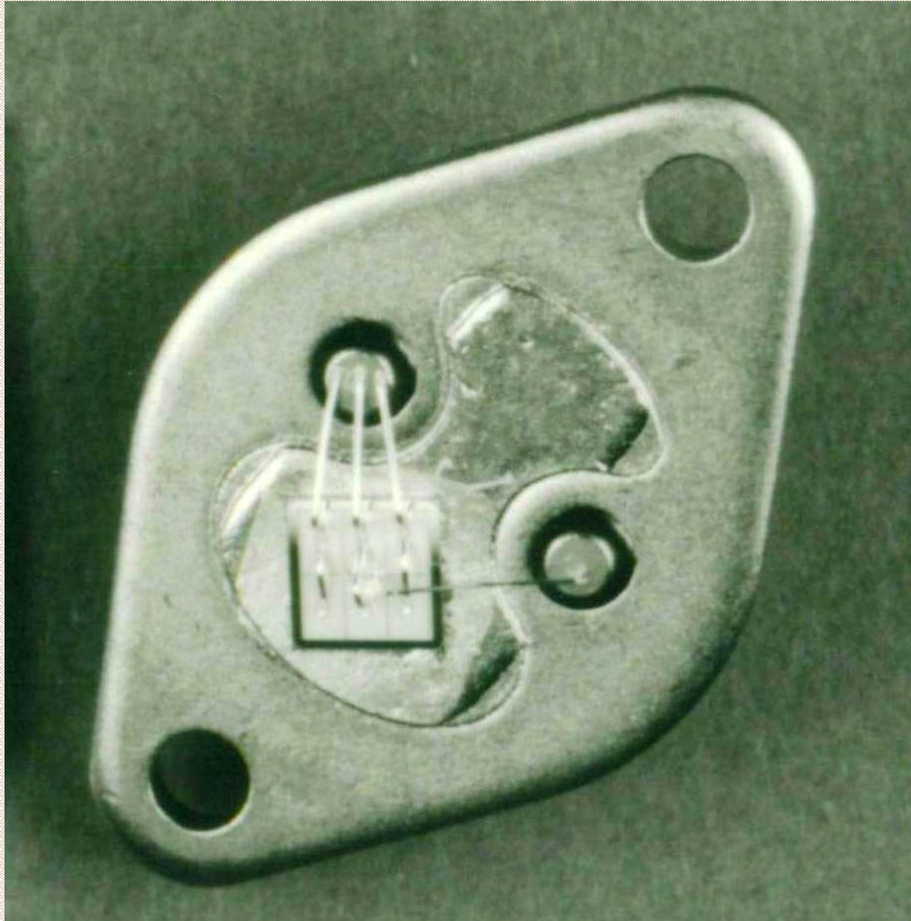
ノンラッチアップIGBT最初の論文
IEDM Late News 1984年12月

First Non-Latch-Up IGBT in 1984.

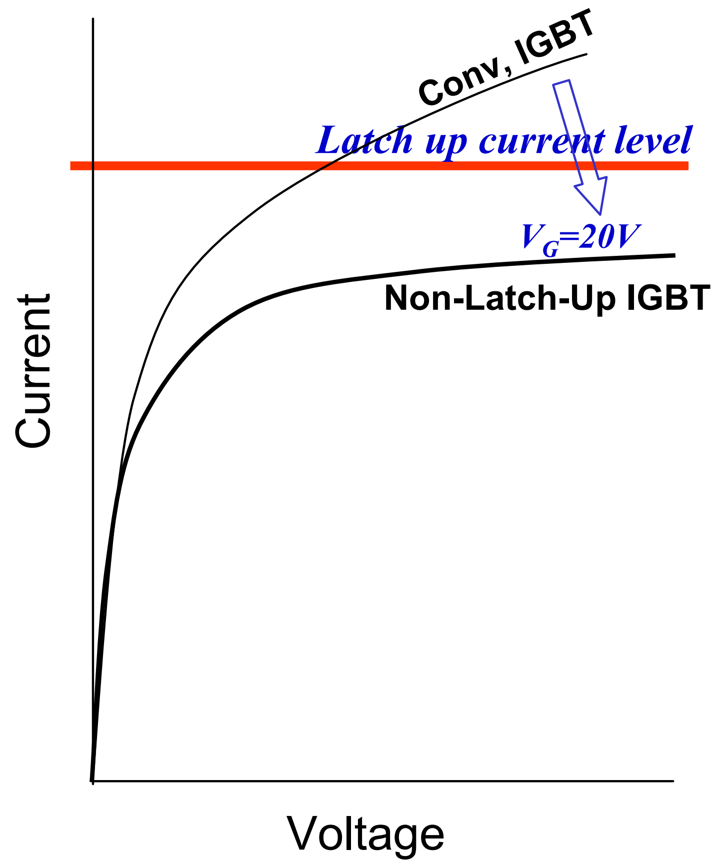


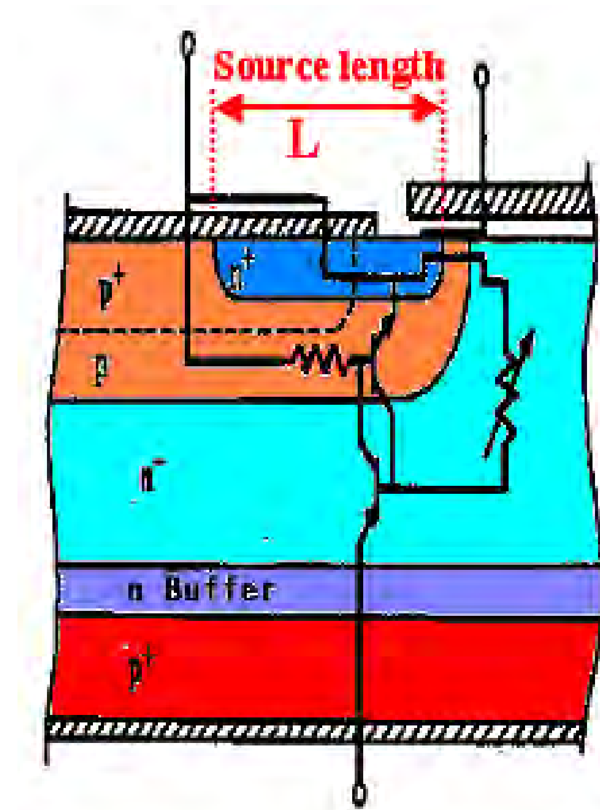
2010 IEEE William E. Newell Power Electronics Award

For development of non-latch-up IGBTs

Design principle of Non-latch-Up IGBT

Saturation current(@ V_G =20V) < Latch-up current





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IGBTの特許

1978 J.D. Plummer discovered “ IGBT mode operation in thyristor”
and was grated a patent.

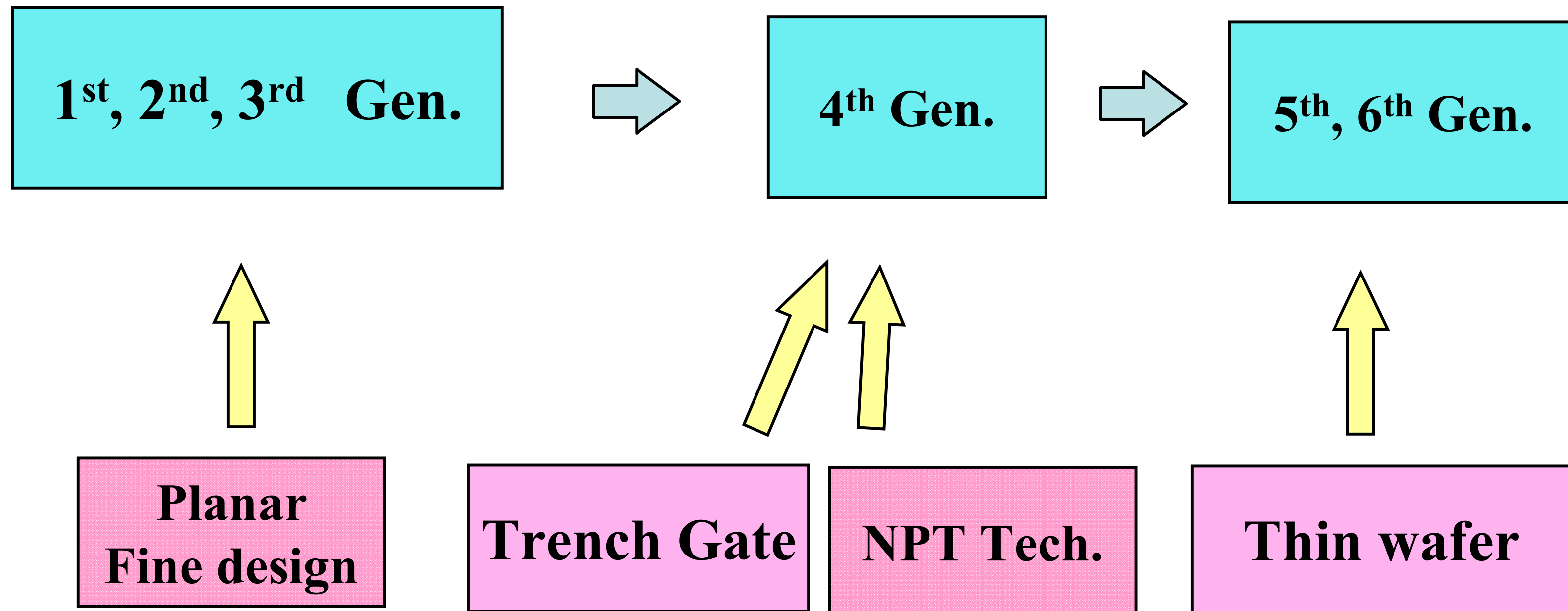
GE(バリガ)のIGBTはラッチアップするPlummer特許の範囲

1980 Hans Becke invented basic idea of IGBT.
He claimed “no thyristor action occurs
under any device operating conditions”

Becke特許はnon-latch-up IGBTsの出現で
IGBTの基本特許に昇格!!!
現在のIGBTはPlummer特許には抵触しない!!

1984 Nakagawa invented the design concept of Non-Latch-Up IGBT.
Saturation current ＜ Latch-up current

Technical trend for 600-1200V IGBT



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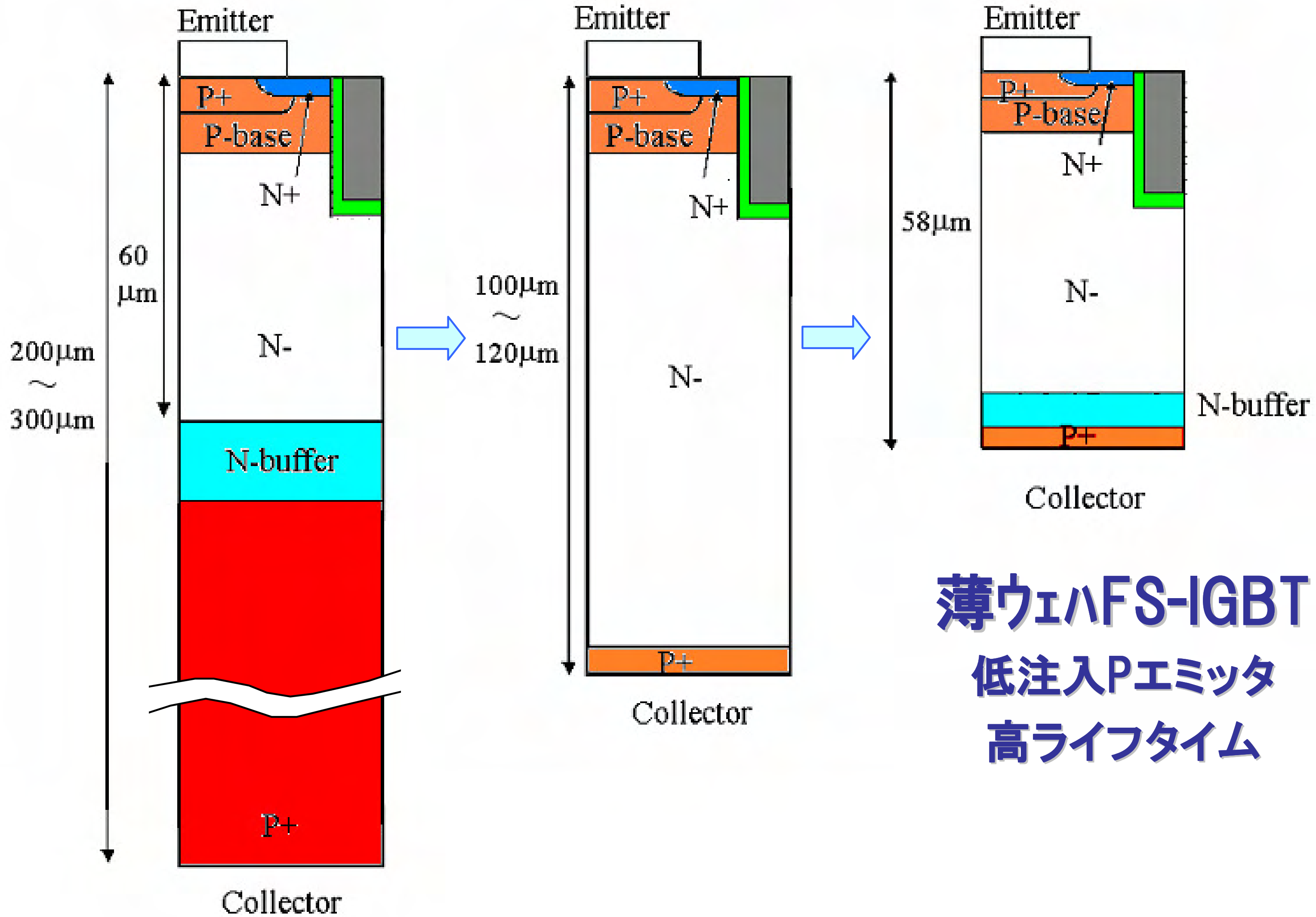


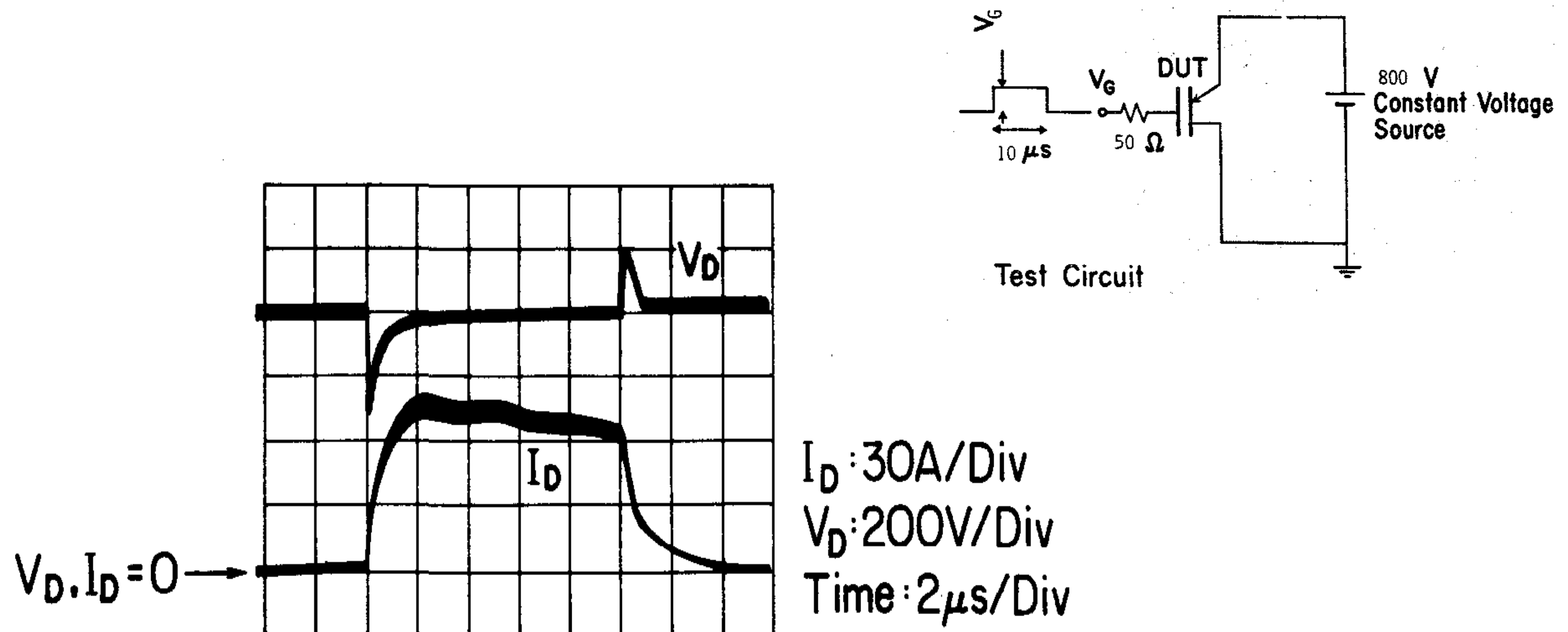
PT-IGBT
高注入Pエミッタ
低ライフタイム

NPT-IGBT
低注入Pエミッタ
高ライフタイム

nバッファとField Stop層の違い

Short Circuit Capability

[1] 0.3 MW/cm² IEDM, Nakagawa, 1984: World first Short-circuit capability
[2] 0.9 MW/cm² PESC, Nakagawa, 1988: IGBT SOA > Bip. Tr. SOA
[3] 2 MW/cm² ISPSD, Hagino, 1996: Extremely large SOA



World First Demonstration of Short Circuit Capability in 1984.

Space charge in N-base

$$Q = qN_D + q(p - n) = qN_D + J\{\gamma/v_h - (1-\gamma)/v_e\}$$

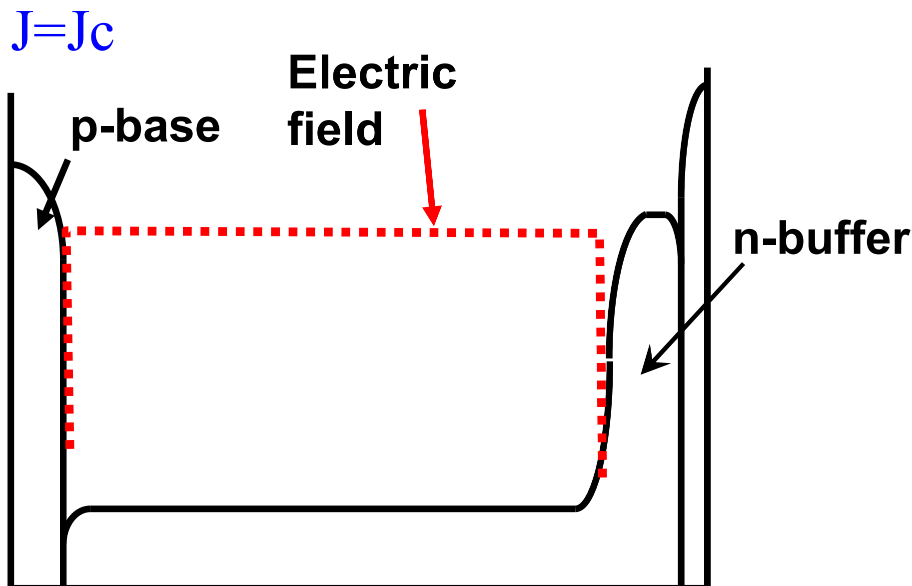
$$p = \frac{J_p}{qv_h} \quad n = \frac{J_n}{qv_e} \quad \gamma = \frac{J_p}{J}$$

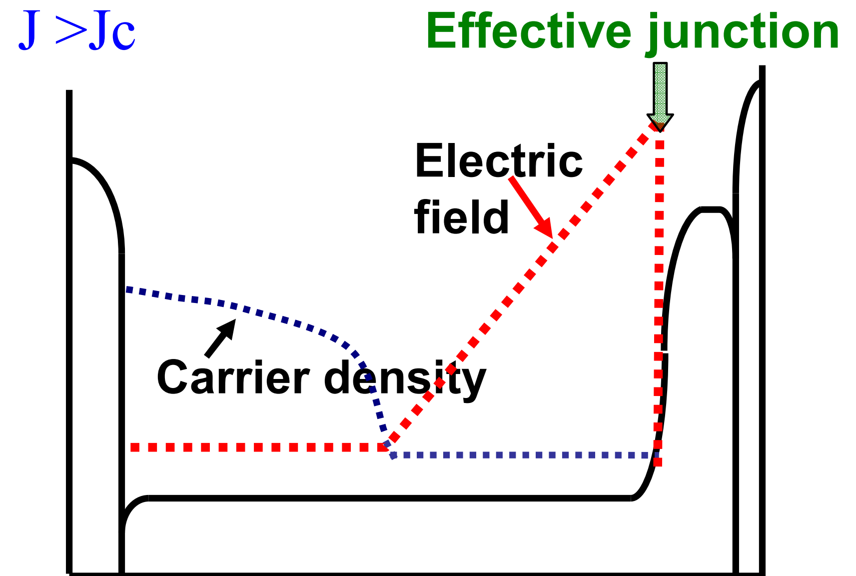
Define $J_C = qN_D/\{(1-\gamma)/v_e - \gamma/v_h\}$ when $\gamma < \frac{v_h}{v_e + v_h}$

$J < J_C$: Space charge, Q is positive.

$J = J_C$: Space charge, Q is zero!

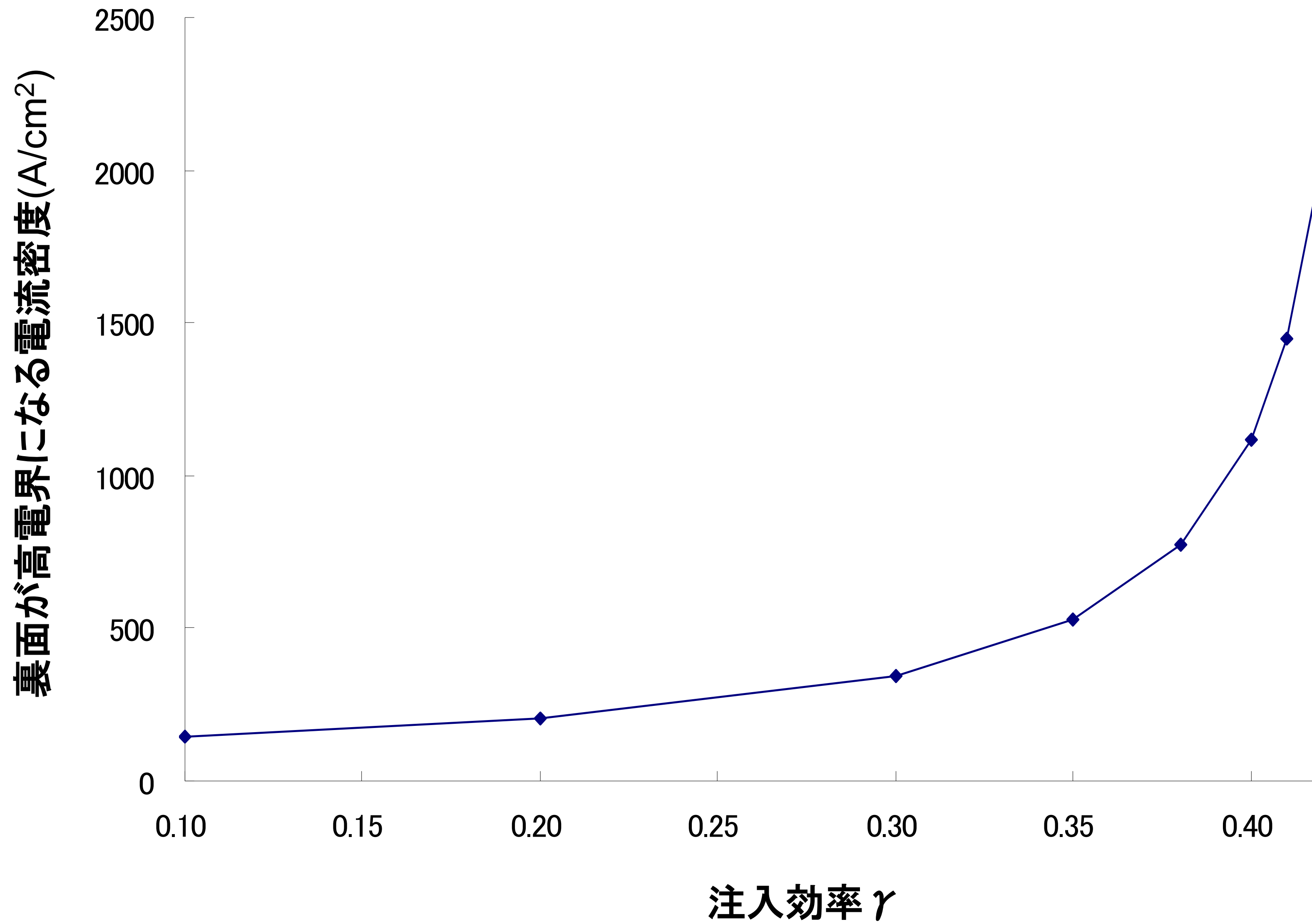
$J > J_C$: Space charge, Q is negative!



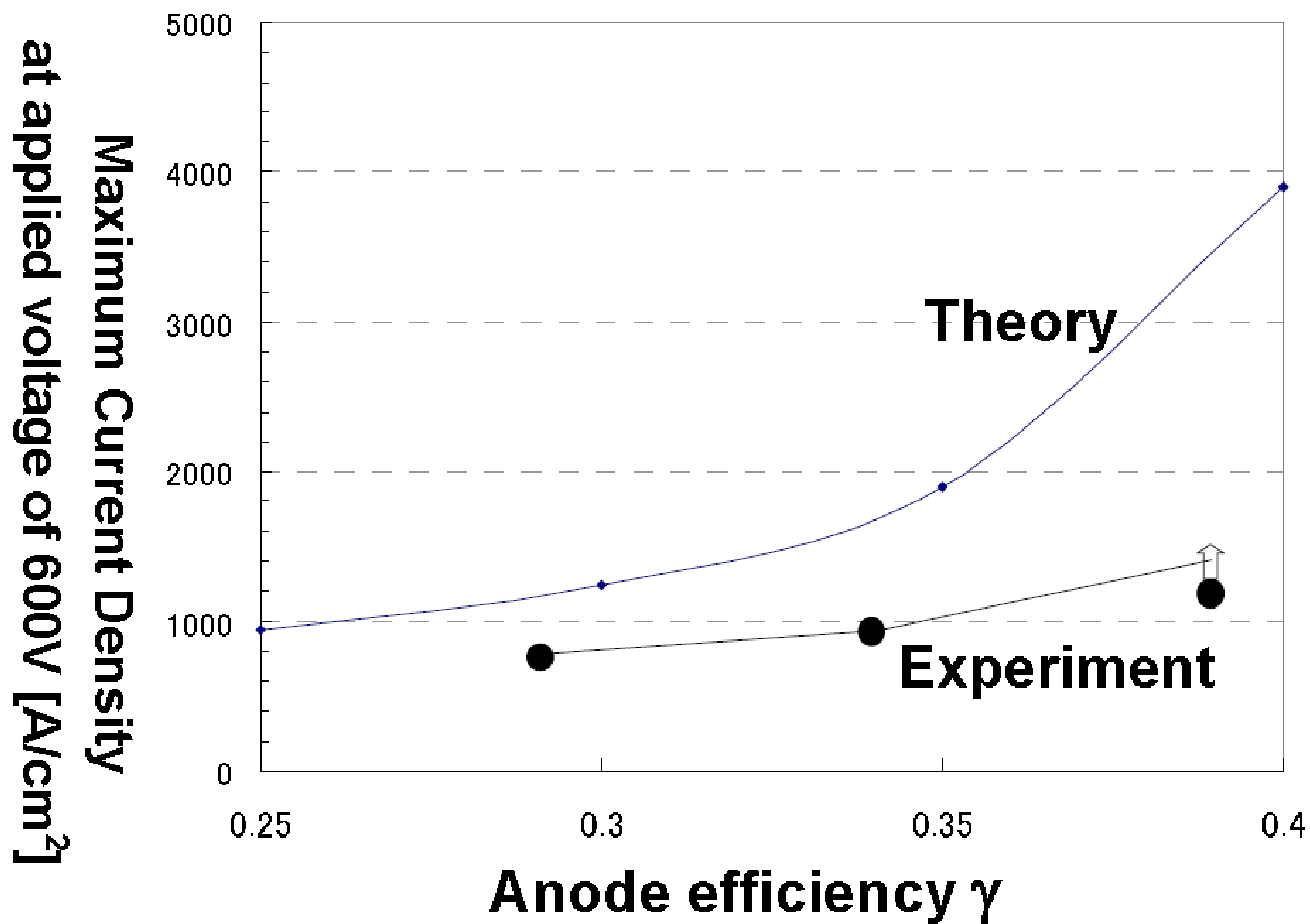


Nakagawa Consulting Office, LLC.

1200V IGBT



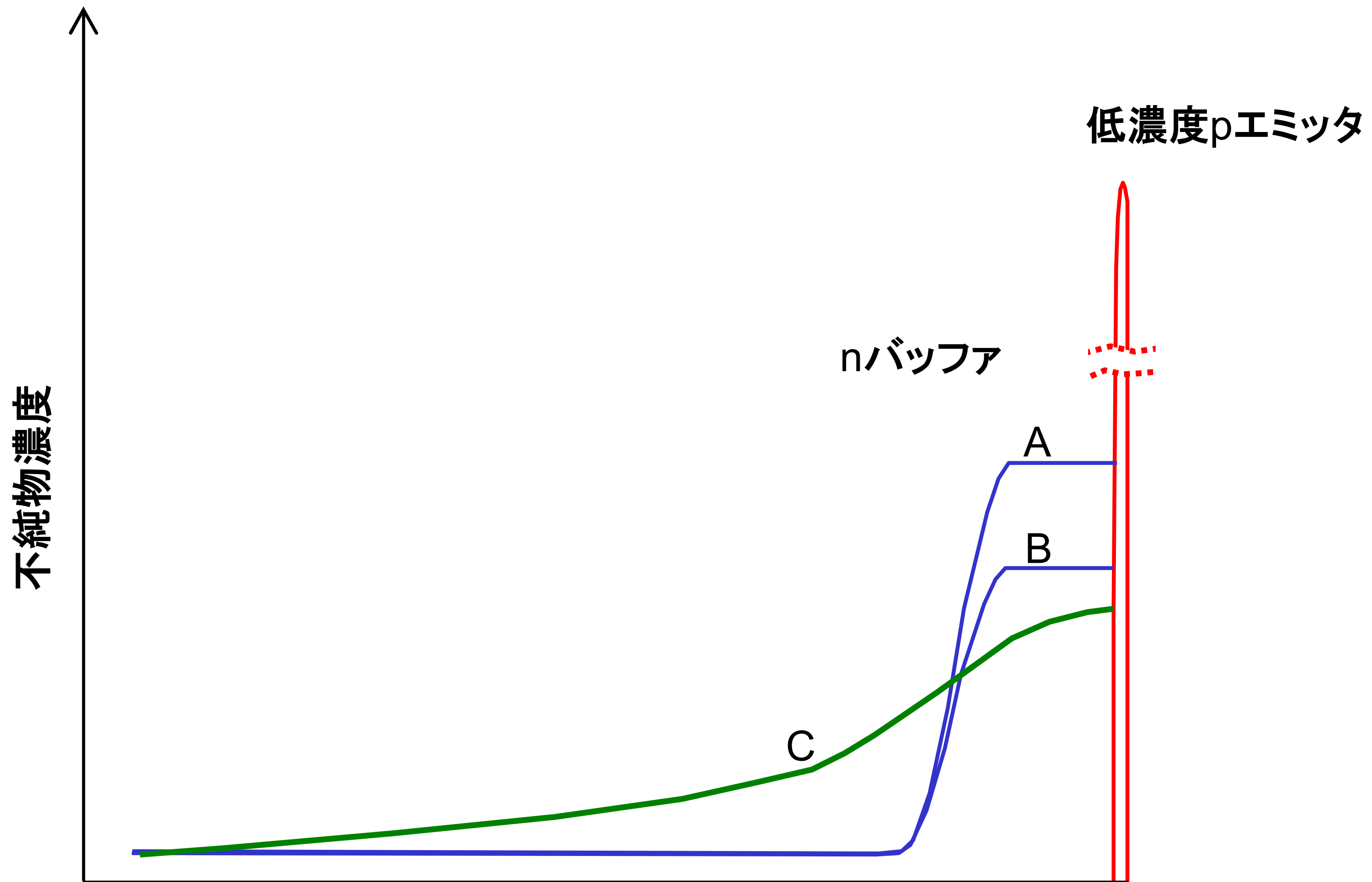
負荷短絡耐量とアノード側の注入効率

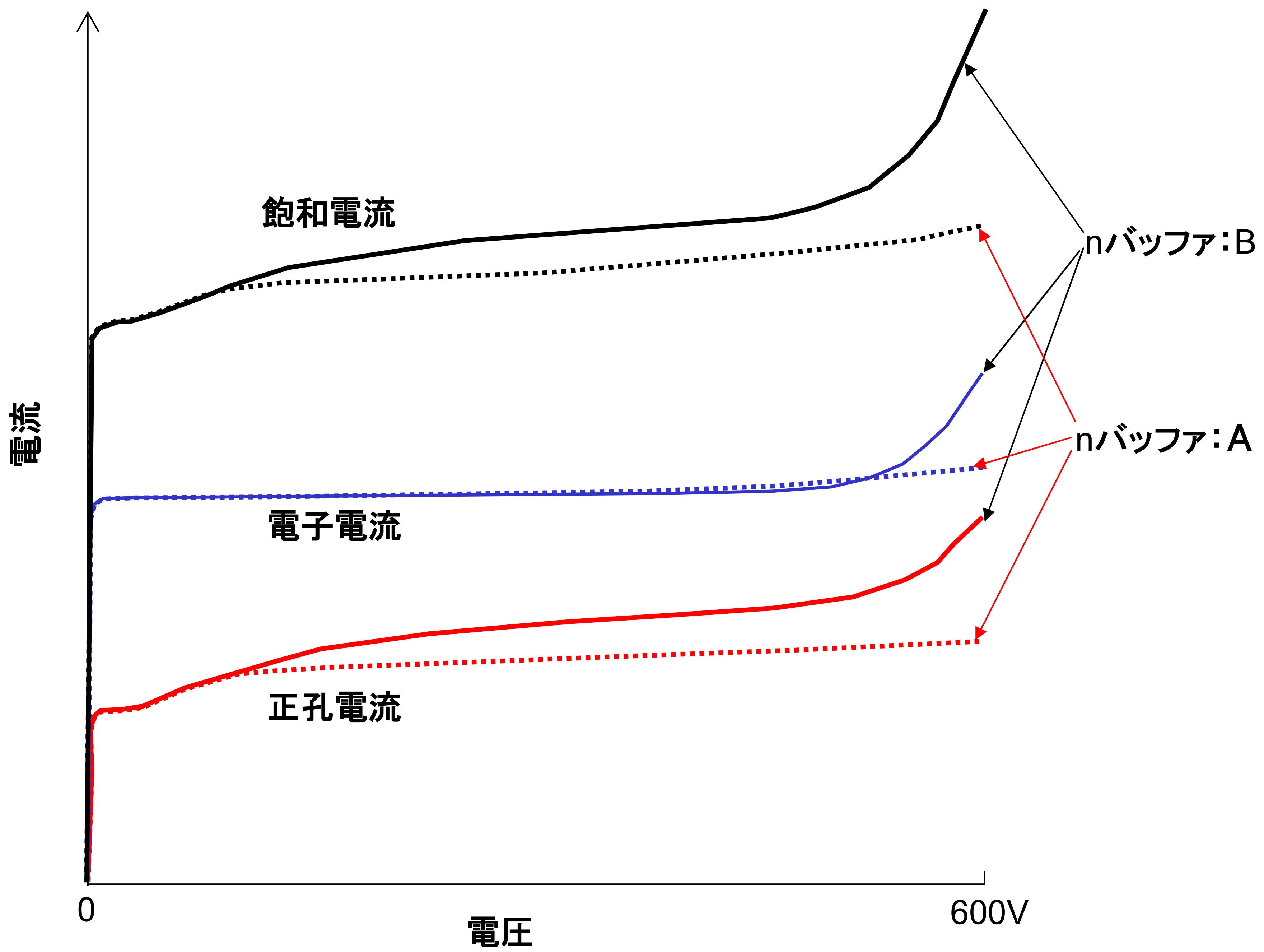


A. Nakagawa et.al., ISPSD 2004, pp.103-106

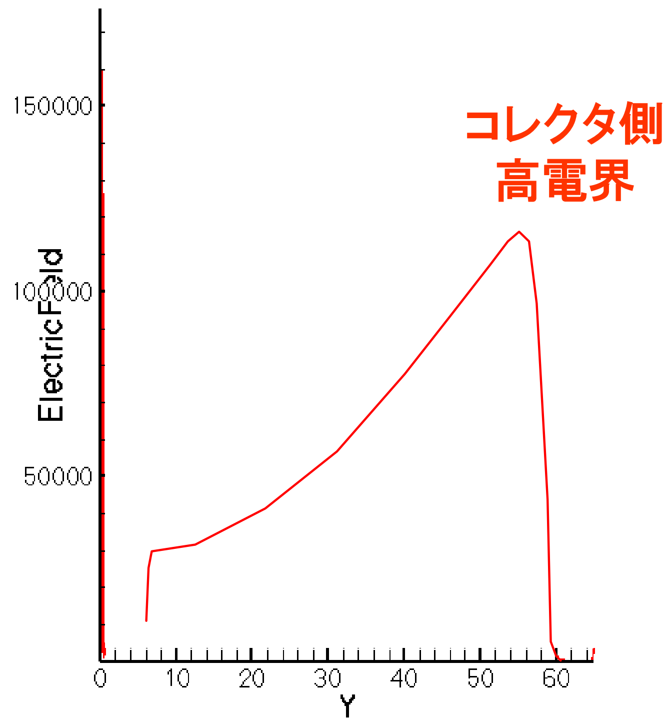
Nakagawa Consulting Office, LLC.

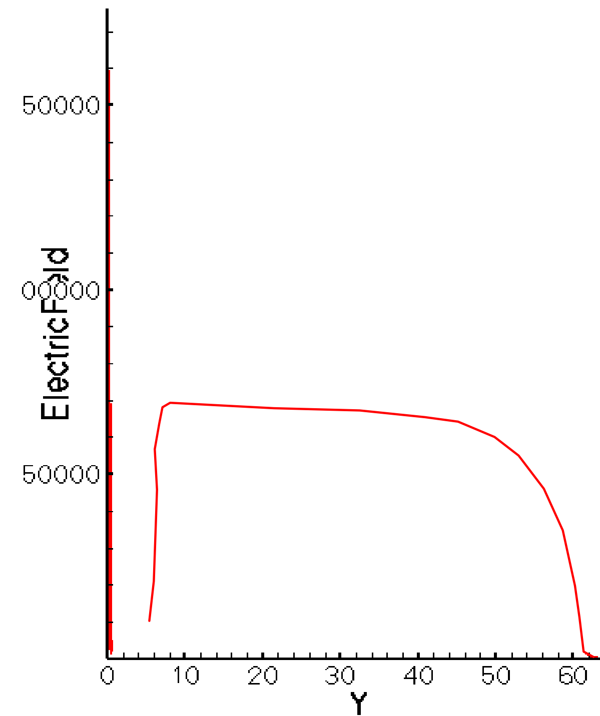
nバッファの最適化
3種類のnバッファの違い




飽和電流
電子電流
正孔電流
nバッファ：B
nバッファ：A
電流
電圧
0
600V

600Vの電界分布

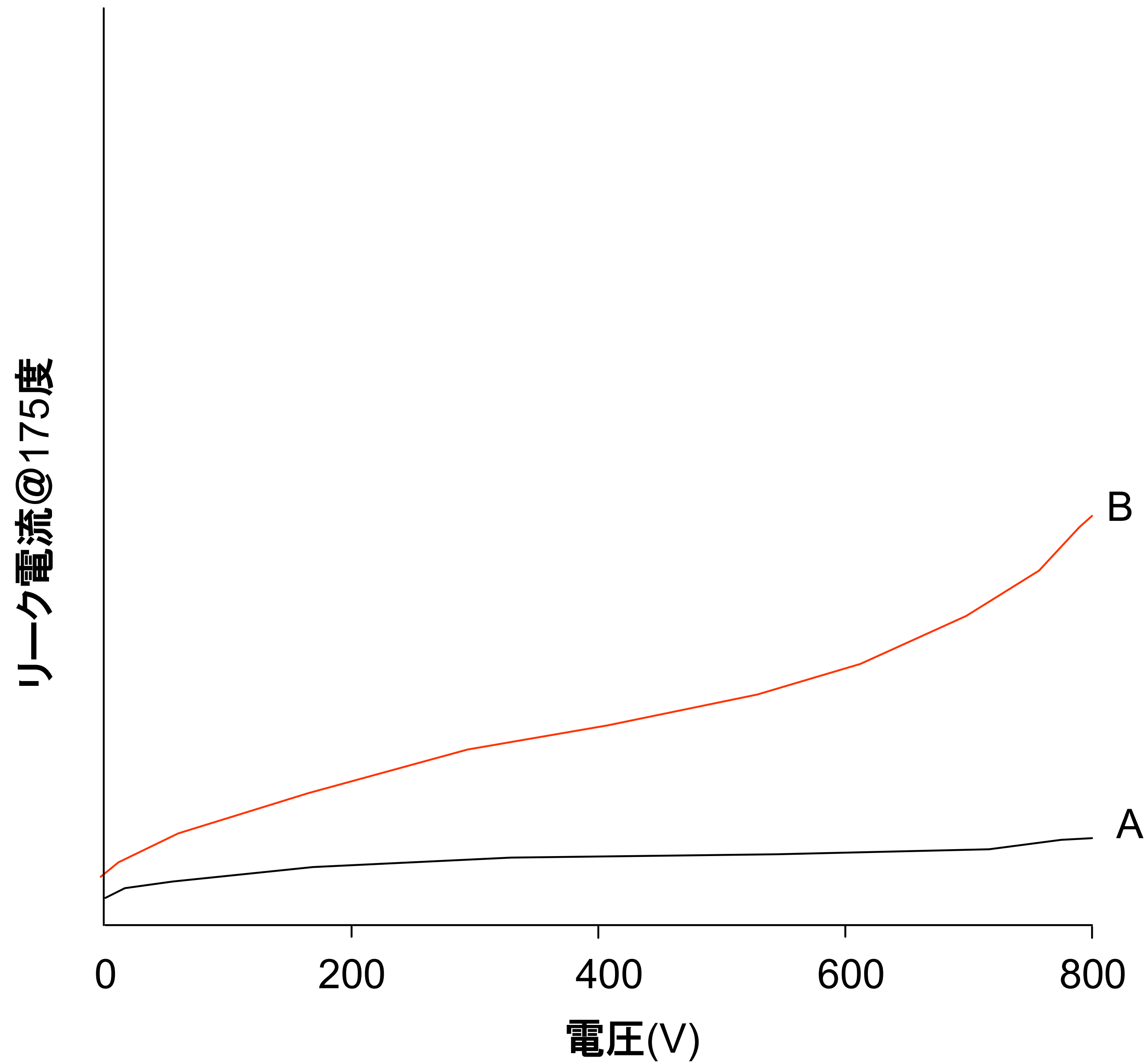




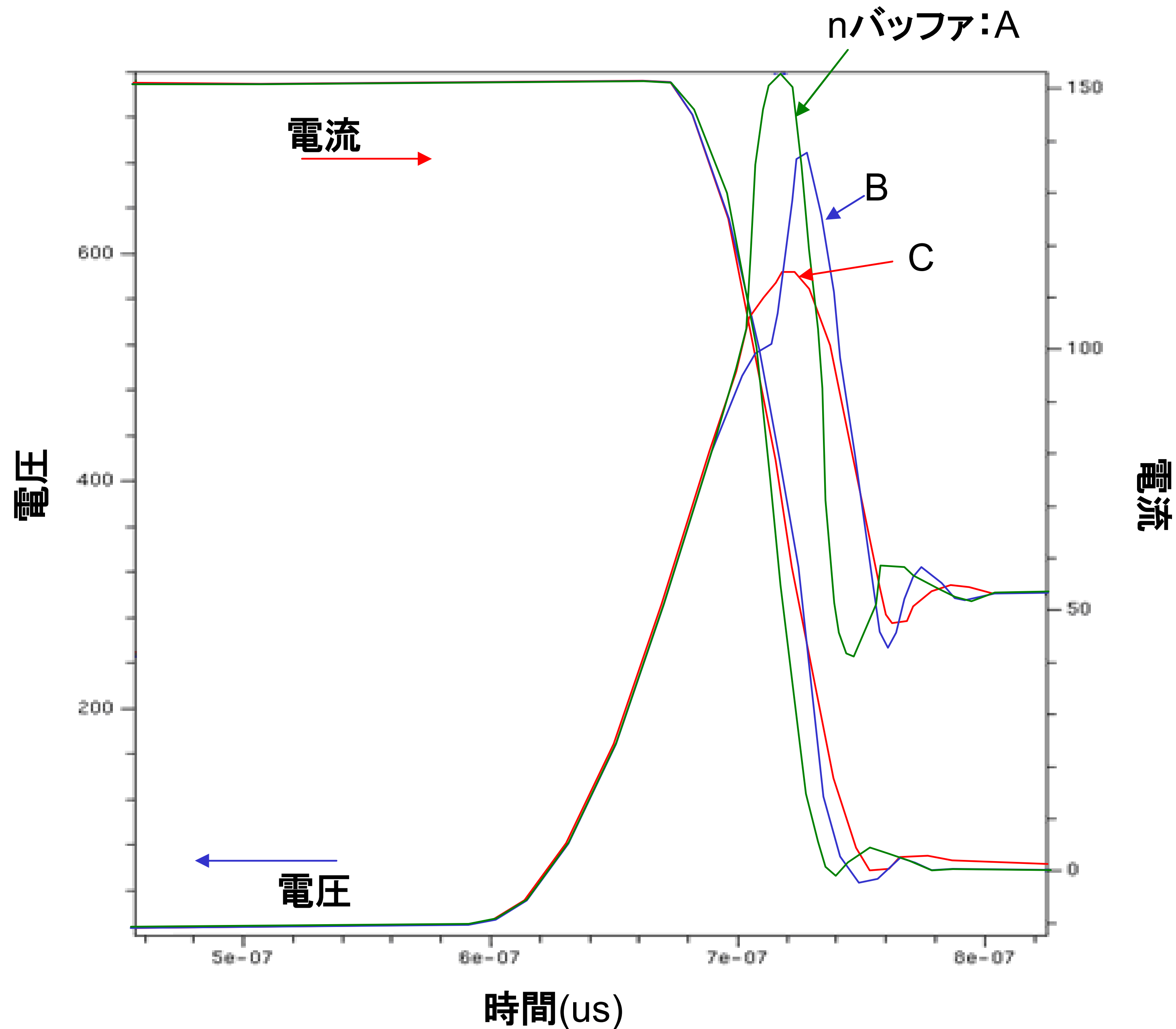
nバッファ：A

負荷短絡破壊

nバッファ：B


リーク電流@175度
B
A
0
200
400
600
800
電圧(V)

nバッファによるターンオフ波形の相違



nバッファ:A は負荷短絡で電流が振動しやすい!

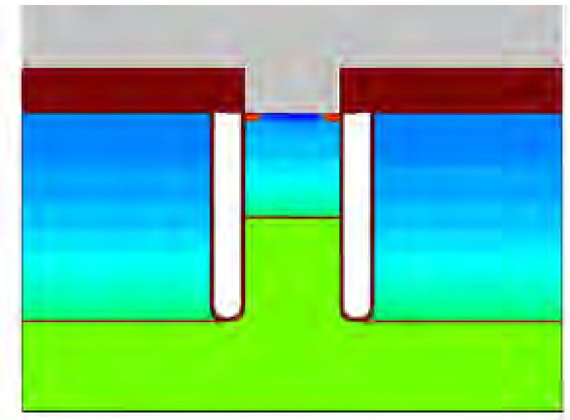
600
400
200
4000
3000
2000
1000
0
0
5e-06
1e-05

TotalC
TotalC
Outer
Outer

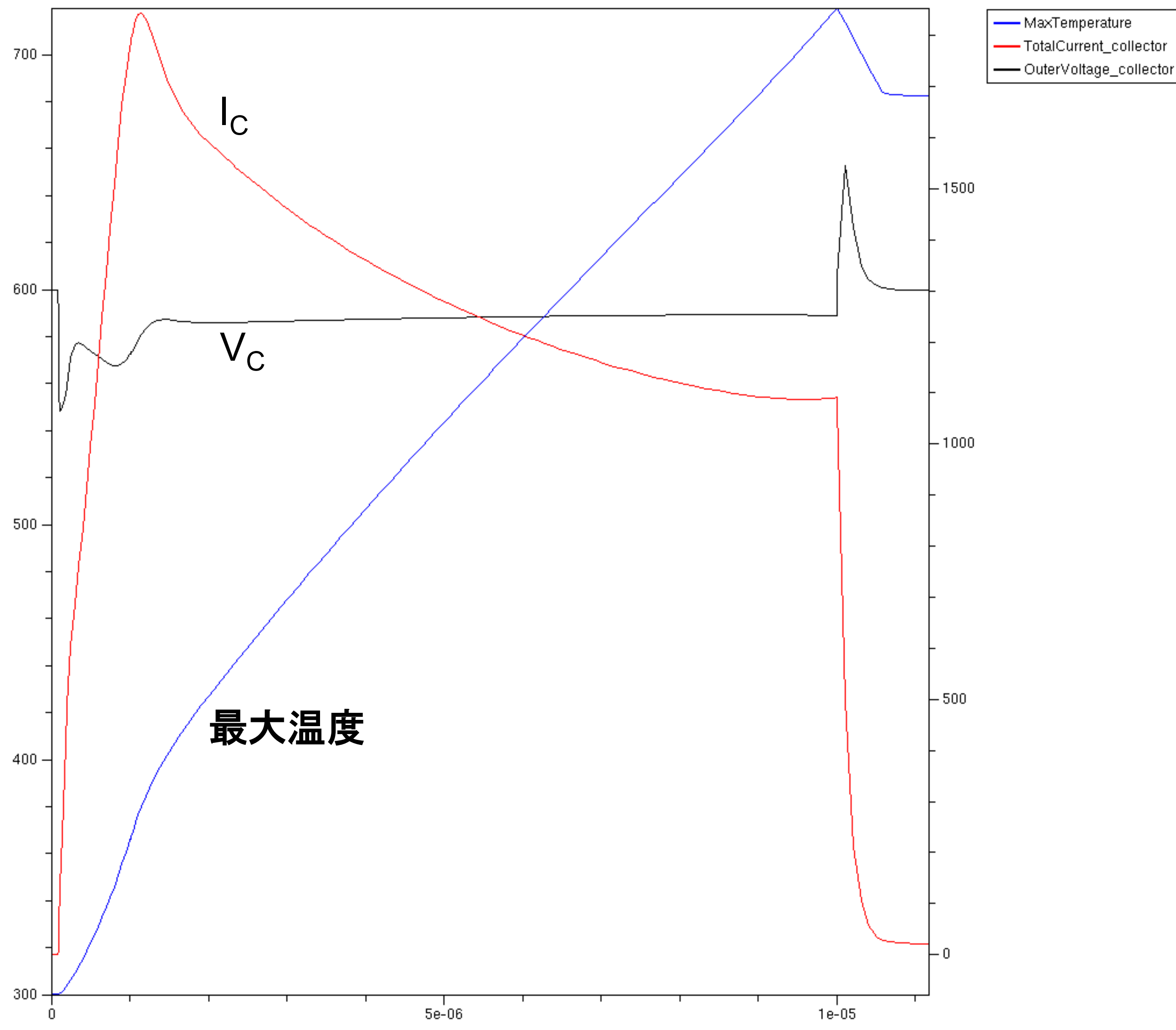
V_C

V_G=15V

V_G=13V

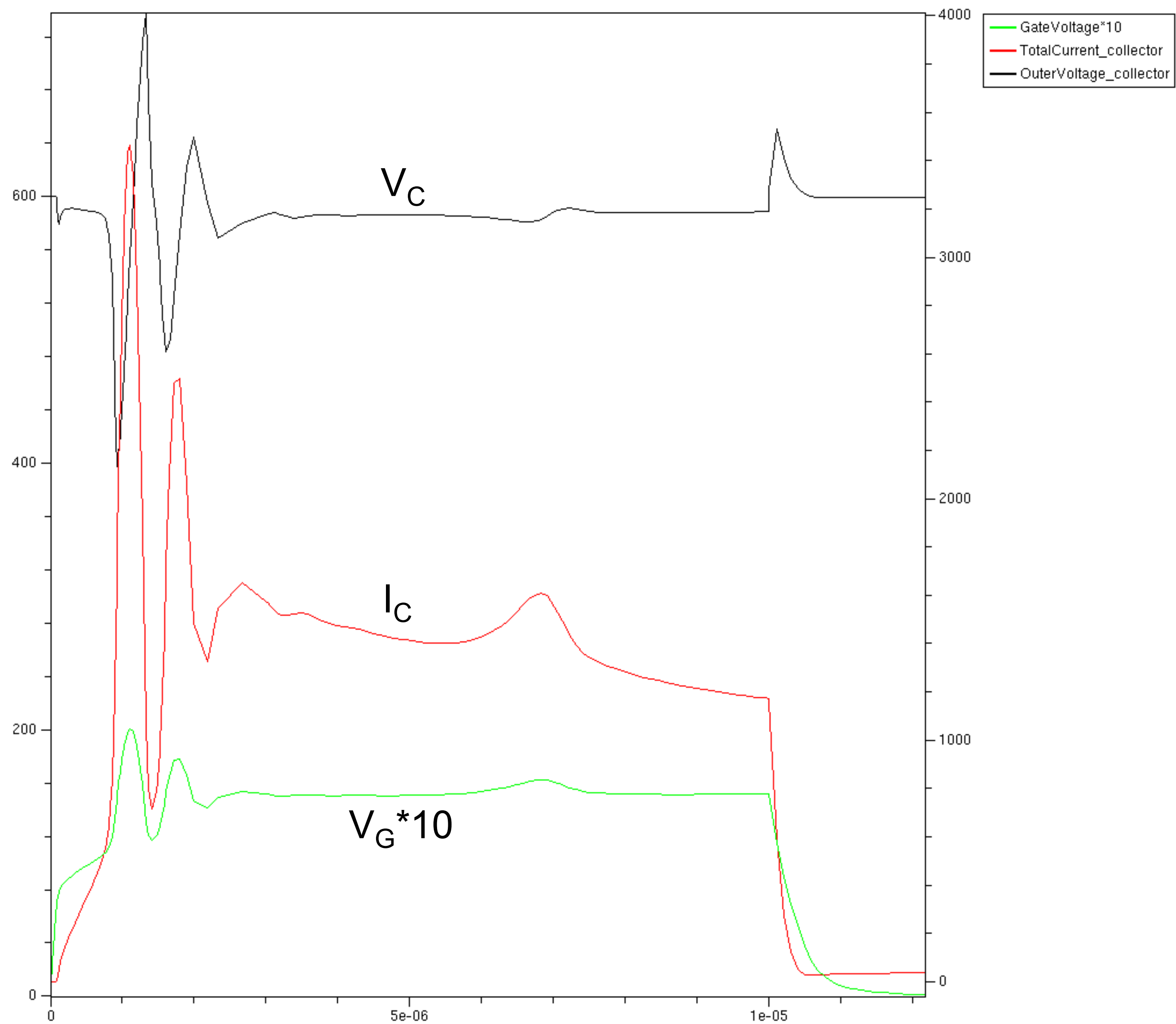


nバッファ：B はOK



振動を増幅しているのはゲート電圧の振動

nバッファ:A



nバッファ:A　　Dummy gate構造は良好！

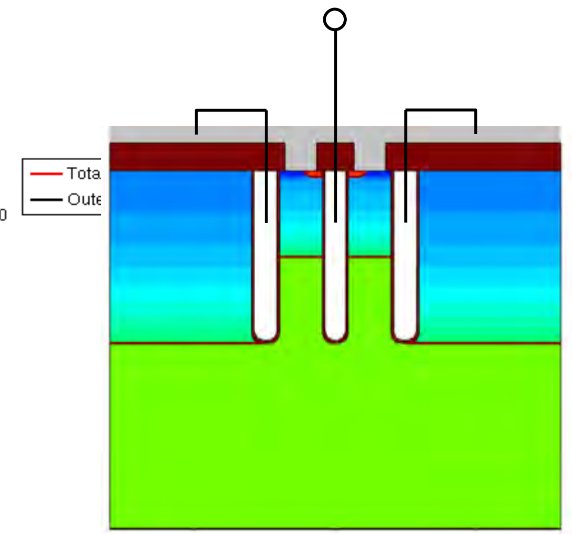
V_C

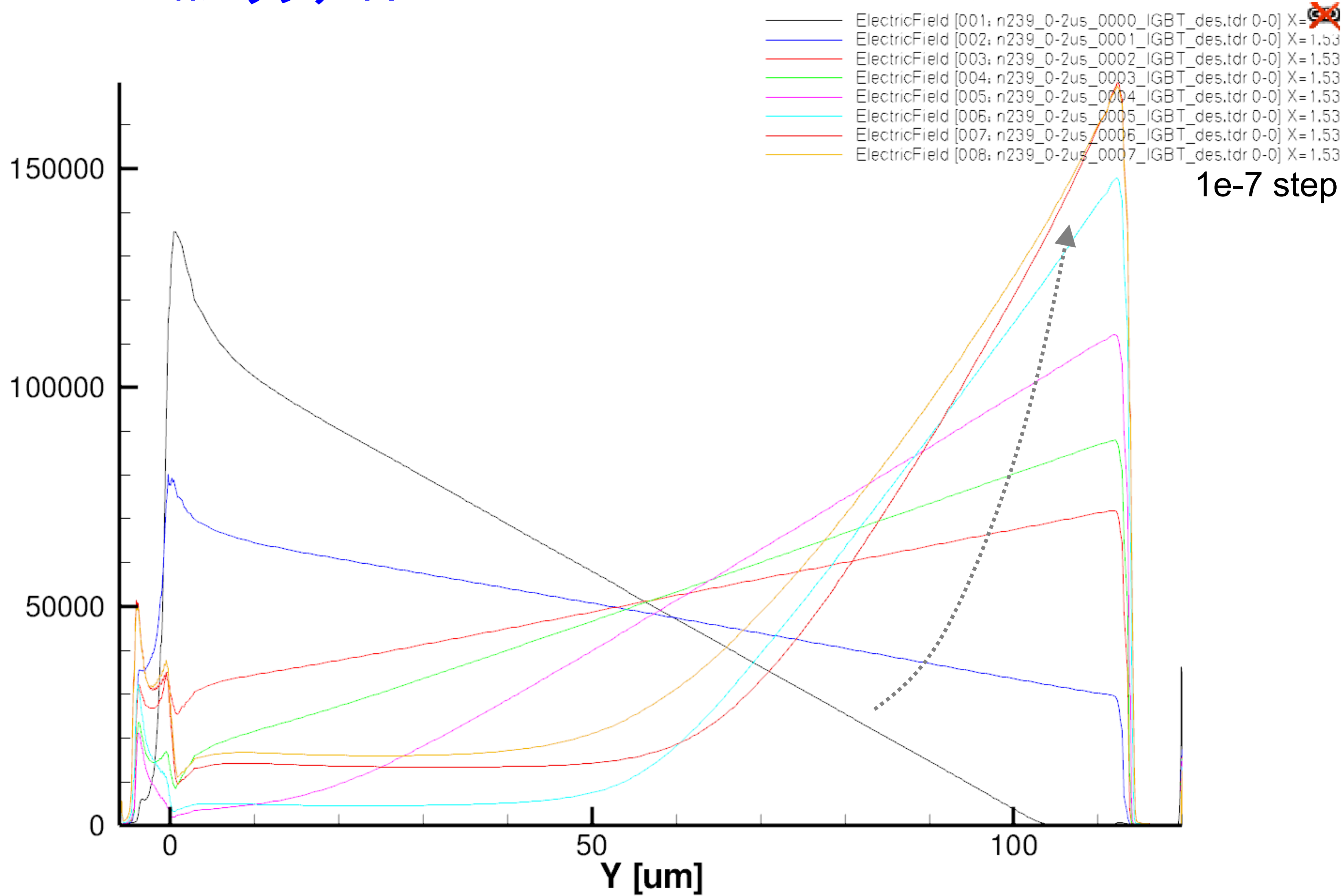
I_C

800
600
400
200
0

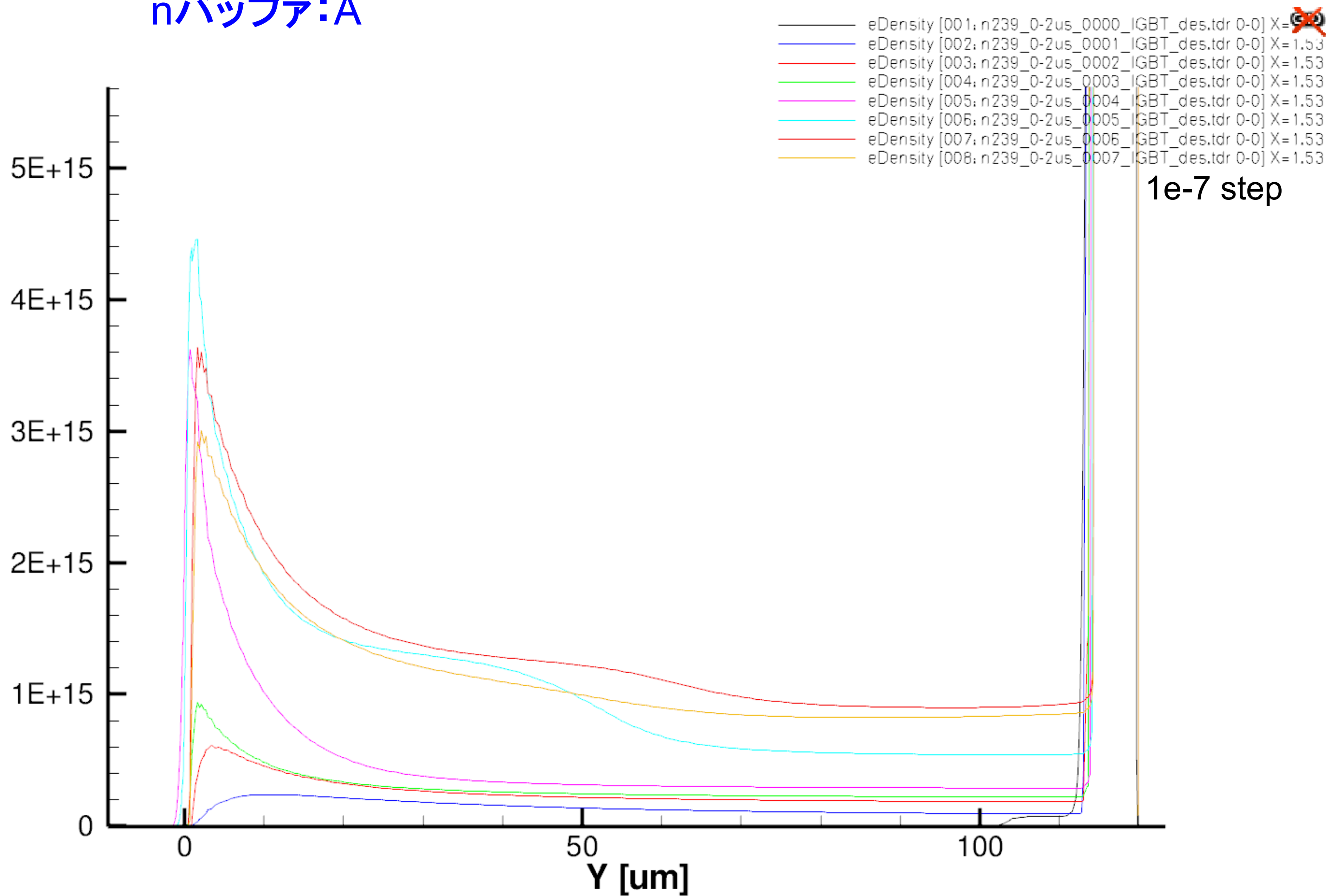
2000
1000
0

0　5e-06　1e-05



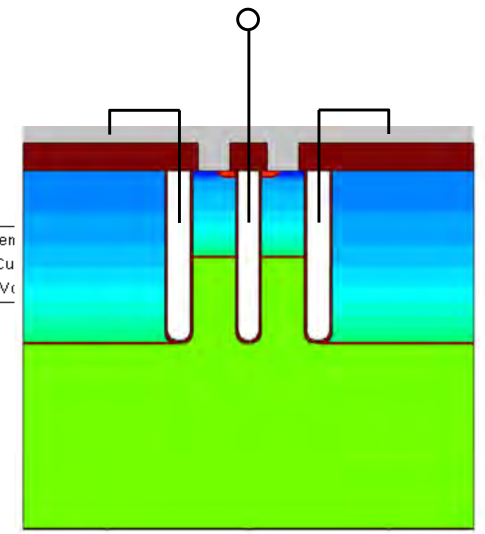


内部電界



電圧が低い時に溜まり、高くなって排出されて電流増大

nバッファ：A



MaxTem
TotalCu
OuterV

800
600
400
200
0
2000
1000
0
0
5e-06
1e-05

最大温度

V_C

I_C

裏面側の温度が急上昇！

nバッファ:A

LatticeTemperature [001: n239_2-8us_0000_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [002: n239_2-8us_0002_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [003: n239_2-8us_0004_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [004: n239_2-8us_0006_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [005: n239_2-8us_0008_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [006: n239_2-8us_0010_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [007: n239_2-8us_0012_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [008: n239_2-8us_0014_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [009: n239_2-8us_0016_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [010: n239_2-8us_0018_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [011: n239_2-8us_0020_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [012: n239_2-8us_0022_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [013: n239_2-8us_0024_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [017: ch_Corrected_Copy_3/n239_09_IGBT_des.tdr 0-0] X=1.38
LatticeTemperature [018: ch_Corrected_Copy_3/n239_10_IGBT_des.tdr 0-0] X=1.38

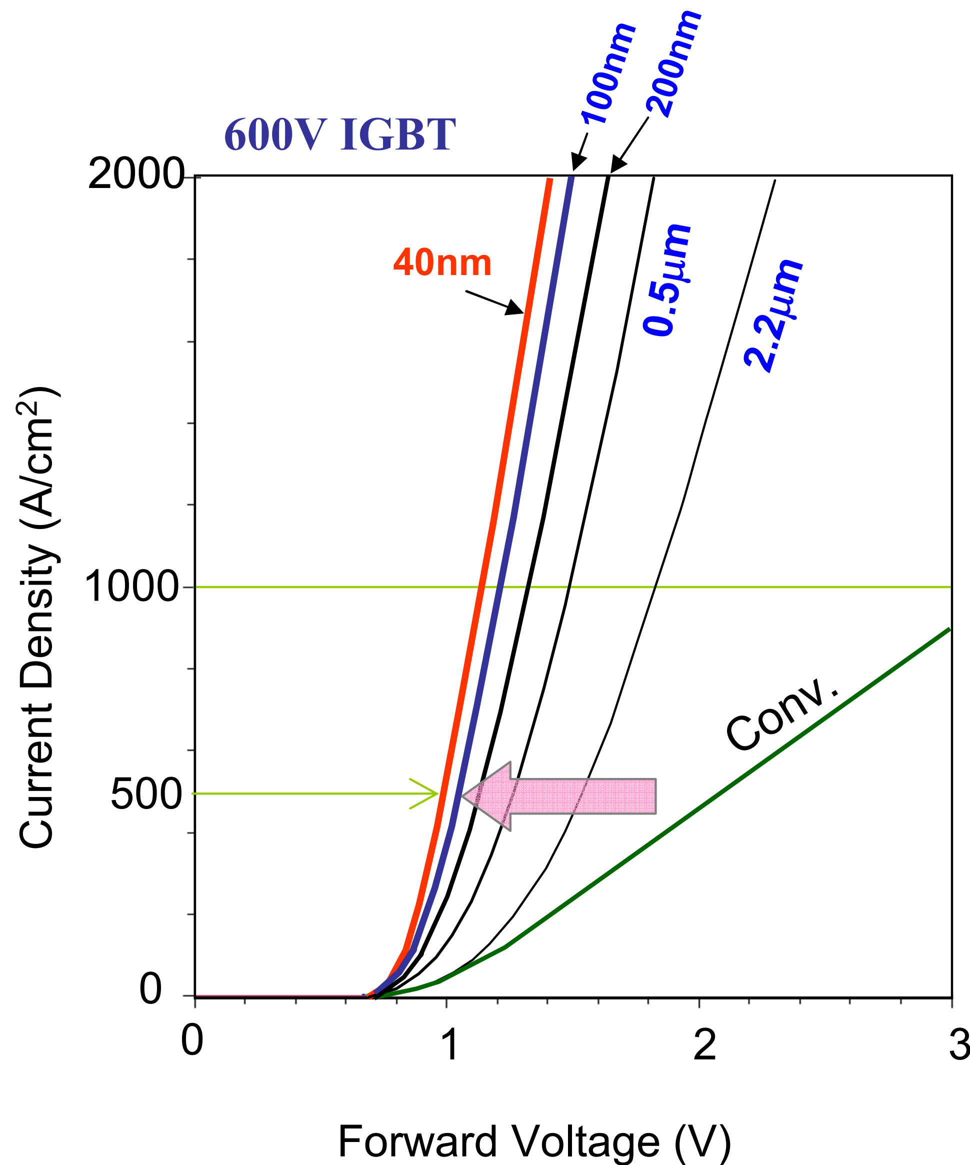
800
700
600
500
400

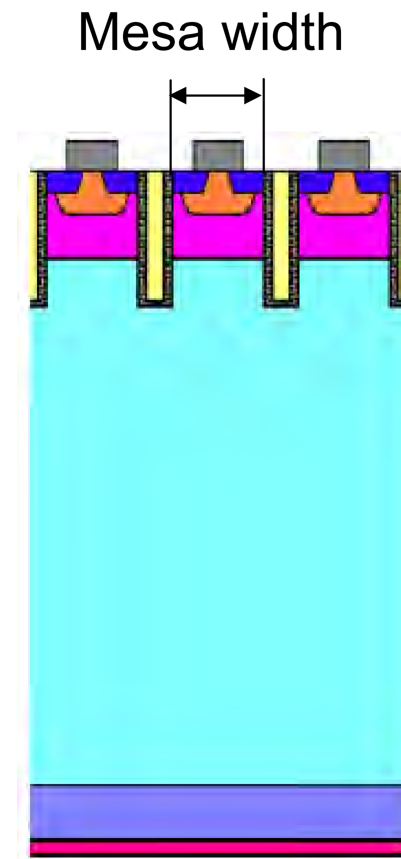
0
50
100

Y [um]

IGBTのシリコン限界に向けた 今後の展開

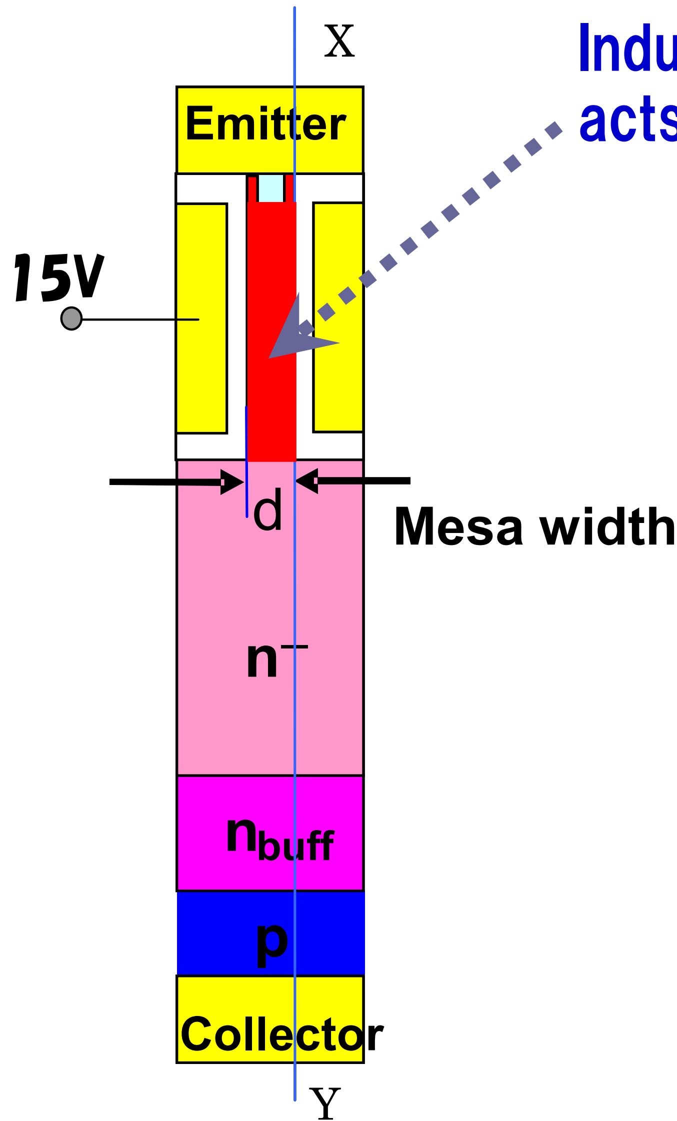
Forward voltage can be greatly improved by reducing mesa width.

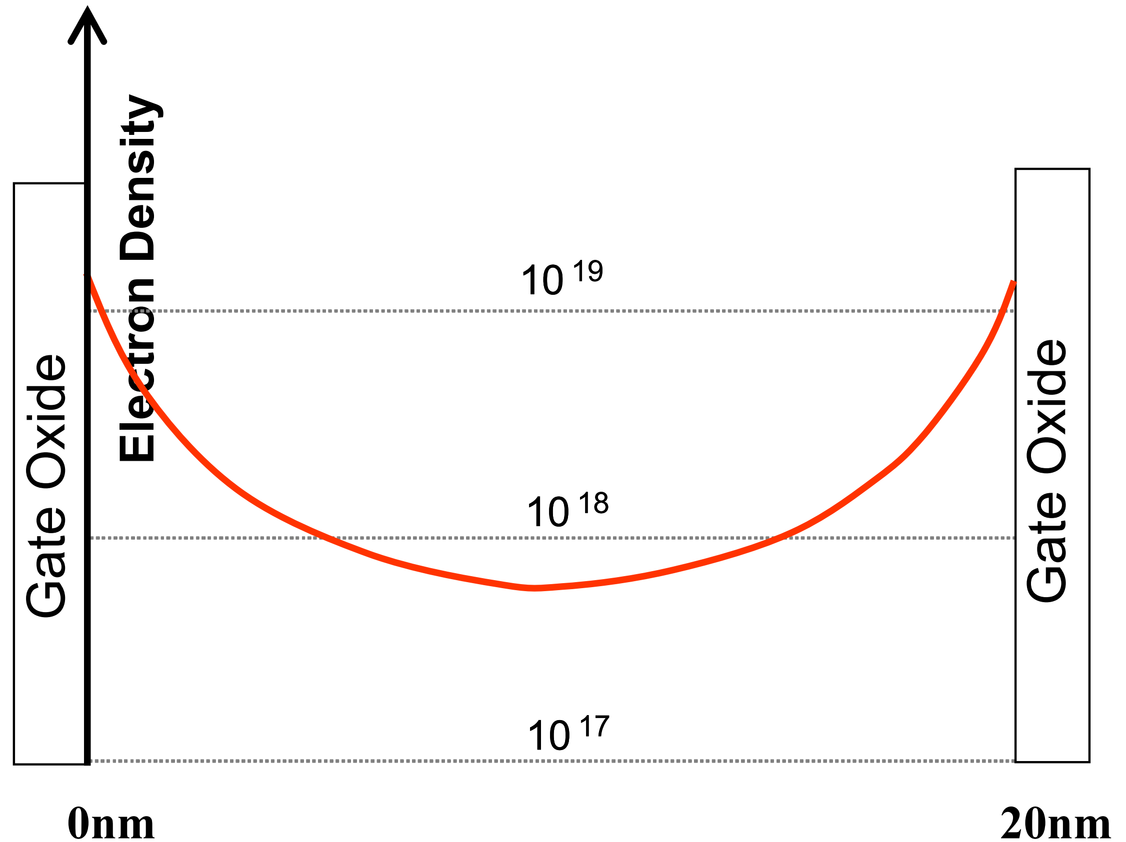




Very Narrow Mesa IGBT

Induced inversion layer
acts as N barrier for holes
→ high injection efficiency > 0.9





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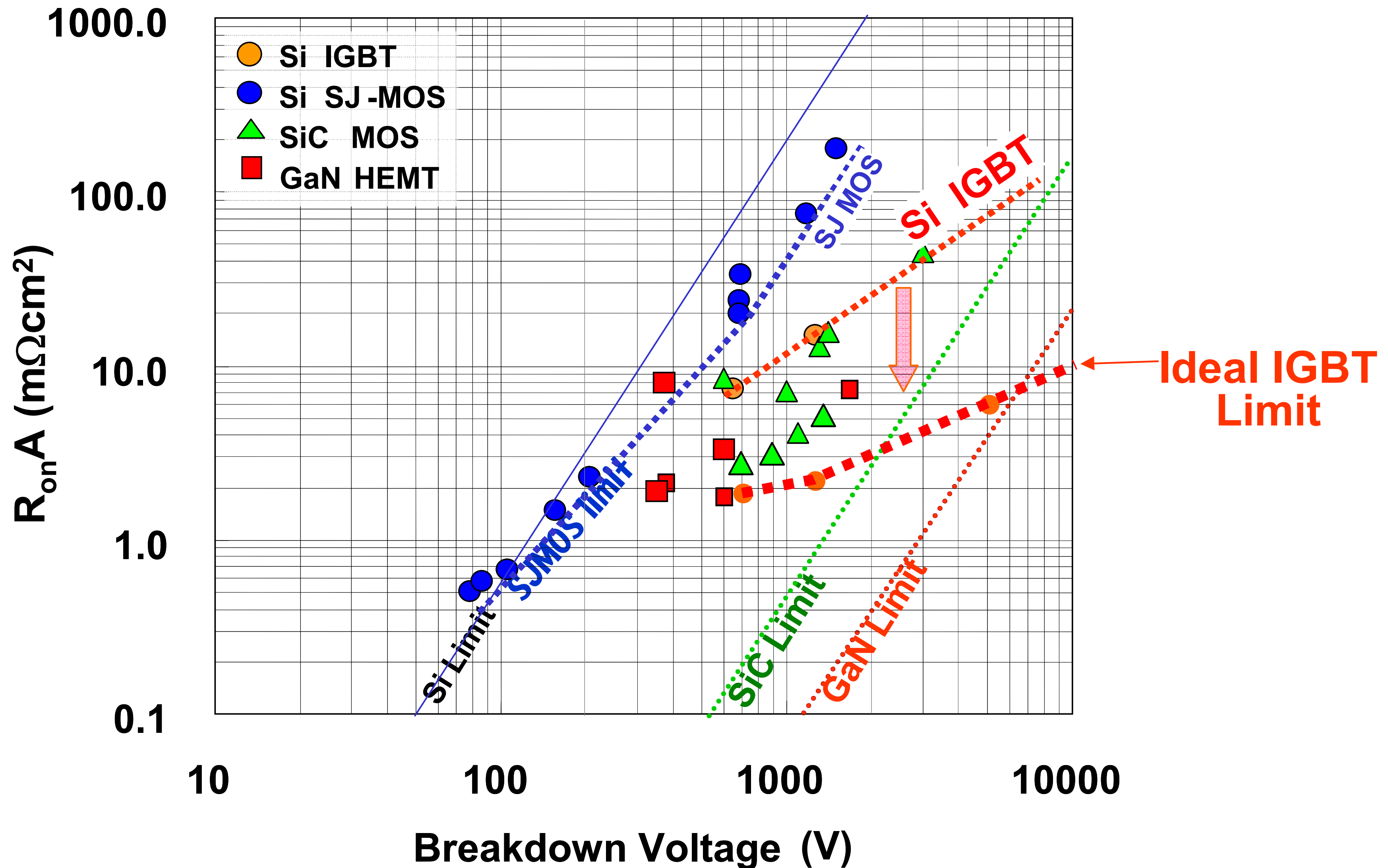
Theoretical limit of IGBT

IGBTs can still be greatly improved in future



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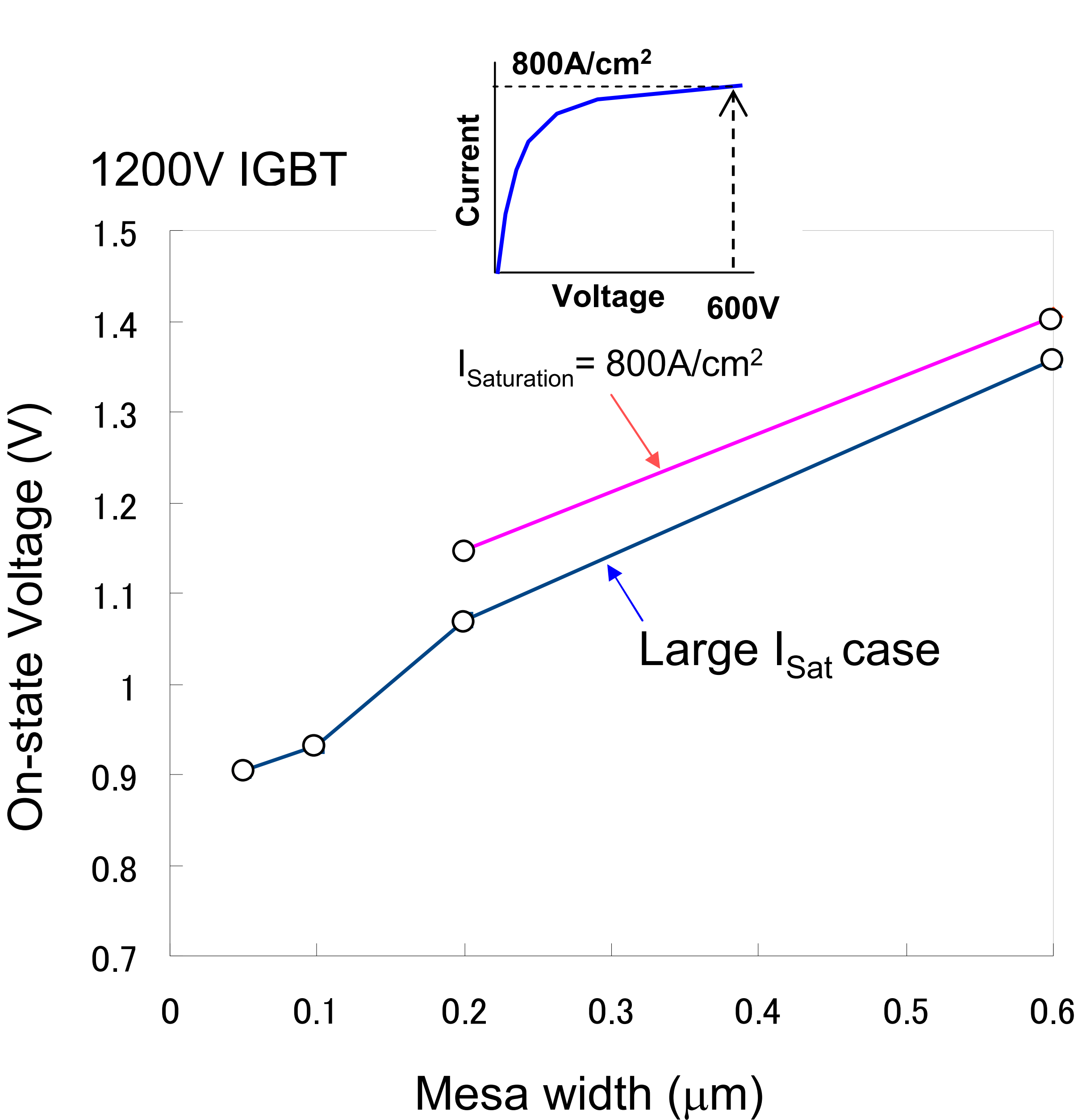
Silicon Limit Analysis based on TCAD for 1200V IGBT

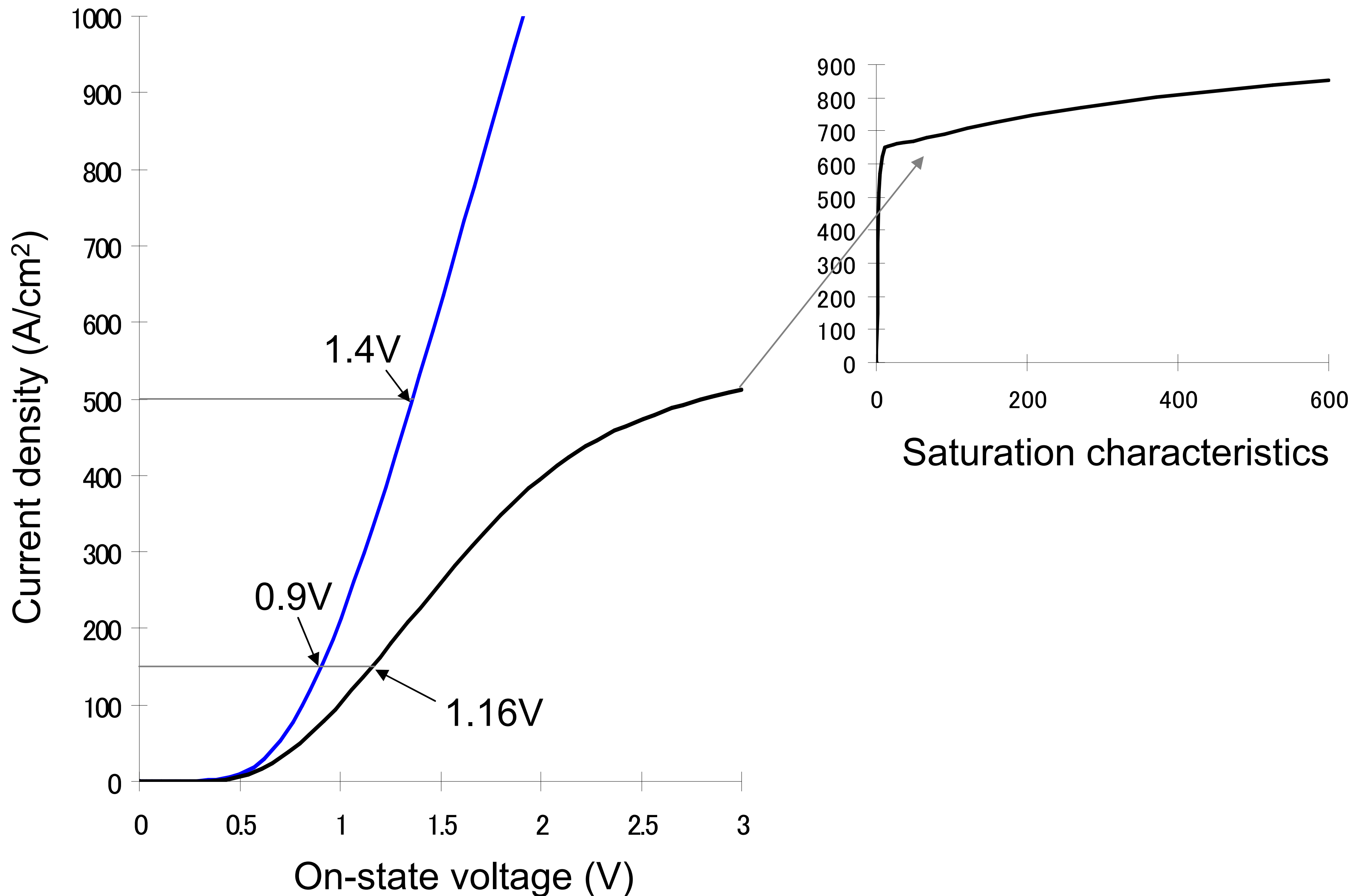


Mesa width

Conditions:
Si thickness=100μm
Current density= 150A/cm2
Temp.=150C
Turn-off loss is fixed at 120μJ/A

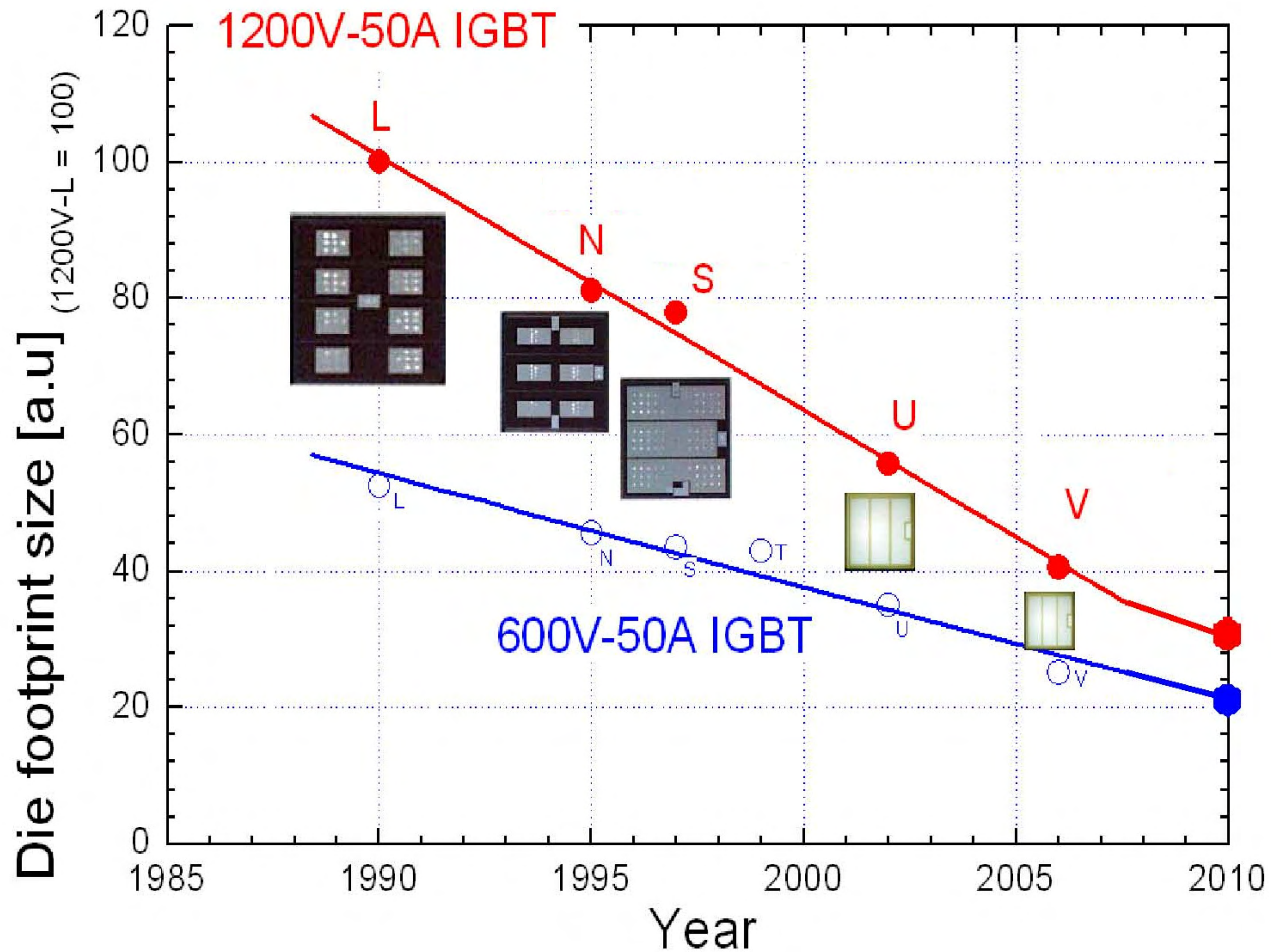
Nakagawa Consulting Office, LLC.

Typical current-voltage relation for optimized IGBTs

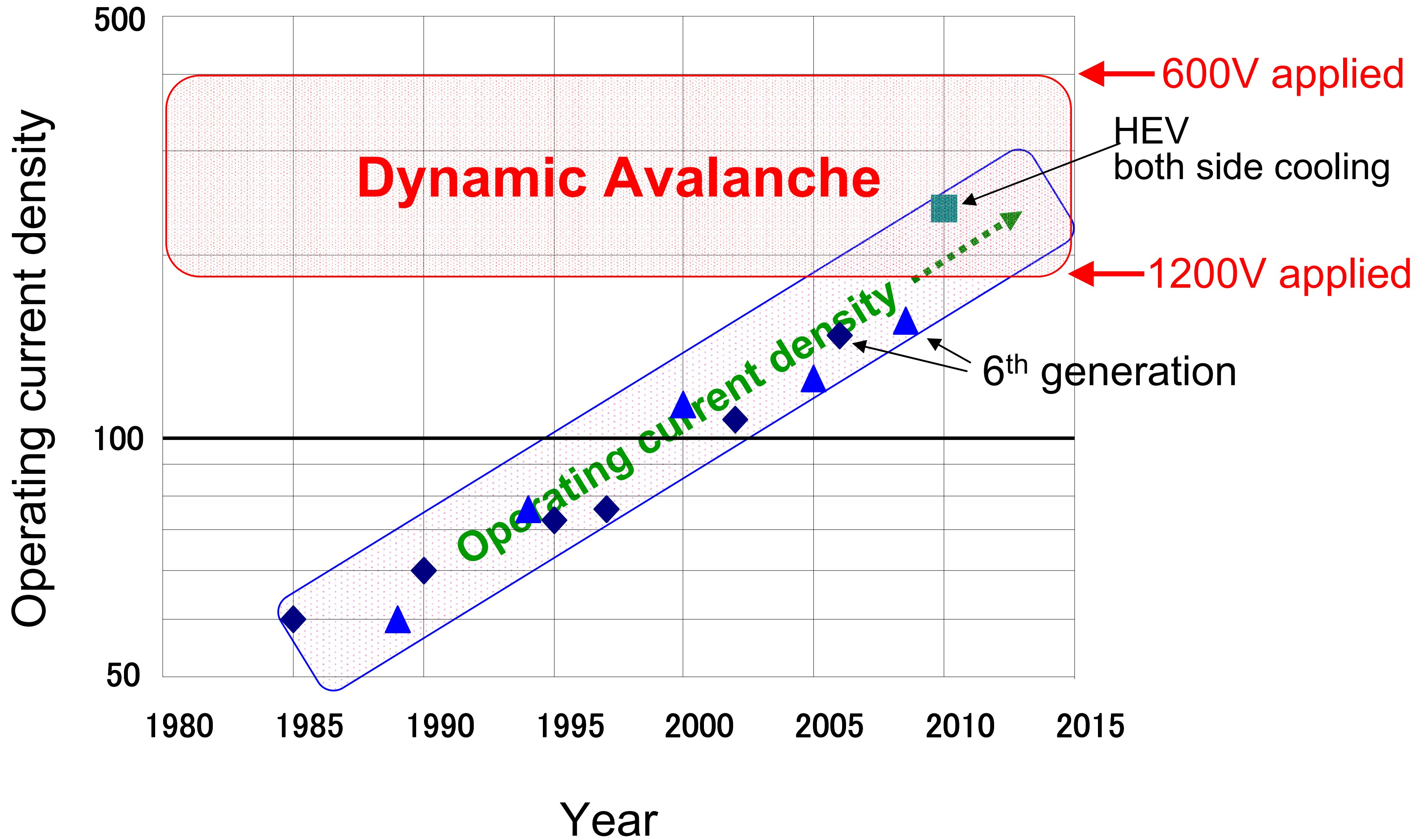


It is important to make use of IGBT chips with large saturation current. Modules should have short-circuit protection function so that low on-state voltage chip can be used for multi-purpose module.

IGBT Chip footprint as a function of year



1200V IGBT operating current density



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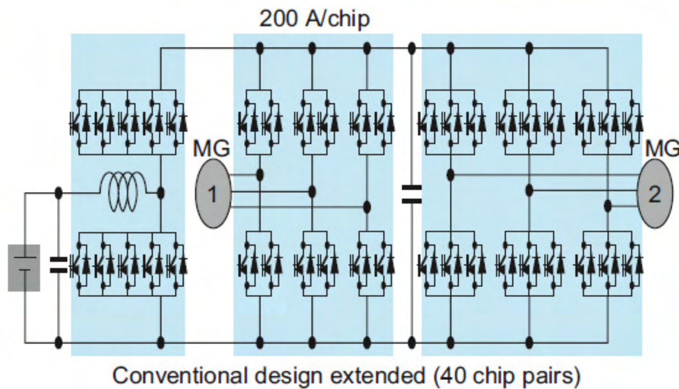
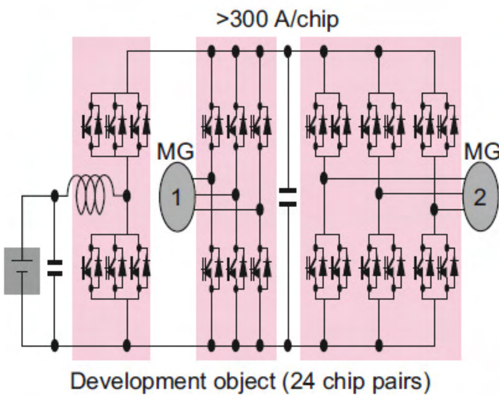
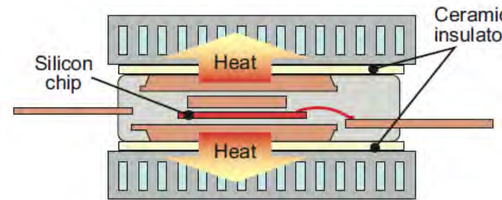
HEVパワーコントロールユニット小型化

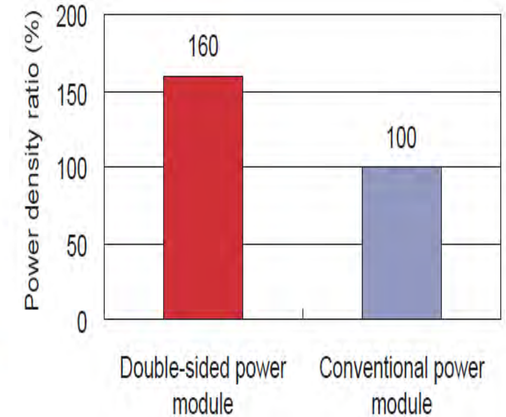
小型実装：両面冷却で高出力化

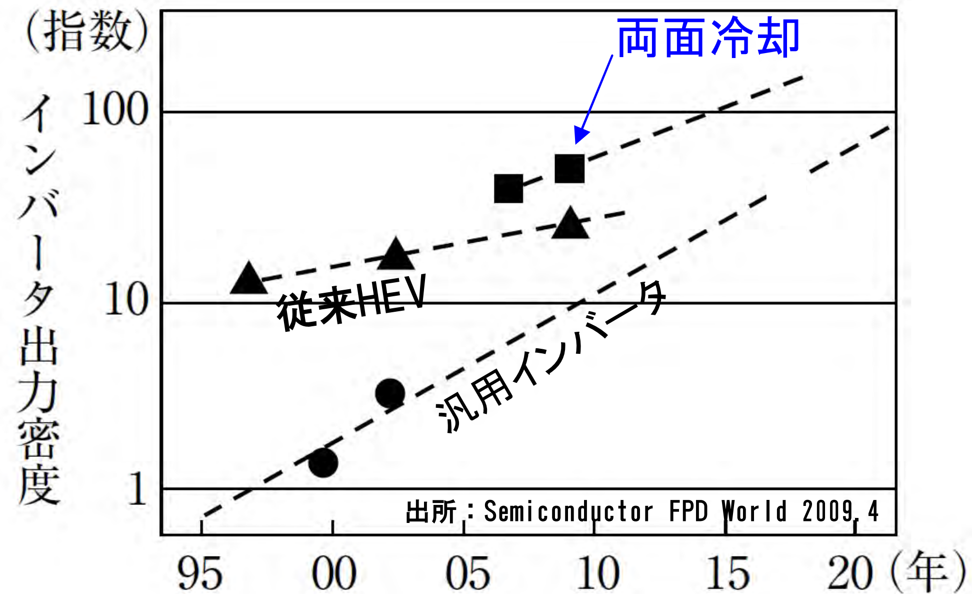




IGBT両面冷却





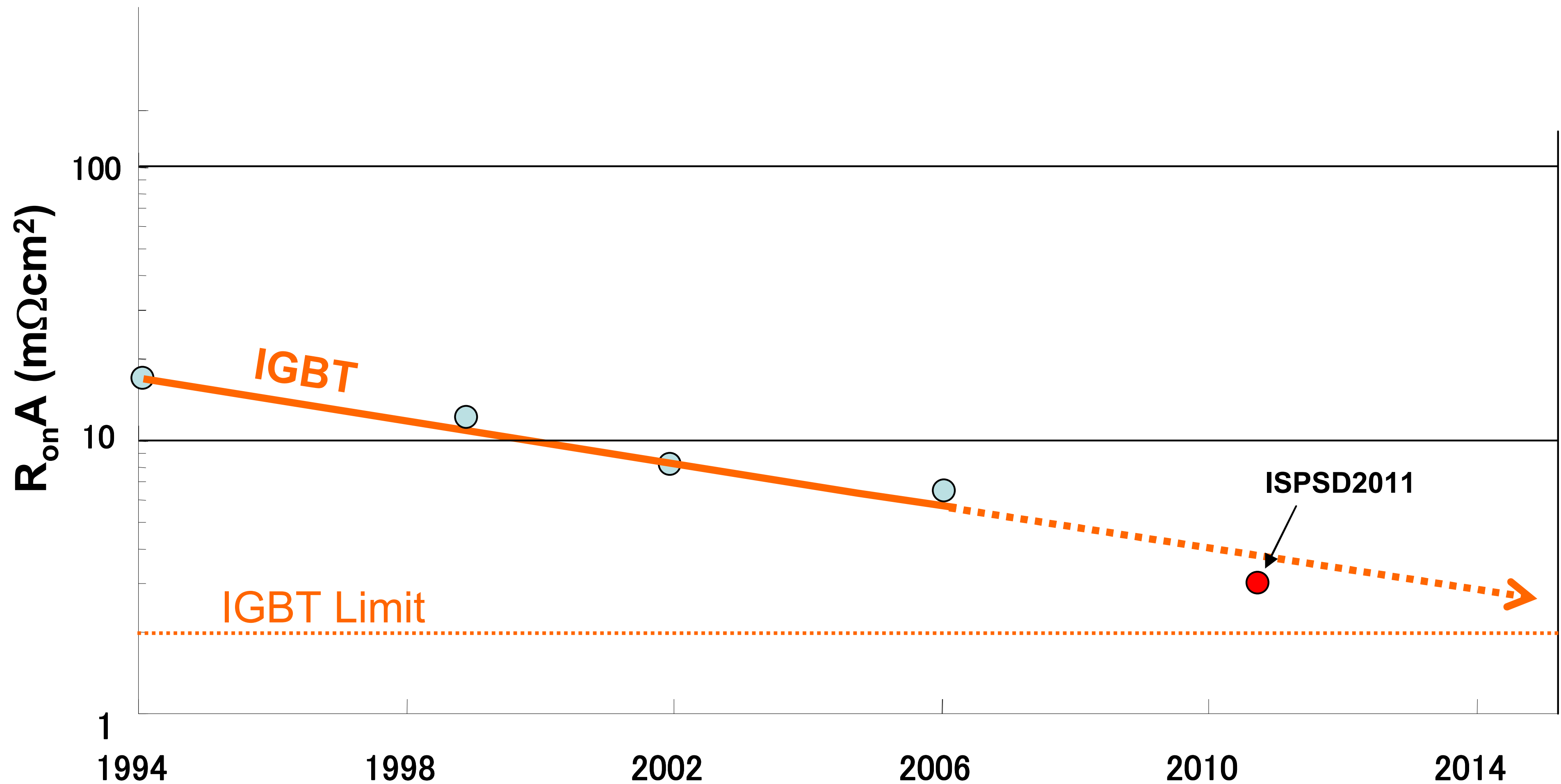


・1Chip当たりの電流を200Aから300Aに増大。
・チップ数を増やさず大容量化。

出典：デンソーテクニカルレビュー　Vol. 14　2009

Trends of 600V IGBT

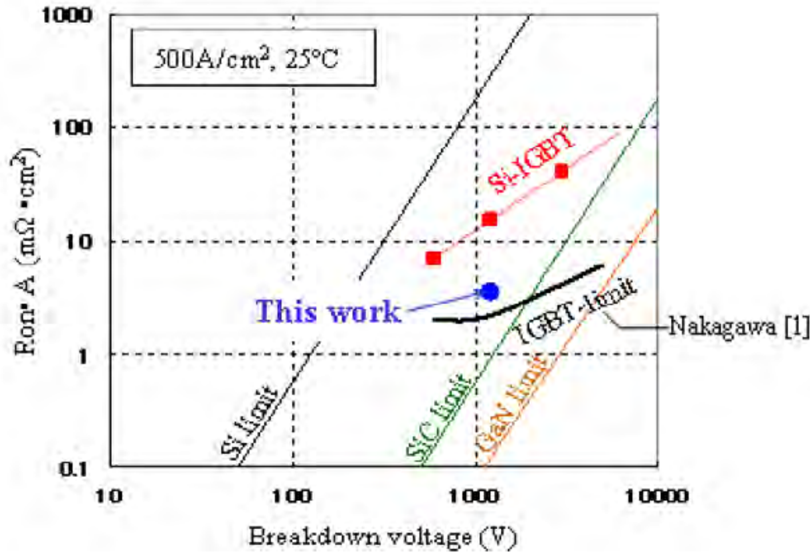
IGBT On-resistance has been steadily improved In the past,
It is predicted that it will approach the IGBT limit in near future.

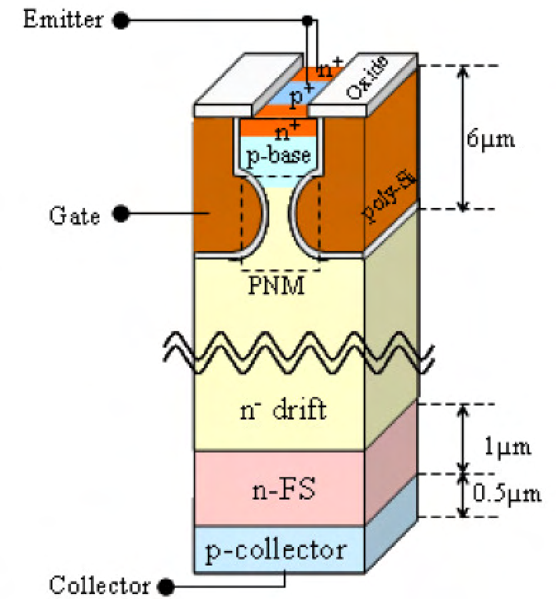


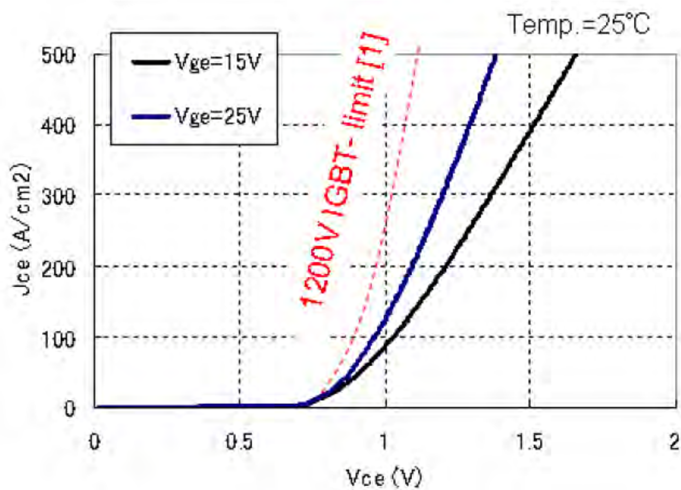
Low loss IGBT with Partially Narrow Mesa Structure (PNM-IGBT)

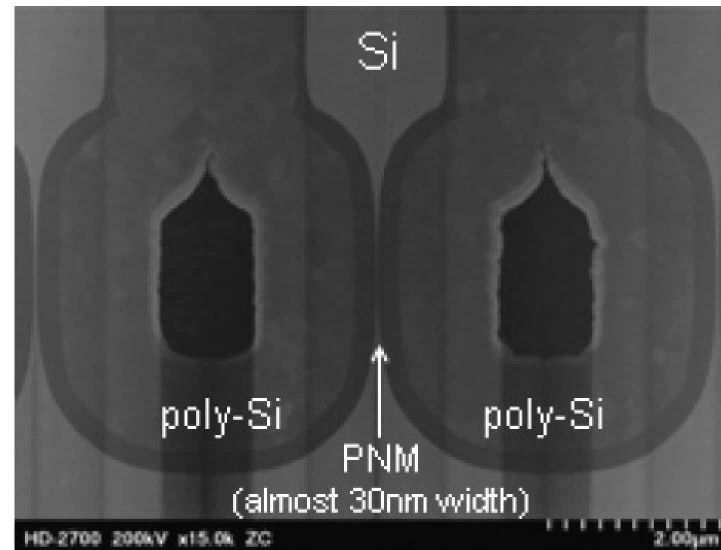
ISPSD' 12

Masakiyo Sumitomo, Junichi Asai, Hiroki Sakane, Kazuki Arakawa, Yasushi Higuchi and M
DENSO CORPORATION
ch Laboratories
:hi, 470-0111, Japan
mitomo@denso.co.jp

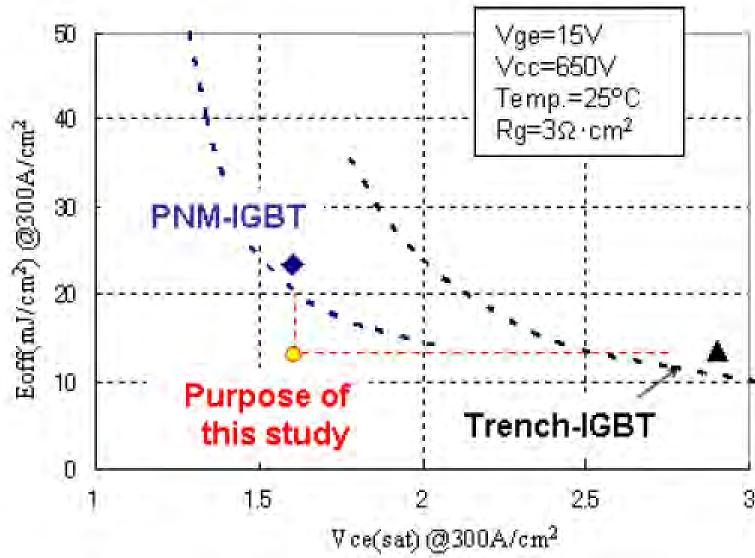


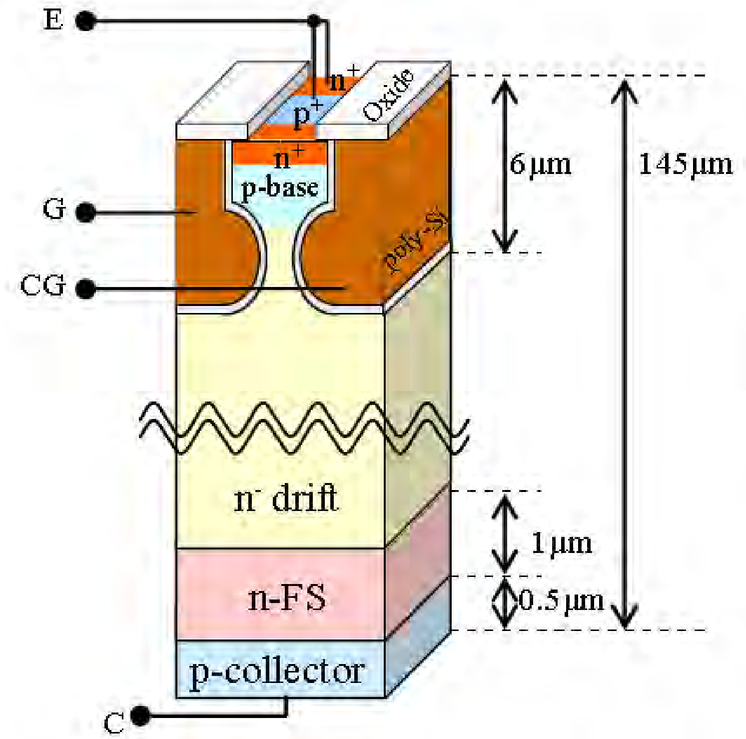


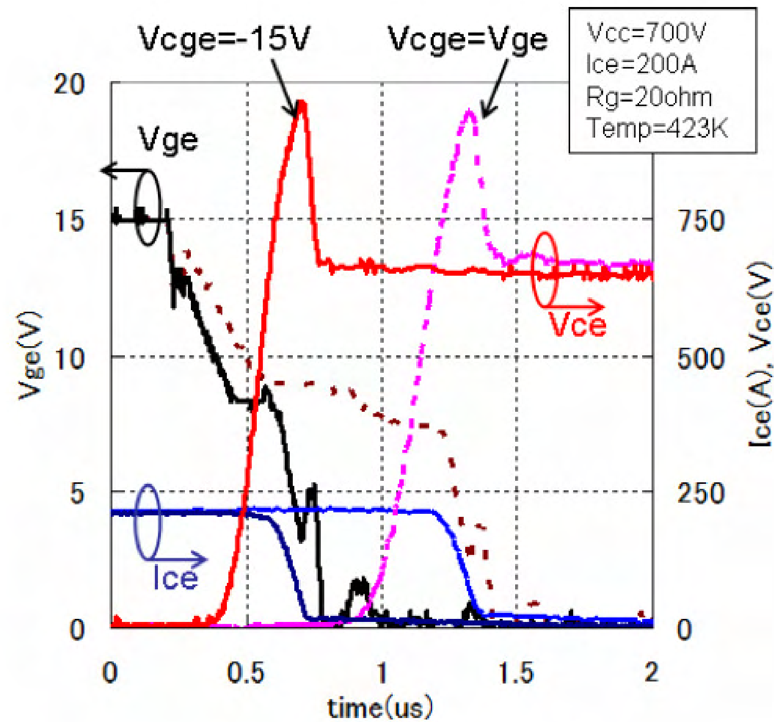




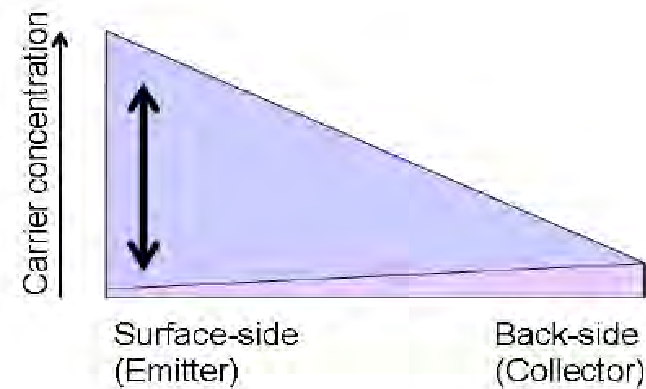
Cross-Sectional TEM image of the prototype







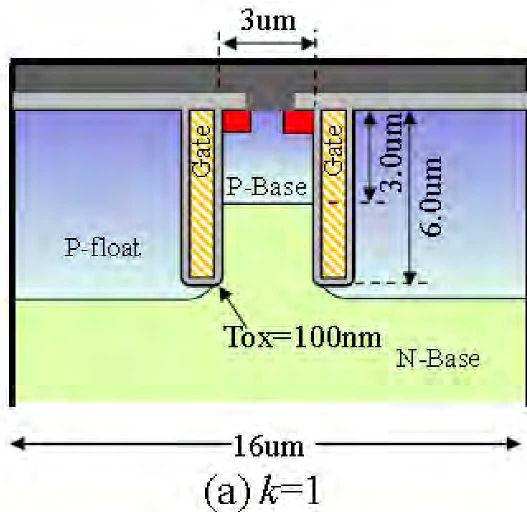
Measured turn-off waveforms

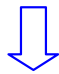


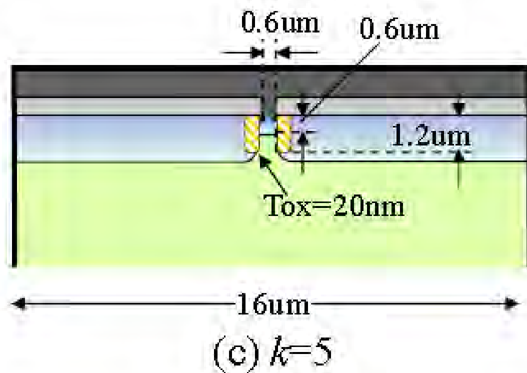
Scaling Rule for Very Shallow Trench IGBT toward CMOS Process Compatibility

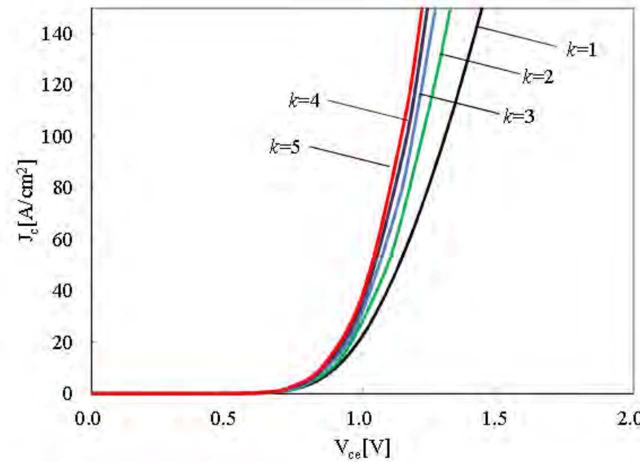
ISPSD' 12

Masahiro Tanaka and Ichiro Omura
Kyushu Institute of Technology

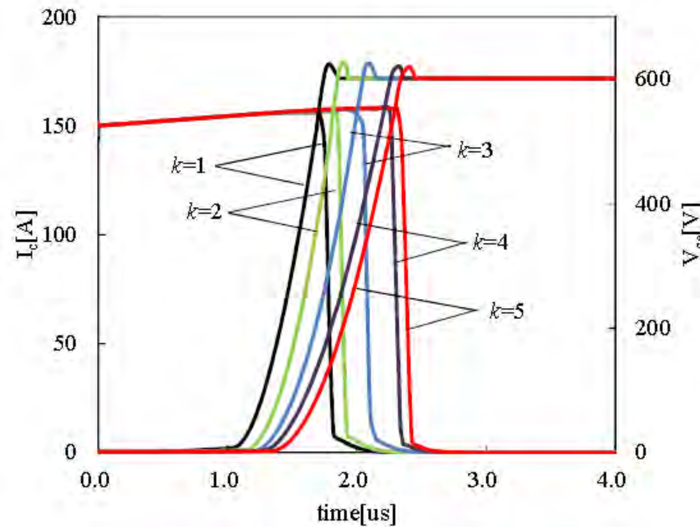


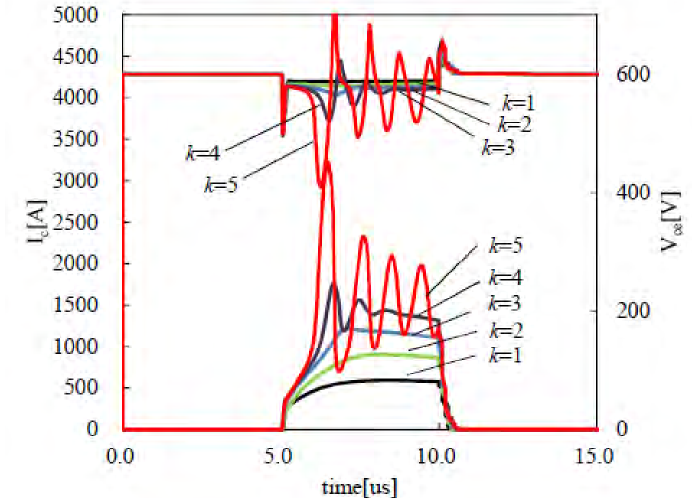






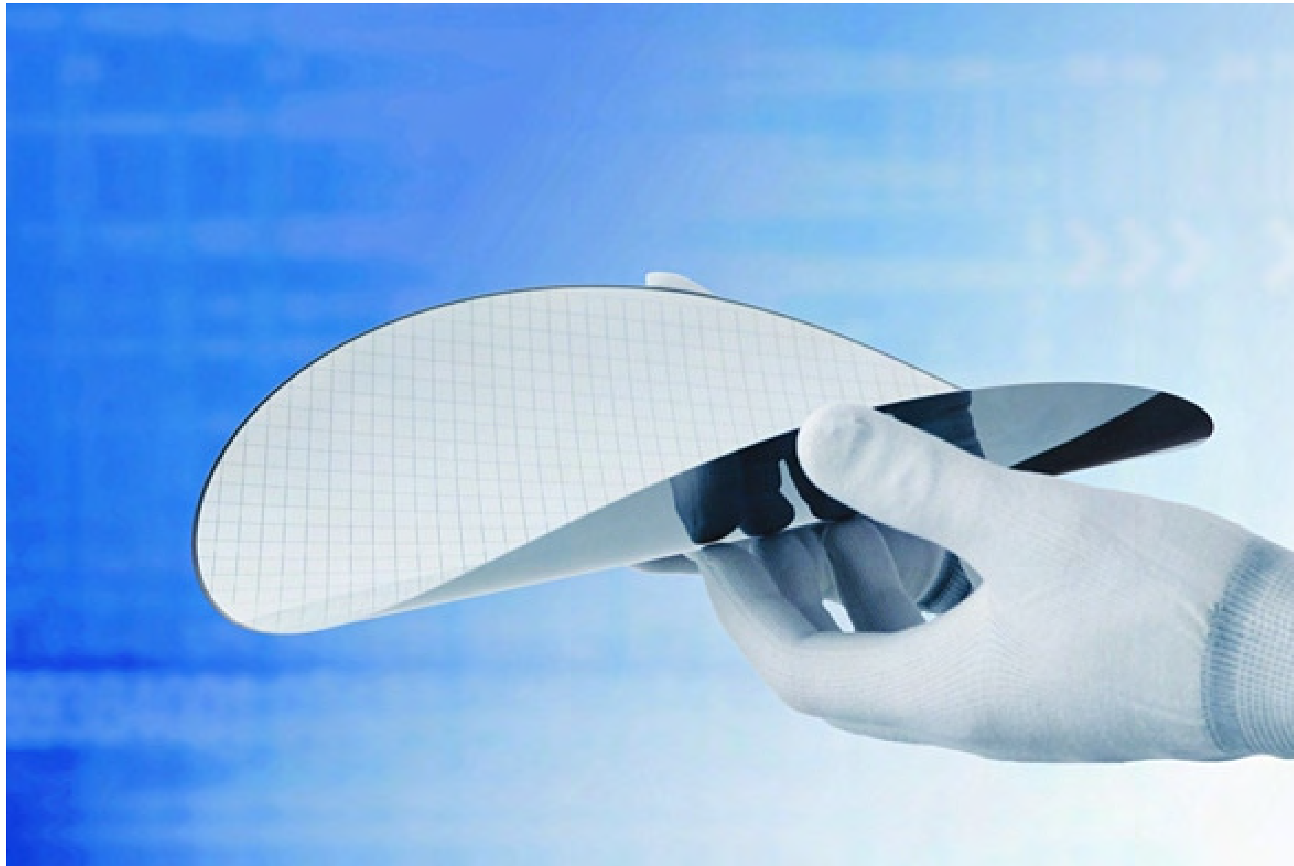
浅いトレンチゲートでも良好な特性。
CMOS Fab.で IGBT生産可能





30cm CMOS Fab for Power Devices

contributes to better performance and low cost.



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約 779,000 件（0.22 秒）

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www.ne.jp/asahi/capri/ocean/

中川コンサルティング事務所 パワーデバイス・パワーICの設計をお手伝いします。・連絡先E-mail: akio.nakagawa@nifty.com 論文のダウンロードができます。マウスで右クリックして"対象をファイルに保存"を選んでください。・New 2012年10月25,26日 浜松 ...

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