Japanese Journal of Applied Physics

The Japan Society of Applied Physics

REGULAR PAPER

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Japanese Journal of Applied Physics 59, SGGD01 (2020) **REGULAR PAPER**
https://doi.org/10.7567/1347-4065/ab5b3a

Impact of 3D simulation on the analysis of unclamped inductive switching

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Received October 1, 2019; revised October 29, 2019; accepted November 25, 2019; published online January 27, 2020

Unclamped inductive switching (UIS) is a crucial topic for modern power devices. The UIS failure analysis has been done by 2D Technology CAD (TCAD) simulations due to the restrictions of computation capabilities. In this paper, the detailed UIS failure mechanism for IGBT was analyzed by large scale 3D TCAD simulations. The authors propose that there are two kinds of current filaments. These are avalanche induced current filament and temperature induced current filament. The avalanche induced current filament firstly developed and moved around during the UIS operation. It finally caused local latch-up. The local temperature rapidly increased by the latch-up. This triggered a destructive temperature induced current filament, which stayed in the same location and caused device failure. It was also found that these phenomena were accurately treated only by large scale 3D simulation of at least 160 μm $\times$ 160 μm device area.

1. Introduction

IGBT is widely used in the middle to high power area in the power semiconductor device field. The demand for IGBT increases especially for new generation vehicles such as hybrid electric vehicle and electric vehicle. In order to enlarge the power density of the systems, high current density is required for modern IGBT. The unclamped inductive switching (UIS) capability is one of the crucial topics in the development of the power devices. During the UIS operation, a large avalanche generation continuously occurs in the device by applying an energy from charged unclamped inductor. Large UIS capability is an index of the device robustness.

Many researches have been performed to analyze UIS failure mechanism of IGBTs by TCAD simulations. In 1990s, the research started with 2D single cell isothermal simulations.[1)] Then 2D single cell electro-thermal simulations[2–5)] have been executed in order to precisely consider the avalanche generation, which has strong dependency on the lattice temperature. Since 2000, 2D multi-cell isothermal simulations have been performed to reproduce current filament formation during UIS. It was discussed that the current filament drastically degrades UIS capability.[6–10)] Furthermore, the filament dynamics have been discussed by using 2D multi-cell electro-thermal simulations.[11–15)] Different approaches such as Quasi-3D simulation,[16)] prediction from half-cell simulation,[17)] full chip simulation using network model,[18)] and 3D single cell electro-thermal simulation[19)] were also reported. On the other hand, it was experimentally observed[20–25)] that the current filaments are formed and they move around inside the IGBT chip during UIS.

However, because of the limitation of these modeling and simulation capabilities, large scale 3D electro-thermal simulation has not been done yet. Thus, detailed failure mechanism has not been discussed yet. The purpose of this work is to clarify the failure mechanism by large scale 3D TCAD simulations. Our related report[26)] proposed that there are two kinds of current filaments. These are avalanche induced current filament and temperature induced current filament, which are relevant to the UIS failure. During the UIS operation, the avalanche induced current filaments firstly develop and move around. They finally turn into one large current density filament and causes local latch-up by high hole current density in the P-base. The latch-up causes huge local temperature increase in the P-base inside the filament. This triggers temperature induced current filament, which stays in the same location and causes device failure. 3D filaments occur even if the device is completely homogeneous and uniform. The current filament dynamics can accurately be treated only by large scale 3D simulation because it is basically 3D phenomenon. The UIS failure energy calculated by large scale 3D simulation agrees with the observed value in the datasheet.

In this paper, we expand the discussion of UIS failure mechanism by deeply analyzing the 3D TCAD simulation results. The dynamics of the avalanche induced current filament and the temperature induced current filament are discussed individually. Furthermore, the simulation device size dependency is discussed in more detail. In the small scale 3D simulations, the avalanche induced current filaments keep moving and do not turn into large current density filament. The amount of the current density in the avalanche induced current filament is not large enough to cause local latch-up. Thus, the lattice temperature increases globally. In result, the failure energies of the small scale simulations are much larger than that of the large scale 3D simulation.

2. TCAD simulation setup

Multi-cell 3D TCAD simulations[27–29)] were performed with taking into account self-heating effect. Synopsys TCAD Sentaurus was used for the simulations. The device structure is shown in Fig. 1. The footprint of the simulated structure is 160 μm $\times$ 160 μm. The multi-cell structure was created by repeatedly reflecting 10 μm $\times$ 10 μm of half-cell IGBT structure for width and length directions (W_{Sim} and L_{Sim} directions in Fig. 1, respectively). It has completely symmetrical mesh. The IGBT is 1.2 kV rated. The device structural parameters are summarized in Table I.

The physical models used for the TCAD simulations are summarized in Table II. The thermodynamic carrier transport model was used in addition to the drift-diffusion transport model. The thermal resistance of 0.3 K W^{-1} was set between the collector electrode, which is located on the bottom of the device, and the heat-sink. The heat-sink temperature was set

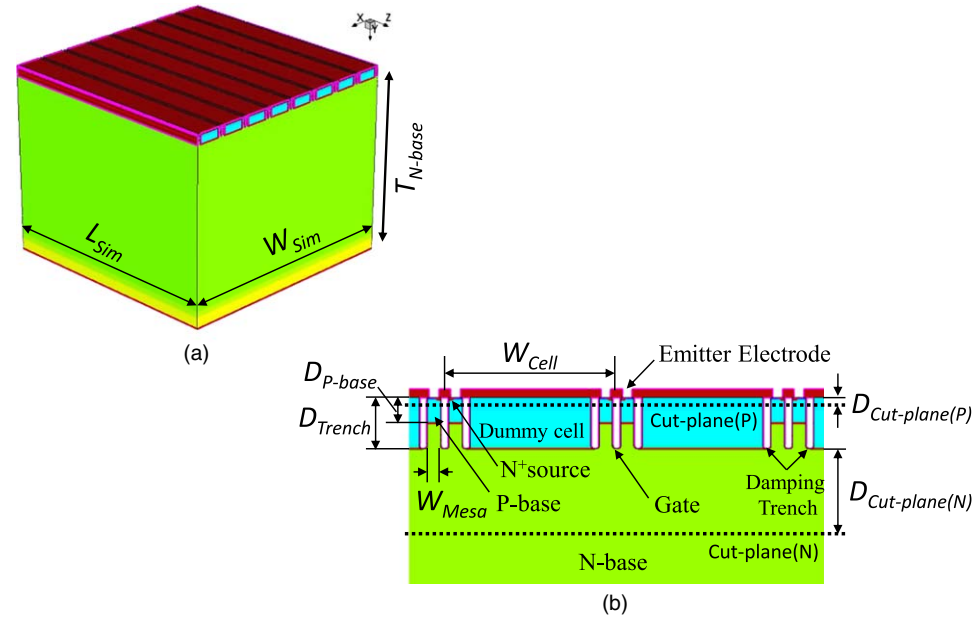

Fig. 1. (Color online) (a) Simulated 3D IGBT structure. The final multi-cell structure is created by repeatedly copying a half unit-cell structure. (b) Cross sectional view in the depth direction of the simulated structure.[30] The cut-planes: (P) and (N) in the figure are used to plot avalanche, temperature and current distributions in Figs. 4, 8, 9, and 11.

Table I. Device structural parameters.

N-base thickness $T_{\text{N-base}}$	120 μm
Simulated device width W_{Sim}	160 μm
Simulated device length L_{Sim}	160 μm
Unit-cell pitch W_{Cell}	20 μm
Mesa width W_{Mesa}	1.5 μm
P-base depth $D_{\text{P-base}}$	3 μm
Trench depth D_{Trench}	6 μm
Depth of cut-plane(P) from the silicon surface $D_{\text{Cut-plane(P)}}$	1 μm
Depth of cut-plane(N) from the trench bottom $D_{\text{Cut-plane(N)}}$	10 μm

Table II. Physical models used in the TCAD simulations.

Model category	Models
Carrier transport	Drift-diffusion
	Thermodynamic
Intrinsic density	Bandgap narrowing
Mobility	Temperature dependence
	Doping concentration dependence
	High electric field dependence
	Carrier-carrier scattering effect
	Normal electric field dependence in the MOS channel
Generation-recombination	Schockley–Read–Hall (Electron lifetime = 10 μs, Hole lifetime = 3 μs)
	Auger
	Avalanche (University of Bologna Model)

at 400 K. The simulation included the mobility degradation models of lattice temperature dependence, high field saturation and carrier–carrier scattering. The temperature dependence of the physical models must be carefully considered to accurately reproduce the device phenomena during the UIS operation. The University of Bologna avalanche model,[31] which is well calibrated for wide range of the lattice temperature, was adopted.

The UIS test circuit is shown in Fig. 2. The turn-off current and applied voltage were set at 400 A cm^{-2} and 800 V, respectively. The gate voltage was controlled from +15 to −15 V. The load inductance was varied to change the sustaining period.

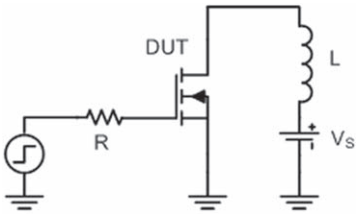

Fig. 2. UIS test circuit.

3. Results and discussion

3.1. Results

3.1.1. Current filament formation and UIS failure. Calculated UIS waveforms of 160 μm × 160 μm device are shown in Fig. 3. The figure includes the waveforms of the maximum P-base temperature as well as the

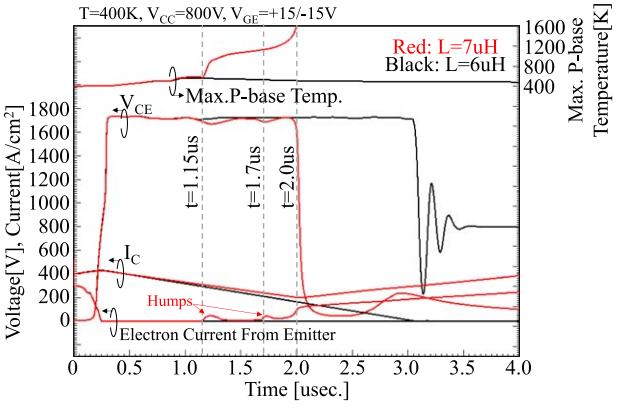

Fig. 3. (Color online) Calculated UIS waveforms of $L = 6\,\mu$H and $L = 7\,\mu$H. The device succeeds in turning-off the collector current when $L = 6\,\mu$H but fails when $L = 7\,\mu$H. In case of $L = 7\,\mu$H, electron current injection starts at $t = 1.15\,\mu$s. The device fails at $t = 2.0\,\mu$s.

waveforms of the electron current from the emitter electrode, which can be used as an indication that latch-up occurs somewhere in the chip. It is shown that the IGBT fails to turn-off 400 A of current when $L = 7\,\mu$H, whereas it succeeds when $L = 6\,\mu$H.

In the case of $L = 7\,\mu$H, the electron current started to be injected at $t = 1.15\,\mu$s, in the other words, latch-up occurred. Then the lattice temperature increased rapidly. Another large electron current was injected again at $t = 1.7\,\mu$s. The device eventually failed at $t = 2.0\,\mu$s. On the other hand, the device safely turned off in the case of $L = 6\,\mu$H.

Figures 4(a)–4(e) show the hole current distributions for several time steps in the N-base. It was observed in the case of $L = 7\,\mu$H that rather broad current filaments appeared from the beginning of the sustaining period as shown in Fig. 4(a). Then, the broad current filaments turned into a single narrow current filament at a corner of the device as shown in Fig. 4(b), which corresponds to the time step of the first hump of the emitter electron current, shown in Fig. 3. It suggests that the first local latch-up occurs at the position of the narrow current filament. Next, the current filament branched into two filaments as shown in Fig. 4(c). One current filament stayed in the same position and the branched current filament moved toward another corner of the device. It reached to another corner of the device, as shown in Fig. 4(d), at $t = 1.7\,\mu$s, which was the same time of the second hump of the emitter electron current. It also suggests that the second local latch-up occurred inside the branched current filament. However, eventually, the device failed at the location where the first latch-up occurred, as shown in Fig. 4(e).

No significant current filaments were observed in the case of $L = 6\,\mu$H.

3.1.2. Device size dependencies. It was observed that there were two large differences between the UIS waveforms of the two simulated devices, $80\,\mu\text{m} \times 80\,\mu\text{m}$ and $160\,\mu\text{m} \times 160\,\mu\text{m}$. One difference was the failure energy. Figure 5 shows the UIS calculation results of $80\,\mu\text{m} \times 80\,\mu\text{m}$ and $160\,\mu\text{m} \times 160\,\mu\text{m}$ device size. The $80\,\mu\text{m} \times 80\,\mu\text{m}$ device survived even when $L = 30\,\mu$H and

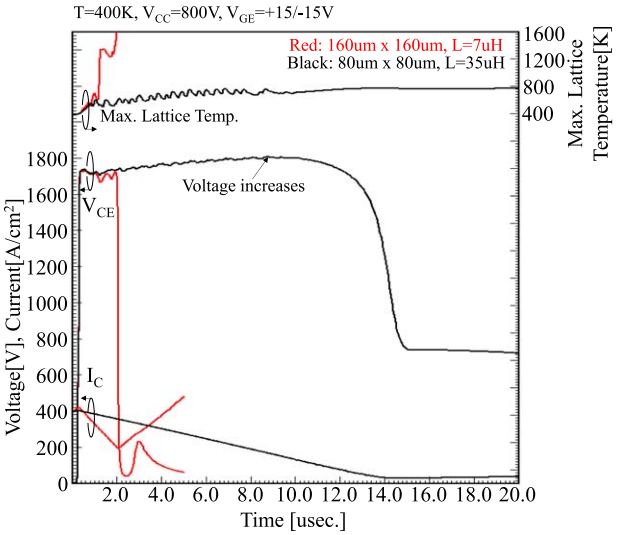

Fig. 5. (Color online) UIS failure waveforms for $80\,\mu\text{m} \times 80\,\mu\text{m}$ and $160\,\mu\text{m} \times 160\,\mu\text{m}$ device sizes. The $80\,\mu\text{m} \times 80\,\mu\text{m}$ device survives much longer period than $160\,\mu\text{m} \times 160\,\mu\text{m}$ device.

failed when $L = 35\,\mu$H. The failure energy was 4.5 J cm^{-2}. The result did not agree with the observed value in the manufacture's datasheets.[31] It was 4 times larger than the failure energy of $160\,\mu\text{m} \times 160\,\mu\text{m}$, as shown in Fig. 6.

The other difference was the waveform of the calculated breakdown voltage. As shown in Fig. 5, the $160\,\mu\text{m} \times 160\,\mu\text{m}$ device showed almost flat breakdown voltage throughout the sustaining period. This waveform agreed with previously reported experimental results.[20,21,32] On the other hand, the $80\,\mu\text{m} \times 80\,\mu\text{m}$ device showed increasing breakdown voltage.

3.2. Discussion

We found that there are two kinds of current filament—avalanche induced current filament and temperature induced current filament. In order to clarify the UIS destruction mechanism, these should be discussed in more detail in this section. First, the avalanche induced current filament appears and grows. Then, the temperature induced current filament

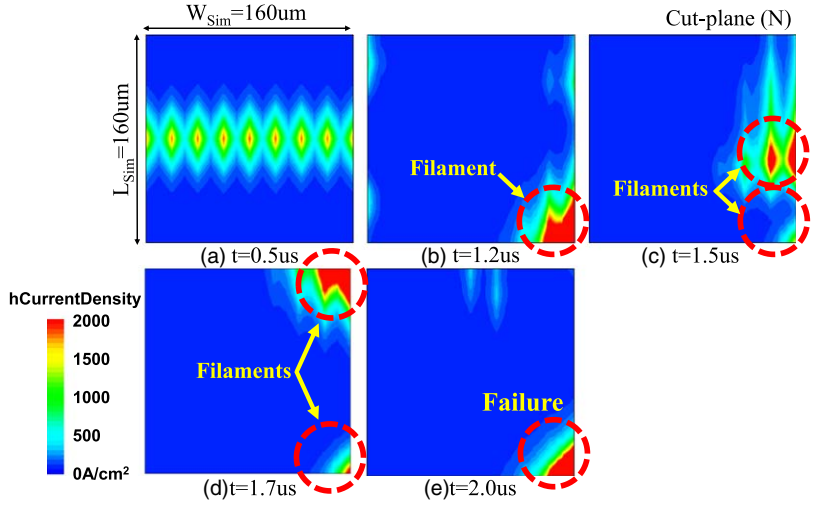

Fig. 4. (Color online) Hole current density distributions are shown for several time steps in the cut-plane (N). (a) Broad current filaments appear in the beginning of the sustaining period. (b) Broad current filaments turn into single narrow one. (c) The current filament branches two filaments. One filament moves toward another corner of the device. (d) One filament reaches another corner of the device. (e) The device fails at the position which first single narrow filament appeared.

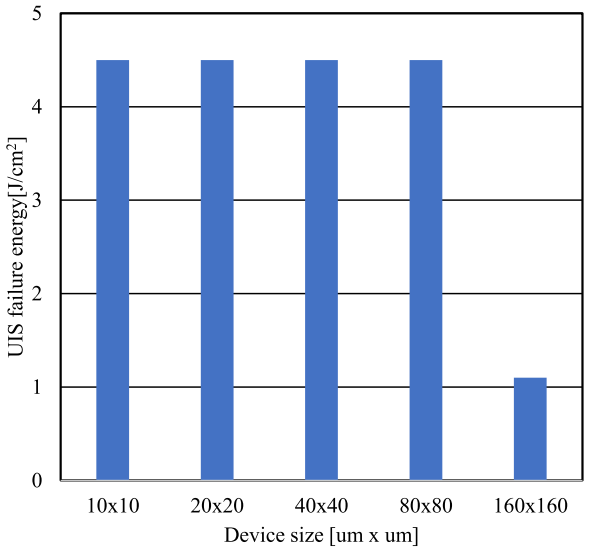

Fig. 6. (Color online) UIS failure energy versus size of simulated device. The failure energy of the 160 μm × 160 μm device is much smaller than smaller sized devices.

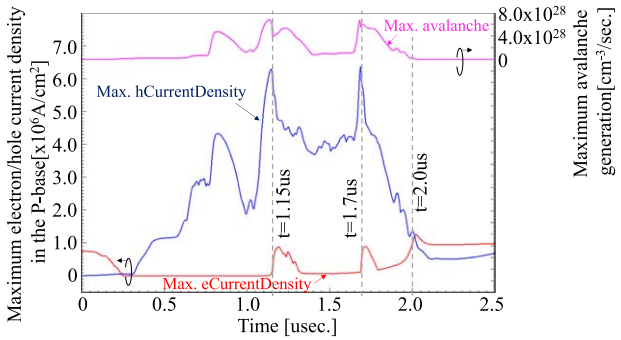

Fig. 7. (Color online) Waveforms of the maximum electron and hole current density in the P-base, and the maximum avalanche generation in the device are plotted as a function of time when $L = 7\,\mu$H. At $t = 1.1\,\mu$s, the avalanche generation is increased by the avalanche induced current filament and, resulting in significant increase in hole current density in the P-base. Then, at $t = 1.15\,\mu$s, the electron current starts to flow from the emitter electrode. This is so-called latch-up. Similar events occur at $t = 1.7\,\mu$s. The electron current continues to increase. Finally the device fails at $t = 2.0\,\mu$s.

appears inside the avalanche induced current filament and causes device failure.

3.2.1. Avalanche induced current filament. In general, impact ionization occurs inhomogeneously because the generated electron-hole pairs reduce the electric field, which is main driving force of the impact ionization. This phenomenon induces a point of localized large impact ionization, which creates avalanche induced current filament. A large power dissipation occurs inside the filament and increases the temperature at the location of the filament. The temperature increase reduces the amount of the impact ionization because the impact ionization rate is inversely dependent on the temperature. Thus, the avalanche induced current filament moves around to a lower temperature point.

3.2.2. Temperature induced current filament. When latch-up occurs inside the avalanche induced current filament, the electron current starts to be injected from the N-emitter to the P-base even when the MOS gate is off state. The injected electron current enhances the avalanche generation. A huge temperature increase occurs and the P-base turns into intrinsic semiconductor. Even when the impact ionization reduces because of the increased temperature, the electron current from the emitter continues to flow into the P-base and still rise the temperature more. This is what we call temperature induced current filament. The power dissipation inside the filament increases the temperature of the P-base and further increases the electron current flow. This creates a positive feedback. In result, the temperature induced current filament continues to stay in the same location. Eventually it causes device failure.

3.2.3. Device destruction mechanism. The UIS failure mechanism can be explained by the dynamics of the avalanche induced current filament and the temperature induced current filament. Figure 7 shows the waveforms of the electron current from the emitter electrode, the maximum hole current in the P-base and the maximum avalanche generation in the device when $L = 7\,\mu$H. The avalanche generation distributions in the N-base is shown for the several time steps in Figs. 8(a)–8(d). The temperature distributions in the P-base is also shown in Figs. 9(a)–9(d).

In the beginning of the UIS, broad avalanche induced current filaments appear as shown in Fig. 8(a). No significant temperature increases are observed as shown in Fig. 9(a).

The avalanche induced current filaments turn into single one at the corner of the device as shown in Fig. 8(b) at $t = 1.15\,\mu$s. The emitter electron current starts to be injected by the latch-up, which is caused by huge hole current density towards the emitter electrode. The injected electron accelerates avalanche generation. These phenomena are observed in Fig. 8(b). The P-base temperature increases rapidly by the power dissipation caused by the large avalanche generation, as shown in Fig. 3. However, the avalanche generation reduces because the P-base temperature reaches 900 K. This reduces the electron current temporarily.

Next, the avalanche induced current filament is divided into the two current filaments. These are the avalanche induced current filament and the temperature induced current filament, which is activated inside the avalanche induced filament. The avalanche induced current filament moves to the other lower temperature region, as indicated in Fig. 8(c). The temperature induced current filament stays in the same position and still rises the P-base temperature, as is shown Fig. 9(c). The electron current continues to flow because the P-base already becomes intrinsic because of the high temperature. The electron current slightly increases again due to the P-base temperature increase.

Then the avalanche induced current filament reaches to another corner and becomes single narrow one, as shown in Fig. 8(d). It causes another latch-up at $t = 1.7\,\mu$s, which is shown by the second hump of the emitter electron current in Fig. 3. This accelerates avalanche generation again. However, the avalanche generation reduces soon. These are same phenomena as we have discussed for the first latch-up. On the other hand, the temperature induced current filament continues to stay in the same position, as shown in Fig. 9(d).

The temperature induced filament eventually causes UIS failure at $t = 2.0\,\mu$s as shown in Fig. 9(e). The electron current density exceeds 1.2×10^6A cm^{-2} when the device

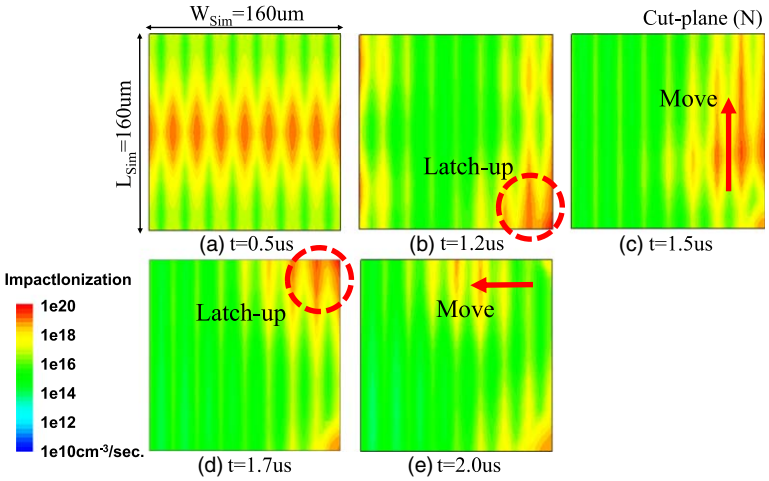

Fig. 8. (Color online) The avalanche generation distributions are shown for the several time steps in the N-base. (a) Several broad avalanche induced current filaments appear in the beginning of the sustaining period. (b) The avalanche current filaments turn into single filament. The emitter electron current starts to be injected by latch-up. (c) The current filament is divided into the two current filaments, the avalanche induced current filament and the temperature induced current filament. The avalanche induced current filament moves toward another corner of the device. (d) The avalanche induced current filament reaches another corner of the device. (e) The avalanche induced current filament moves again even when the device fails.

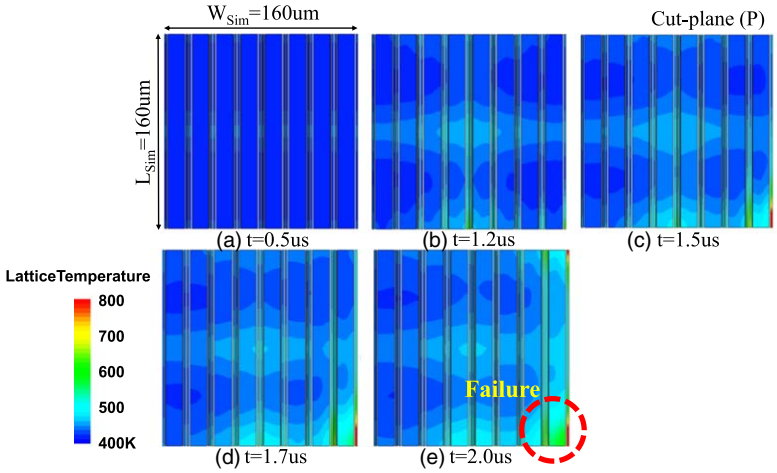

Fig. 9. (Color online) The lattice temperature distributions are shown for the several time steps in the P-base. (a) No significant temperature increases appear in the beginning of the sustaining period. (b), (c) The avalanche current filaments turn into single filament. The emitter electron current starts to be injected by latch-up. The temperature rises at the position of the single filament. It causes temperature induced current filament. (d) The temperature induced current filament stays in the same position. (e) The device fails at the position of temperature induced current filament occurs.

fails. The device no more sustains the breakdown voltage because the lattice temperature exceeds 1600K.

3.2.4. Relationship of device size and current filament evolution. The calculated UIS failure energy depends on the simulation device size. This result is relevant to the amount of current density in the avalanche induced current filament. The transient of the maximum avalanche generation, the maximum lattice temperature and the electron current from the emitter electrode of $80\,\mu\text{m} \times 80\,\mu\text{m}$ and $160\,\mu\text{m} \times 160\,\mu\text{m}$ device size are compared in Fig. 10. During the breakdown period, the avalanche generation of the $80\,\mu\text{m} \times 80\,\mu\text{m}$ device is quite lower than that of the $160\,\mu\text{m} \times 160\,\mu\text{m}$ device. The avalanche induced current filaments keep moving and do not turn into large current density filament as shown in Fig. 11. It indicates that, in the $80\,\mu\text{m} \times 80\,\mu\text{m}$ device, the amount of the current density in the avalanche induced current filament is not large enough to cause latch-up. Thus, the lattice temperature increases not locally but globally. It results in an increasing breakdown voltage waveform as a function of time. The electron current

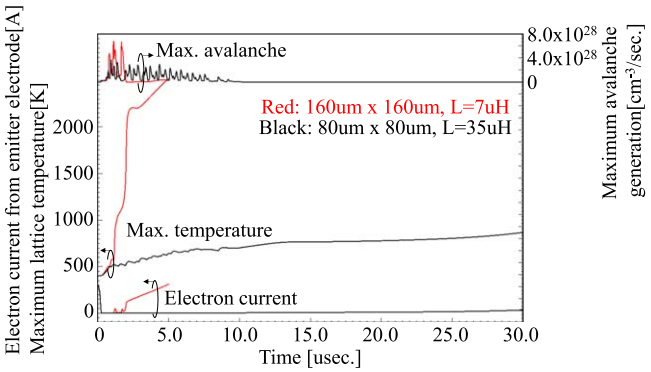

Fig. 10. (Color online) Comparison of the maximum avalanche generation, the maximum lattice temperature and the electron current from the emitter electrode between $80\,\mu\text{m} \times 80\,\mu\text{m}$ and $160\,\mu\text{m} \times 160\,\mu\text{m}$ device size.

starts to inject when the temperature exceeds a certain value. Finally, the device fails by global temperature increases. This is different failure mechanism from $160\,\mu\text{m} \times 160\,\mu\text{m}$ device.

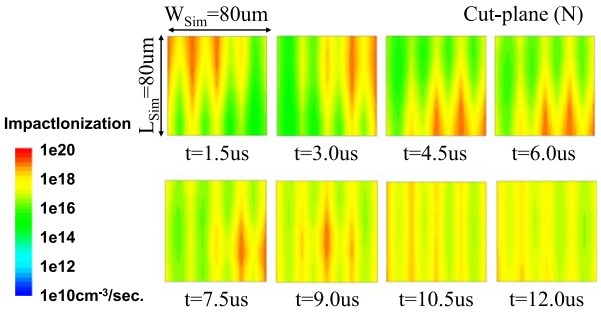

Fig. 11. (Color online) The avalanche generation distributions are shown for the several time steps in case of 80 μm × 80 μm simulation size. The avalanche induced current filaments keep moving and do not turn into large current density filament.

4. Conclusions

The detailed failure mechanism of UIS has been analyzed by large scale 3D TCAD simulations.

There are two kinds of current filament, avalanche induced current filament and temperature induced current filament. The avalanche induced current filament moves toward lower temperature region, although the temperature induced current filament stays in the same position. During the UIS operation, the avalanche induced current filaments firstly develop and move around. They finally turn into one large current density filament and cause local latch-up by high hole current density in the P-base. The latch-up causes huge local temperature increase in the P-base inside the filament. This activates temperature induced current filament. The device fails by local temperature increase.

The UIS failure energy depends on the simulated device size. In the small scale 3D simulations, the amount of the current density in the avalanche induced current filament is not enough to cause local latch-up. The device fails by global temperature increase. The calculated UIS failure energy becomes much larger than that of actual device. Large scale 3D simulation is mandatory to reproduce correct phenomena of UIS failure.

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