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Power Device Evolution Challenging to Silicon Material Limit

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1. Introduction

Recent epoch-making event is the advent of IGBTs and super-junction MOSFETs. IGBTs have displaced current control devices, GTOs and BTr's. Now, three types of MOS gate devices, IGBTs, power MOSFETs and lateral DMOS (LDMOS), are predominantly used depending on the applications (see Fig.1).

It is often cited that power devices are facing the silicon limit. The present paper makes clear where the limit of each power device exists and how to achieve the silicon limit characteristics. It is also clarified that system improvement cannot be achieved without the environmental circuit improvement associated with the devices.

2. IGBTs (Insulated Gate Bipolar Transistor)

Applications of IGBTs include home appliance motors, electric trains, hybrid vehicles, etc. In the early development stage, IGBTs were easily destroyed by the latch-up of the parasitic thyristor. The author successfully developed the world first non-latch-up IGBTs in 1984[1]. The developed IGBTs exhibited a lower on-resistance as well as a capability of withstanding a large power, exceeding the bipolar transistor limit: $2x10^5$W/cm^2. This triggered the evolution of IGBTs, and opened up the new era of IGBTs. Now, IGBTs have been greatly improved by trench gates and the thin wafer technology.

It is important to clarify the silicon limit of IGBTs, The author predicted the I-V curve of the silicon limit IGBT in 2006[2], which is shown by Eq.(1). In 2008, the author also proposed the practical IGBT limit[3], shown by Eq.(2), which is based on a more realistic assumption.

$$V_F = \frac{2kT}{q} \ln[\frac{1}{n_i}\{(\sqrt{\frac{QJ}{qD_{pe}}} + b)\exp(\frac{JW_i}{2qa}) - b\}] \quad + R_{ch}J. \quad \text{..... Eq.(1)}$$

$$V_F = \frac{kT}{q} \ln \frac{\mu_n Q_{pe} J}{qD_{pe} n_i^2 (\mu_n + \mu_p)} + W_i \sqrt{\frac{D_{pe} J}{q\mu_n(\mu_n + \mu_p)Q_{pe}}} + \frac{\mu_n R_{ch}}{\mu_n + \mu_p} J \quad \text{..... Eq.(2)}$$

W_i, Q R_{ch} and D_{pe} denote the n-base width, the p-emitter dose, the channel resistance and the electron diffusion coefficient in the p-emitter, respectively. In Fig.2 and 3, the ideal and practical silicon limit of IGBTs are shown and compared with other devices. "Practical limit" is very close to the "ideal limit" and can be realized with a larger possibility.

Higher operating current density is demanded for HEV application. Fig.4 shows typical dependence of I-V curve on device cell pitch. Chip shrink or an operating current density exceeding 500A/cm^2 will be realized in IGBTs, if the issue of short-circuit-withstanding capability is properly handled.

3. Power MOSFETs

Recent evolution in high speed power MOSFETs has been initiated by the need of voltage regulator module (VRM) for CPUs. In the conventional MOS gate drive condition, the switching time is dominated by the mirror period, which depends on Q_{gd}/I_G *(gate-drain charge/gate current.)* Most of the switching power loss occurs in this mirror period. The product $R_{on}Q_{gd}$ has conventionally been adopted as FOM. Today, the FOM value of power MOSFETs has been decreased to 1/4 of the value in 1999.

If a low impedance gate drive is used in order to supply a large gate current and make the value of Q_{gd}/I_G small, the switching power loss is greatly reduced. The remaining major switching losses are the joule loss ($R_{on}I_D^2$), the center junction capacitance loss ($Q_{ds}V_D$) and the gate drive loss (Q_GV_Gf). (Q_{ds} denotes the stored charge in the device).

$$P_{loss} = R_{on}I_D^2 + \frac{1}{3}Q_{ds}V_Df + Q_GV_Gf \geq 2\sqrt{\mathbf{R_{on}Q_{ds}}\frac{1}{3}I_D^2V_Df} + Q_GV_Gf \quad \text{...Eq.(3)}$$

The total power loss, P_{loss}, takes a minimum when the first term and the second term are equal. According to Eq.(3), new FOM, $R_{on}Q_{ds}$, is introduced for the ideal switching case[4], and can be used to compare the switching speed capability of various power devices, as shown in Fig.5.

High frequency operation in buck converters can be realized by Multi-Chip-Module[5], which can implement a low impedance gate drive by integrating a gate driver and two MOSFETs in one package. MCM can also optimize the total inductance value in the power stage so that the total power loss can be minimized[6], as seen in Fig.6. Fig.7 shows the efficiency improvement by the low impedance gate drive. Efficiency improvement in MCM necessitates the environmental circuit improvements in addition to the MOSFET improvement.

4. Power ICs and DCDC converters

Low voltage BiCD (BiCMOS DMOS) technology is applied to various applications below 100V, including motor control, power supplies and automotive ICs. Device scaling in BiCD power ICs was made possible just like logic CMOS by using pure "lateral DMOS"(LDMOS) in place of so-called "up-drain vertical DMOS."

DCDC converters are essential because electric appliances, PCs and mobile equipments rely on batteries and power supplies. We have developed 12V 10A single chip DCDC converters[7] using 0.6μm BiCD platform. The switching speed and the on-resistance of LDMOS are the key parameters to realize a high efficiency. We adopted the bump technology to reduce the metal interconnection resistance. The chip is mounted on PCB board by flip chip technology. The thick Cu metal layers in the PCB board can be used as interconnection wires and the interconnection resistance can be significantly reduced.

We also adopted distributed gate drivers[6] for uniform and high speed switching. The gate driver consists of a number of local gate drivers. Each local gate driver is placed close to the each segmented lateral DMOS. Only the gate triggering signals are transmitted to the each local driver, and do not induce any significant voltage drop in the gate

interconnection wires, thus avoiding non-uniform switching. The on-resistance of the large area LDMOS is 9.7mΩ. The developed 12V 10A chip (see Fig.8) achieved 88.9 % efficiency at 780kHz.

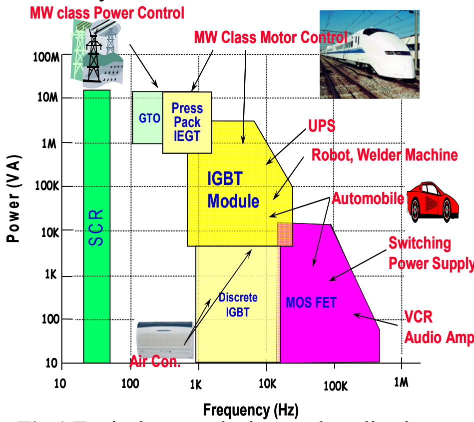

Fig.1 Typical power devices and applications

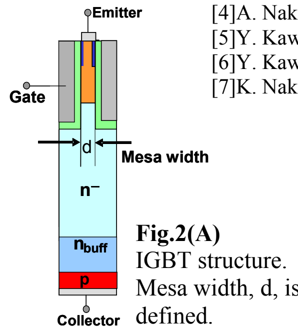

Fig.2(A) IGBT structure. Mesa width, d, is defined.

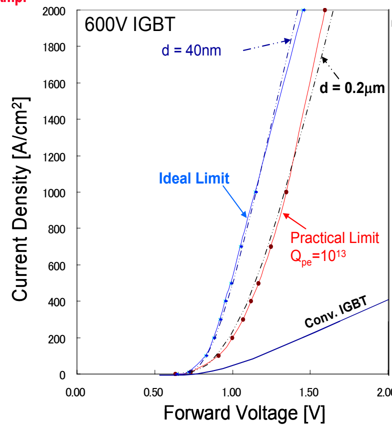

Fig.2(B) "Ideal IGBT limit," given by Eq.(1), agrees with TCAD simulation result of 600V IGBT with 40nm mesa. "Practical limit" V-I curve (Eq.(2)) agrees with simulation result of IGBT with 0.2μm mesa. Conventional 600V IGBT is shown for comparison.

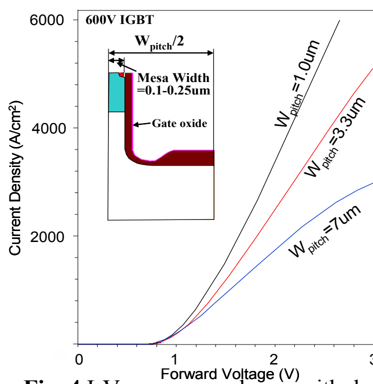

Fig. 4 I-V curves are shown with device cell pitch (W_{pitch}) as a parameter. 0.1μm or 0.25μm Mesa width is chosen so that flat carrier profile is maintained. Forward voltage is still low in 500A/cm^2 range for IGBT with cell pitch of 7μm although saturation current is greatly reduced.

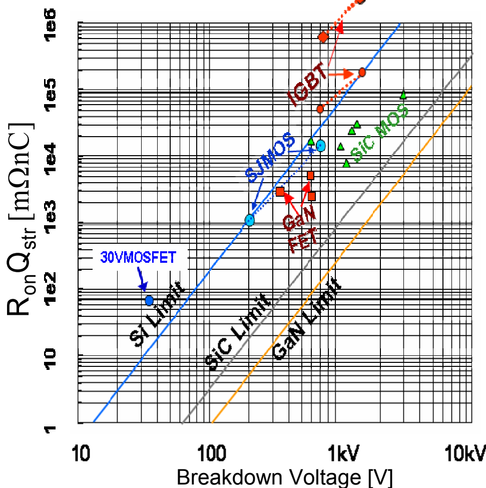

Fig.5 The values of the FOM ($R_{on}Q_{str}$) are calculated for various devices. Here, Q_{str} is the same as Q_{ds}. Lower FOM value means superior device characteristics, because the FOM is equivalent to the product of forward voltage and switching time: $V_F T_S$, where $V_F = R_{on}J$ and $T_S = Q_{str}/J$.

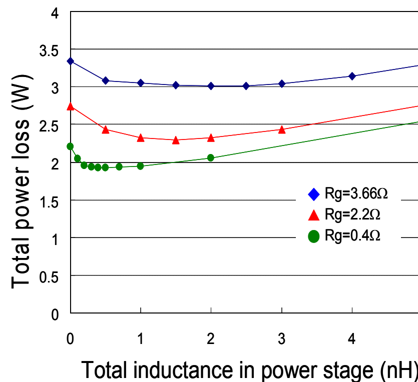

Fig.6 There is an optimum value of total inductance in power stage circuit that minimizes the total power loss of power MOSFETs and their gate driver. Parameter, R_g, means the sum of gate driver circuit impedance and the gate resistance of MOSFET.

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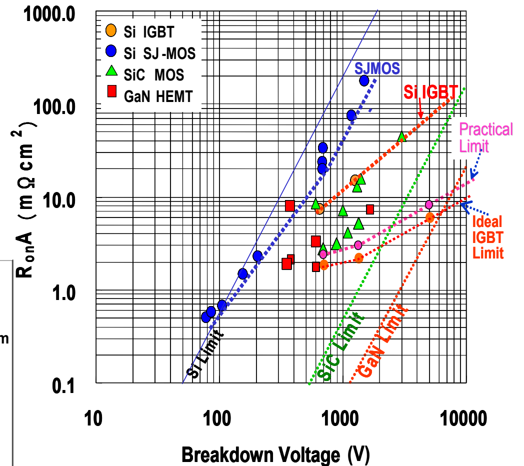

Fig.3 Theoretically predicted "practical IGBT limit" is shown together with "ideal IGBT limit" predicted in Ref.[2]. Practical limit is very close to ideal limit.

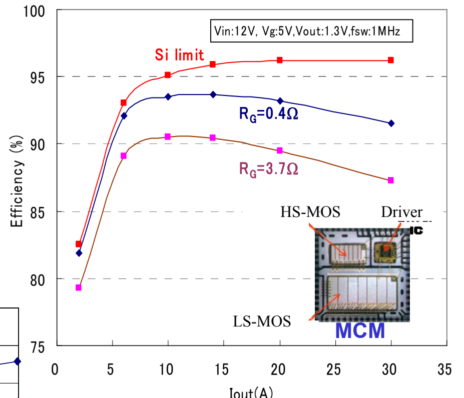

Fig.7 The low impedance gate drive circuit (R_G=0.4Ω) achieves more than 90% efficiency at 30A, 1MHz operation in Multi-Chip-Module (MCM). The figure compares buck converter efficiency between low impedance gate drive and conventional 3.7Ω gate drive. Prediction of silicon limit efficiency is also included[6].

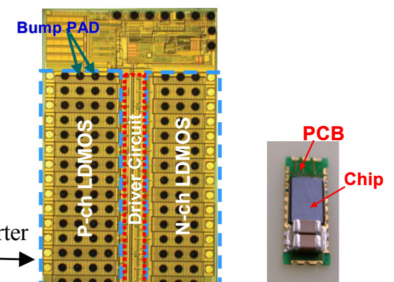

Fig.8 12V 10A DCDC converter chip photo.