20V and 8 V Lateral Trench Gate Power MOSFETs with Record-Low On-resistance

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Abstract

We propose a novel lateral trench gate power MOSFET which utilizes narrow and shallow multiple trenches as channel regions. The developed device achieved 13mΩ·mm^2 and 5 mΩ·mm^2 of on-resistance with the breakdown voltage of 25V, 11V respectively, which is the record low on-resistance among the previous works

Introduction

Many studies of low on-resistance 8 - 20 V range MOSFETs have been conducted because these devices have a variety of applications in computer peripherals. In this paper, we propose, for the first time, a novel lateral trench gate power MOSFET which utilizes narrow and shallow multiple trenches as channel regions as shown in Fig.1. Conventional trench gate structures have been used for vertical trench MOSFETs, where channel current flows vertically on the trench side walls. The unique feature of the lateral trench gate MOSFETs is that the electron current spreads into the channel regions induced both on the trench terrace and on the trench side walls, and that the channel current flows laterally on the trench side walls from the source to the drain. The n-diffusion layer reaches the bottom of the trenches so that the electron channel current, flowing widely spread in the trench side walls, is effectively collected by the drain n layer, reducing channel resistance.

The proposed device was fabricated using the standard 0.6μm CMOS process and an additional trench gate formation process. The developed device achieved 13 mΩ·mm^2 and 5 mΩ·mm^2 of on-resistance with the breakdown voltage of 25V, 11V respectively, which is the record low on-resistance compared with the previous works, and is even lower than that of the vertical trench MOSFETs. For a reference, the on-resistances of the simultaneously fabricated planar lateral DMOS were 25 mΩ·mm^2 and 9 mΩ·mm^2 with the breakdown voltage of 24 V and 11 V respectively. The previously reported lowest specific on-resistance of 25 V lateral DMOS was 18 mΩ·mm^2 [1].

Device Description

A. Device Structure

Figure 1 (a), (b) shows a top view of the proposed 20 V and 8 V trench gate LDMOS respectively, and fig. 2 (a), (b) (c) shows cross-sectional views of line A-A', B-B' and C-C' in fig. 1 respectively. A number of fine trenches were formed, running from the source to the drain n-layer. For 8 V device, the drain n+ layer is self-aligned to the poly gate, and 20 V device has a drift region in order to achieve high breakdown voltage.

The width, space and depth of the trenches are 0.4 μm, 0.4μm and 1.0μm, respectively. Since the terrace and the side walls of the trenches works as channels, the effective gate width is 3.5 times as wide as that of the conventional planer LDMOS. It is important to reduce the spreading resistance from the source to the channel. The trench gate must overlap sufficiently with the source n+ diffusion.

B. Calculation Results

Calculations were carried out using 3D device simulator dessis-3D in order to optimized device parameters. The overlapped length of the trench and the source n+ layer (L in fig. 2 (d)) were optimized in order to reduce the spreading resistance and to realize uniform electron current flow in the trench side wall.

Figure 3 shows the calculated dependence of breakdown voltage on the dose of drift region for 20 V device. It was predicted that the proposed trench gate LDMOS achieves 10 mΩ·mm^2 specific on-resistance for the breakdown voltage of more than 20 V. This is about a half of that of conventional planer LDMOS.

Figure 4 shows the current density distribution which correspond to the cross-section of fig. 2 (a) when the drain is 0.1 V and the gate voltage is 5 V. This figure shows that the electron current flows widely spread in the trench side walls and effectively collected by the drain n layer.

C. Fabrication process

Figure 5 shows the process flow chart to fabricate the proposed trench gate LDMOS. Because the trenches are formed just before gate oxide formation and the gate oxide and gate polysilicon electrode are common to standard CMOS devices, the proposed device can be fabricated by standard CMOS process and additional trench formation process.

Figure 6 shows the SEM photograph of fabricated device which correspond to the cross-section of fig. 2 (b). This photograph shows that the fine trenches are formed and filled up with gate polysilicon.

Experimental Results and Discussion

Figure 7 and 8 show the measured blocking characteristics and the V-I characteristics of the fabricated trench gate LDMOS. The measured and calculated values of the device characteristics are listed in table 1. The developed device achieved 13 $m\Omega \cdot mm^2$ and 5 $m\Omega \cdot mm^2$ of on-resistance with the breakdown voltage of 25V, 11V respectively. Figure 9 compares the measured and calculated specific on-resistance of fabricated device with previously publish data. The developed device achieved the record low on-resistance compared with the previous works.

However, the measured value of the on-resistance is not so low as the calculated value. This is assumed that the channel mobility of trench side wall is lower than that of planer devices because of the surface roughness. It was reported [2, 3] that the surface roughness of trench side wall greatly influence the channel mobility. The on-resistance will be further reduced by optimization of the smoothing process of trench side walls.

The developed LDMOS also achieve extremely large current turn-off capability of 8.6×10^3 A/cm^2 for 20 V device and 1.1×10^4 A/cm^2 for 8 V device, respectively

Conclusion

We have presented a 20 V and 8 V low on-resistance novel structure trench gate LDMOS. The proposed device can be fabricated using standard CMOS process and additional trench formation process. The proposed device achieves 13 $m\Omega \cdot mm^2$ and 5 $m\Omega \cdot mm^2$ of on-resistance with the breakdown voltage of 25V, 11V respectively, which is the record low on-resistance compared with the previous works. The on-resistance will be further reduced by optimization of the smoothing process of trench side walls.

Acknowledgments

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References

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TABLE I
Measured and calculated values of the device characteristics of the proposed MOSFET

	Measured Value	Calculated Value
20 V device		
Breakdown Voltage (V)	25	26
On-resistance ($m\Omega \cdot mm^2$)	13.0	10.3
turn-off capability (A/cm^2)	8.6×10^3	-
8 V device		
Breakdown Voltage (V)	11	11
On-resistance ($m\Omega \cdot mm^2$)	5.0	3.3
turn-off capability (A/cm^2)	1.1×10^4	-

Fig. 1 Top view of the proposed trench gate (a) 20 V, (b) 8 V LDMOS. Trench gate is arrayed at right angles with device pitch. The width and space of trench gate is 0.4 μm

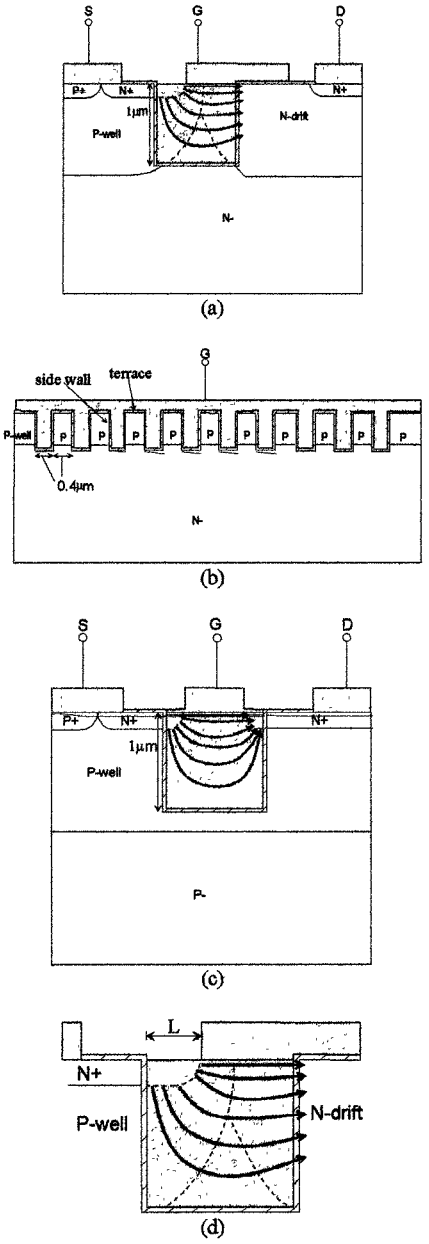

Fig. 2 (a) Cross sectional view of proposed trench gate LDMOS in line A-A', (b) line B-B' and (c) line C-C' in fig. 1.and (d) magnified view of the channel region in fig. 2 (a). The depth of trench gate is 1.0 μm. The electron channel current flows laterally on the trench side walls from the source to the drain.

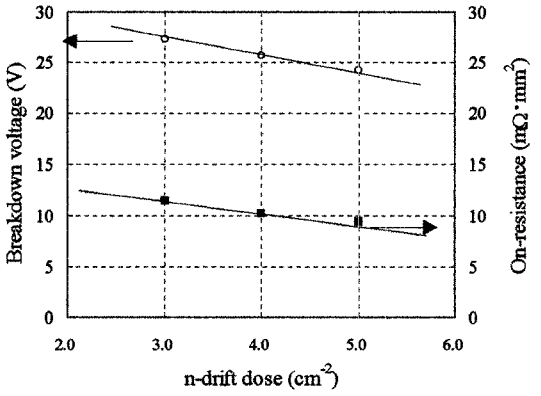

Fig. 3 Calculated dependence of breakdown voltage and on-resistance on the dose of drift region. It was predicted that the proposed trench gate LDMOS achieves 10 mΩ·mm² specific on-resistance for the breakdown voltage of more than 20 V.

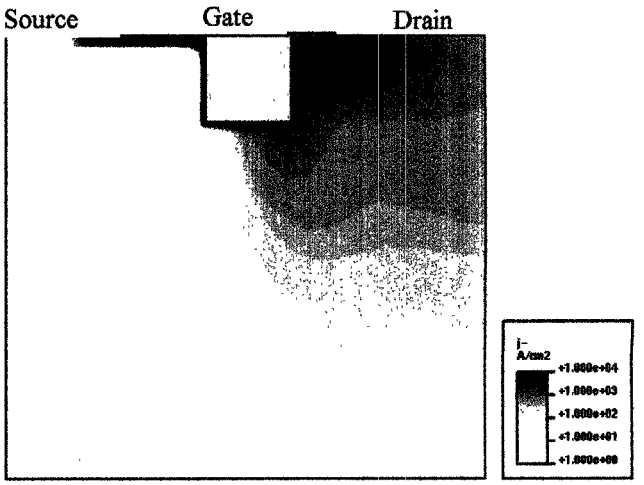

Fig. 4 Current density distribution which correspond to the cross-section of fig. 2 (a) when the drain is 0.1V and the gate voltage is 5 V. This figure shows that the electron current flows widely spread in the trench side walls and effectively collected by the drain n layer.

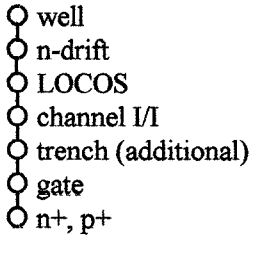

Fig. 5 Process flow of proposed trench gate LDMOS

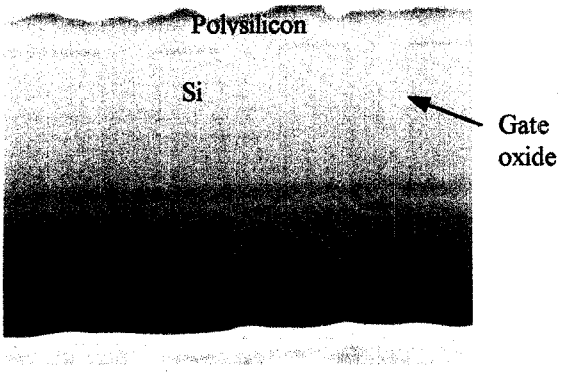

Fig. 6 SEM photograph of fabricated trench gate LDMOS. The fine trenches are formed and filled up with gate polysilicon electrode

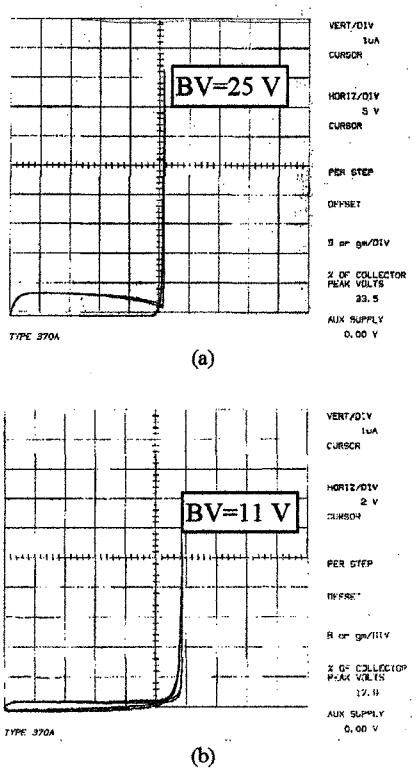

Fig. 7 Blocking characteristics of fabricated trench gate LDMOS. (a) 20 V device (BV=25V), (b) 8 V device (BV=11V).

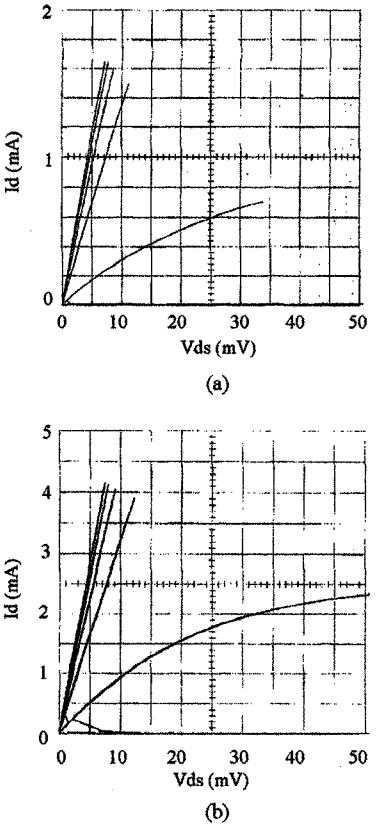

Fig. 8 V-I characteristics of fabricated trench gate LDMOS . (a) 20 V device, (b) 8 V device.

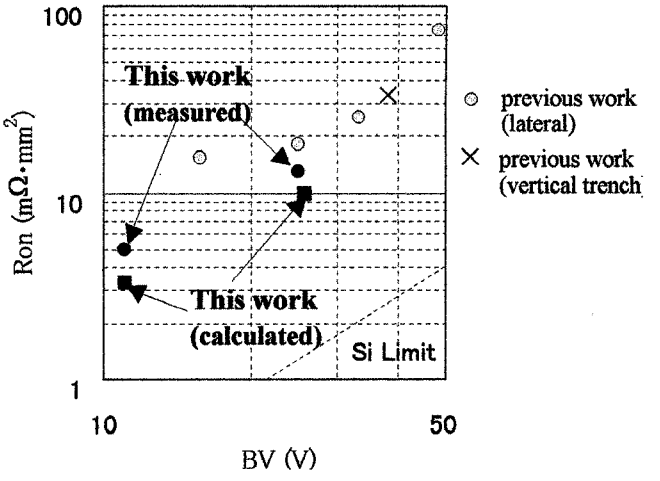

Fig. 9 Comparison of on-resistance and breakdown voltage for this work (●) and previously publish data. The developed device shows the record low on-resistance among the previous works(○), and is even lower than that of the vertical trench MOSFET(×). Comparing to calculated data (■), the on-resistance will be further reduced by optimization of the smoothing process of trench side walls.