# High Voltage BiCDMOS Technology on Bonded 2μm SOI Integrating Vertical npn pnp, 60V-LDMOS and MPU, Capable of 200 °C Operation

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## Abstract

Trench isolated 60 V BiCDMOS processes on bonded 2 μm thick SOI, capable of integrating 60 V low on-resistance lateral DMOS, vertical npn and pnp, and an MPU have been developed and demonstrated 200 °C high temperature operation, for the first time. The developed processes are completely compatible with the conventional 0.8 μm rule CMOS processes and, thus, capable of integrating any existing library of MPUs, logic and analog circuits together with 60V-DMOS H bridges.

## Introduction

The SOI Technology has been of great interest because high-voltage devices can be integrated on the same chip together with CMOS circuitry by simply using shallow trench isolation. It has the further advantages of high-speed and high-temperature operation. The authors have already reported that high voltage lateral IGBTs fabricated on 1.5 μm thick SOI operated at 200 °C at a frequency of 20 kHz [1,2]. 200 °C operation covers most of the high temperature applications, including automotive engine related ones. SOI solution is now practical because the price of bonded SOI wafers with thicker silicon layers has become the same as that of epi-wafers with $n^+$ buried layers.

We have developed trench isolated 60 V BiCDMOS processes on bonded 2 μm thick SOI, capable of integrating 60 V low on-resistance lateral DMOS, vertical npn, and even an MPU. The developed processes are completely compatible with the conventional 0.8 μm rule CMOS processes. This paper demonstrates for the first time that 60 V lateral DMOS's and MPUs fabricated by the developed 0.8 μm rule BiCDMOS processes on the same 2 μm thick SOI wafer successfully operated at 200 °C. The authors also show that thin SOI is suitable for high temperature operation of bipolar analog circuits.

## BiCDMOS Technology on SOI

The developed processes are completely compatible with the conventional 0.8 μm rule CMOS processes. In order to verify the compatibility of the process, a 4 bit CMOS version MPU, consisting of 30,000 FETs for Core, 6,000 FETs for cash and 120,000 ROM FETs, has been fabricated on 2 μm thick SOI with 0.5 μm buried oxide, using the same mask for the bulk CMOS MPU. Figure 1 shows the cross-sectional view and layout of the 4 bit CMOS MPU on 2 μm SOI.

Trench isolated H bridges of 60V lateral DMOSFETs, vertical npn and CMOS were fabricated together with MPUs on the same 2μm thick SOI substrates by the same conventional 0.8μm rule CMOS processes with 2 additional masks in addition to additional trench processes. Figure 2 shows the cross section of the developed 60V BiCDMOS technology. The CMOS p- and n-well layers were diffused into the buried oxide layer. The n-drift layer in the DMOSFET was formed using the same thermal process for the p- and n-well layers. The vertical pnp transistors are optional. The n-base of the pnp was formed by using the capacitor n-diffusion in common.

## Results and Discussion

### *A. 4bit CMOS MPU*

The fabricated SOI 4 bit MPU chips operated at a 20% faster clock speed of 50 MHz at 25 °C as compared with 42 MHz of the bulk version MPU and even operated at over 200 °C. It was found that clock speed can be improved and that a large latch up immunity at high temperature was realized even if any MOSFET is not isolated by trenches and if the SOI layer is not so thin as SIMOX. The maximum operating temperature was expected to be more than 300 °C but was not able to be measured because of instrument limitation. It was found that the yield of the MPU fabricated on SOI is the same as that on bulk wafers, verifying that the crystal quality of the currently available SOI wafers is sufficiently good. It was also found that even bulk MPUs can be operated at 300 °C if MPUs consist of pure CMOS, although the power consumption of the bulk MPU is larger than that of the SOI one.



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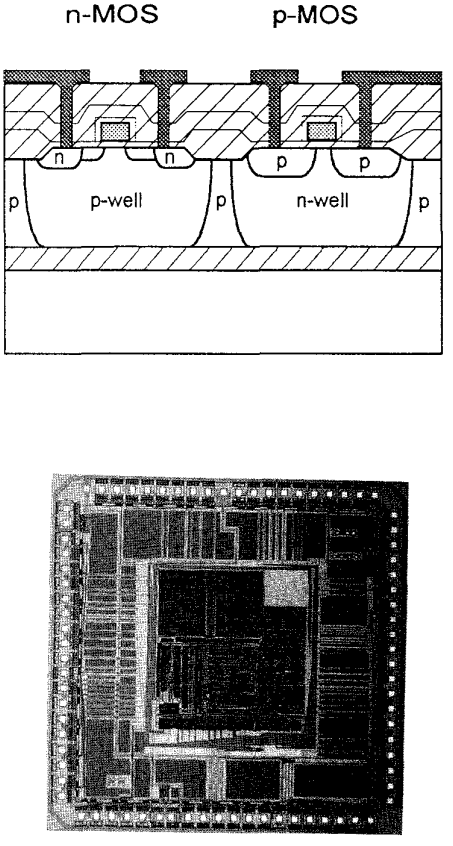


Fig. 1: Cross-sectional view and layout of the 4 bit CMOS MPU on 2μm SOI.

### B. 60V Lateral DMOS

The on-resistance of conventional high voltage DMOSFETs on SOI is influenced by the substrate bias [3]. However, the current-voltage curves of the developed DMOS are free from substrate bias influence as seen in Fig. 3. This is because the hole accumulation layer is induced on the bottom oxide as illustrated in Fig. 2 and shields the influence of the source to substrate bias. Thus, the 60V-DMOS can be operated as a high side switch (source follower) without on-resistance increase.

The $R_{on}$ · Area product of the fabricated LDMOS was 140 mΩ-mm$^2$, although the $R_{on}$ · Area product of an optimized LDMOS by the device simulator TONADDE is as low as 85 mΩ-mm$^2$. Figure 4 shows the calculated on-resistance for the optimized device and the breakdown voltage dependence on the impurity dose of the resurf layer in the LDMOS. Most of the on-resistance of the actual devices comes from the aluminum layer because the currently available 1μm thick 2nd aluminum layer is too thin for power devices.

### C. Vertical pnp and npn Transistors

Although SOI wafers have no $n^+/p^+$ buried layers, vertical npn and pnp transistors fabricated on the n-well and p-well layers exhibited sufficiently good characteristics, as seen in Fig. 5. The p- and n-base diffusion areas are 48 μm$^2$ and 114 μm$^2$, respectively. The current gains $h_{FE}$ obtained for the vertical npn and pnp transistors were 80 and 30, respectively.

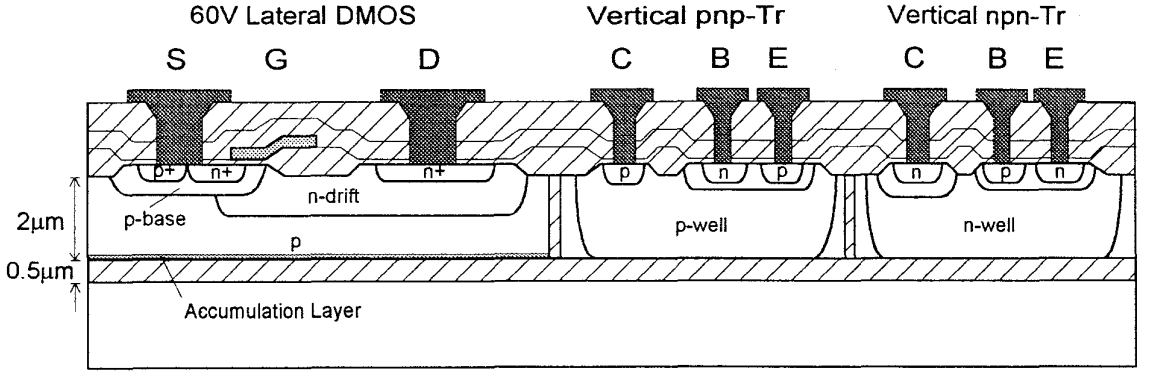


Fig. 2: Cross-sectional view of the developed 60V BiCDMOS. An accumulation layer appears to shield the influence of substrate bias if DMOS operates as a high side switch.

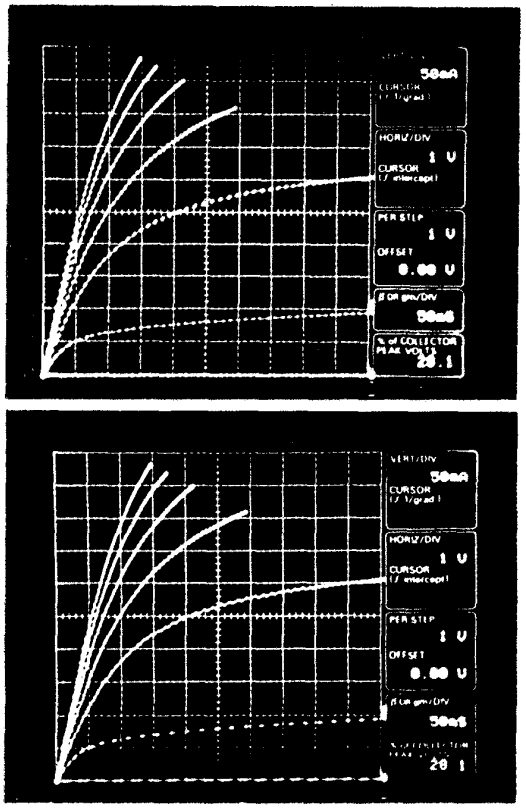


Fig. 3: Current-voltage curves of the 60V-DMOS for (a) 0V and (b) -50V substrate bias voltages. The substrate bias influence was completely suppressed.

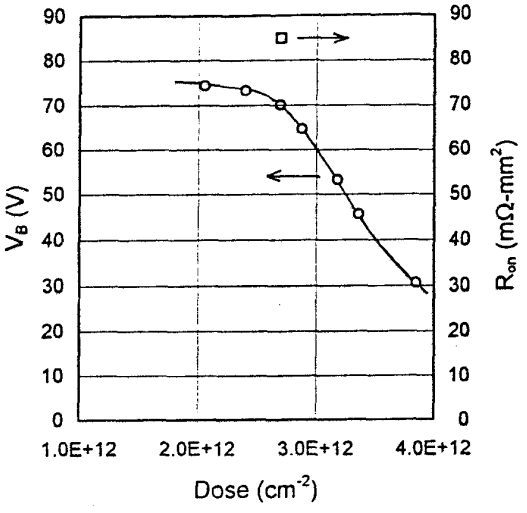


Fig. 4: Calculated breakdown voltage and on-resistance as a function of the impurity dose of the resurf layer in the LDMOS.

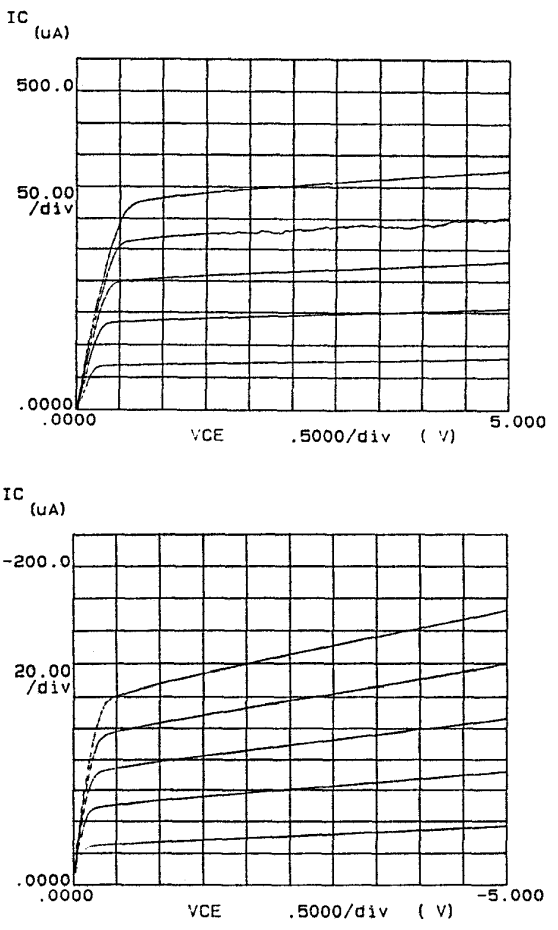


Fig. 5: Current-voltage curves of the vertical (a) npn and (b) pnp transistors. The p- and n-base diffusion areas are 48 $\mu m^2$ and 114 $\mu m^2$, respectively.

### *D. Analog Circuits*

Figure 7 shows the output voltages of the band gap reference circuit as a function of temperature with the silicon layer thickness as a parameter. It was found that maximum operating temperature of CMOS/npn analog circuits (not trench isolated) simply increases as the silicon layer thickness decreases. and 200 °C operation is possible for 2 μm SOI.

It should be noted that the CMOS and bipolar transistors described in this section were fabricated by 6 μm rule BiCMOS process and were not isolated by trenches but isolated by pn junction (see Fig. 8). If each bipolar transistor is isolated by trenches, much higher temperature operation is expected. These results assure 200 °C operation of whole IC chips based on the developed BiCDMOS technology on 2 μm SOI. if each bipolar transistor is trench-isolated.

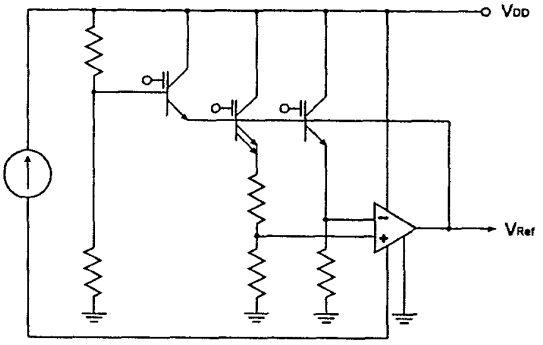


Fig. 6: Block diagram of the band gap reference circuit.

## Conclusions

We have developed trench isolated 60V BiCDMOS processes on bonded 2 μm thick SOI, capable of integrating 60V low on-resistance lateral DMOS, vertical npn and pnp, and an MPU and demonstrated 200 °C high temperature operation, for the first time.

The SOI 4 bit MPU chips operated at a 20% faster clock speed of 50 MHz at 25 °C as compared with 42 MHz of the bulk version MPU, and even operated at over 200 °C. The 60V-DMOS can be operated as a high side switch without on-resistance increase because of the induced bottom accumulation p-layer. Sufficiently good current-voltage curves were obtained for the vertical npn and pnp transistors of 80 and 30 $h_{FE}$, respectively. Maximum operating temperature of CMOS/npn analog circuits simply increases as the silicon layer thickness decreases, and 200 °C operation is possible for 2 μm SOI.

## Acknowledgments

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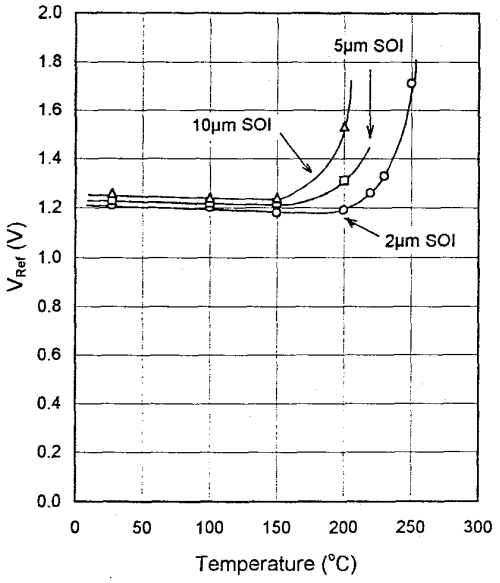


Fig. 7: Output voltages of the band gap reference circuit on SOI as a function of the temperature with the silicon layer thickness as a parameter.

## References

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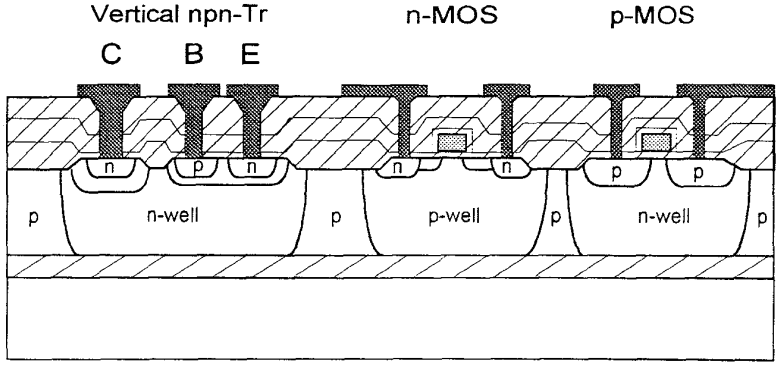


Fig. 8: Cross-sectional view of the analog circuits. CMOS and bipolar transistors were not isolated by trenches but isolated by pn junction.