Prospects of high voltage power ICs on thin SOI (Invited paper)

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Abstract

Silicon on Insulator technology is promising for high voltage power IC applications. The required SOI layer thickness can be reduced if a large portion of the applied voltage is sustained by the bottom insulator layer. Combination of SOI and trenches or LOCOS has merits of simplified device isolation and high device packing density. Thin SOI layer will realize high-speed switching in high voltage devices because of the smaller amount of stored carriers. Substrate bias influences on device characteristics and potentials of SOI technology are discussed.

1. Introduction

Silicon on Insulator technology has been of considerable interest for power IC applications since it was numerically predicted[1] that high breakdown voltage devices above 500V can be realized on relatively thin SOI of less than 20μm. A high device packing density and low cost dielectric isolation can be realized by a combination of trenches and SOI.

The basic concept is that the required silicon layer thickness can be reduced if a portion of the applied voltage is sustained by the bottom insulator layer. This approach has not been adopted because of the belief that the substrate bias will greatly influence the high voltage device characteristics.

There are three basic problems to overcome in order to realize high voltage power ICs on SOI:

1)How to realize high breakdown voltage devices on thin SOI.

2)How to minimize substrate bias effects on high voltage device characteristics.

3)How to realize large current high-speed devices on thin SOI.

This paper summarizes our recent research results and shows that all three problems can be overcome. It was experimentally verified that high voltage devices, exceeding 500V, can be realized on a 10μm thick SOI on 3μm thick bottom oxide.

The authors and another research team showed[2,3] that negative substrate bias can dynamically be shielded by inducing a p-channel on the bottom oxide if high voltage devices are formed on a relatively thick SOI layer. The substrate bias effects are less significant for lateral IGBTs on SOI[2]. It was further predicted[2] that even switching characteristics of IGBTs are not significantly influenced by the substrate bias. These results show that IGBTs can be used as source followers or high side switches.

Recently, it was reported[4] that switching speed of IGBTs on SOI is faster than that of conventional junction isolated IGBTs. This paper, for the first time, compares, in detail, the trade-off relations of IGBTs on SOI and conventional junction isolated lateral IGBTs.

2. Optimization of high voltage SOI device structure

The analysis on diode breakdown voltages on SOI was first done by H.C. Chen et al. in 1989[5]. Since they adopted a p^+/n^-/oxide/substrate diode structure and SIMOX substrate, they did not contemplate the idea of imposing a large part of applied voltage on the bottom oxide. The authors proposed an n^+/n^-/oxide/substrate structure for high voltage diodes in 1990[1]. It was found that positive interface charge density increases diode breakdown voltage. The authors further proposed[1,6] that $n^+/n^-/n^+$/oxide/substrate structure enhances diode breakdown voltage since the bottom oxide shares a larger part of the applied voltage.

The diode breakdown voltage takes its maximum when the total donor impurity dose of the SOI layer is around $1.2x10^{12}$, following the Resurf principle.

Figure 1 shows calculated n^+/n^-/oxide/substrate diode breakdown voltage as a function of n^- layer thickness with bottom oxide thickness as a parameter, assuming an abrupt n^+/n^- junction. A similar calculation, first performed by S. Merchant et al.[7] in 1991, showed the possibility of a very high breakdown voltage diodes, theoretically and experimentally, if SOI thickness is less than a few 100nm.

Figure 2 shows the breakdown voltage dependence on n^- layer thickness with positive interface charge density as a parameter. Figure 3 shows similar results, using a shallow n diffusion layer on the bottom oxide instead of positive interface charges. Figure 4 shows an optimized high voltage IGBT structure on SOI, based on the above analyses. Figures 1 to 3 show the 1 dimensional breakdown voltage along the symmetry axis A-A' in Fig.4. The 1-d breakdown voltage can be realized by optimizing lateral diode structures.

2. Static I-V characteristics of IGBTs and MOSFETs on SOI and substrate bias effects

Figure 5 shows calculated hole distribution for an

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IGBT of Fig.4 when a -100V negative substrate bias is applied against both the source and the drain. It is seen that substrate bias is shielded by the induced bottom p-channel and that most of the SOI layer remains undepleted. This means that the on-resistance of relatively thick SOI MOSFETs or IGBTs is not greatly affected by the substrate bias and ,thus, can be used as high side switches or source followers.

Figure 6 shows calculated on-resistance change as a function of SOI layer thickness associated with negative substrate bias with total impurity dose as a parameter. R_{on} and R_0 are defined in the figure. The calculations were carried out, assuming uniform impurity concentration in the SOI layer, with total impurity dose kept constant. The on-resistance of a 500V MOSFET on a very thin SOI such as 100nm depends greatly on the substrate bias as seen in Fig.6. This is because the thickness of the SOI layer is comparable to that of inversion layer(p-channel).

Thyristor like devices, such as IGBTs, are relatively free from substrate bias effects due to a large amount of carrier plasma, and exhibit almost the same current-voltage curves regardless of the substrate bias level. Figure 7 shows the calculated drain current change as a function of negative substrate bias. It was shown that the calculated on-resistance was scarcely affected by negative substrate bias. The stored carrier plasma easily shields the substrate bias and a hole accumulation layer is formed on the bottom oxide. It is understood that the substrate bias scarcely affects the current voltage curve of IGBTs since only a small portion of the total current flows in the bottom accumulation layer.

3. Electrical characteristics of IGBTs on SOI

It was experimentally shown that IGBTs on SOI operate at high switching speed. However, it was found that the trade-off relations for SOI IGBTs are no better than those for optimized junction isolated lateral IGBTs.

Figure 8 shows our experimental results on the trade-off relation between the drain current for 3V forward voltage vs. fall-time. Fabricated device structures were exactly the same except for the devices labeled A. SOI wafers were fabricated using boron doped 200Ωcm resistivity wafers. Each of these wafer were directly bonded to another substrate wafer after 2μm thick oxide films were grown. SOI layer thickness was adjusted by the conventional lapping technique. 8μm n diffusion layers were formed on all the SOI and 200Ωcm p^- bulk wafers. Thus, the differences among the SOI wafers are the thickness of the remaining p^- layer between the n diffusion layer and the bottom oxide.

The broken line E in the figure 5 shows the change in the fall-time with the decrease in the SOI layer thickness, namely from JI to 1 1μm thick SOI. Although the fall-time actually decreases, the device characteristics are not improved from the viewpoint of trade-off relation. However, significant improvement in the trade-off relations in IGBTs on SOI were still realized by optimizing drain structures as indicated by solid lines B,C, and D in Fig.5. The typical new drain structure is shown in Fig.9.

The influences of further reduction in the SOI layer thickness was investigated by a device simulator TONADDE II . Calculations were carried out assuming uniformly doped n type SOI layer with keeping total impurity dose as a constant value of $1x10^{12}$. The results are shown in Fig.10.

Switching speed enhancement is predicted for IGBTs on very thin SOI such as 2μm. Surface recombination cannot be neglected for IGBTs on very thin SOI. Figure 11 shows calculated forward voltage dependence on surface recombination velocity S with SOI layer thickness as a parameter. 1 or 2μm SOI is still quite attractive because of high-speed switching and easy device isolation, although their characteristics are significantly influenced by surface recombination velocity.

4.Conclusion

Fundamental problems associated with high voltage SOI power ICs have been overcome. The combination of CMOS logic, trench(or LOCOS) isolation and high voltage SOI output devices is promising for high voltage power ICs. Application of SOI technology to high voltage power ICs is now realistic.

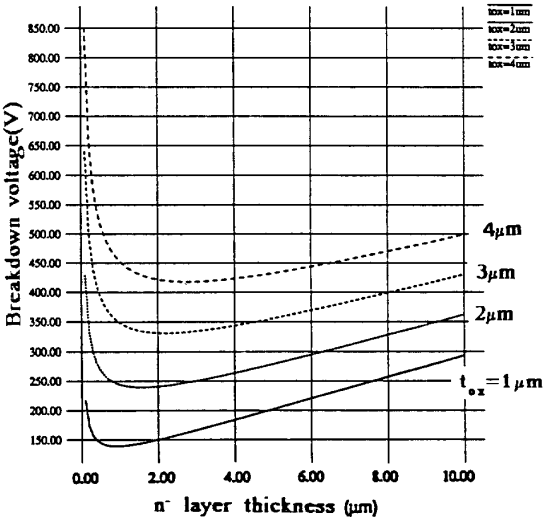

Fig.1 Calculated 1-d n^+/n^-/oxide/substrate diode breakdown voltage as a function of n^- layer thickness with bottom oxide thickness tox as a parameter

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[2]T.Matsudai et al, Proc. of 1992 ISPSD, p.272.
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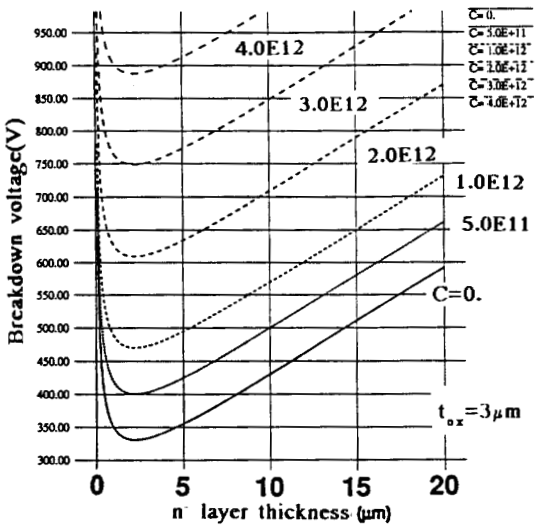
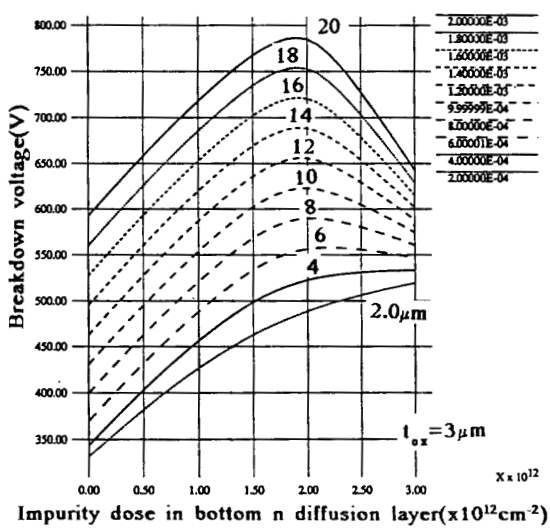


Fig.2 Calculated 1-d n^+/n^-/oxide/substrate diode breakdown voltage as a function of SOI layer thickness with interface charge density C as a parameter



Impurity dose in bottom n diffusion layer($x10^{12}cm^{-2}$)

Fig.3 Calculated $n^+/n^-/n$/oxide/substrate diode breakdown voltage as a function of n diffusion layer impurity dose with n^- layer thickness as a parameter

Gaussian impurity profile($2\sqrt{Dt}$= 1μm) is assumed for bottom n diffusion.

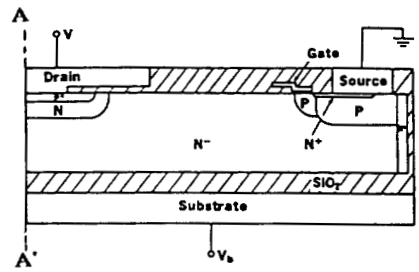


Fig.4 Optimized IGBT structure. Fig.1 to 3 shows the breakdown voltage along the symmetry axis A-A'.

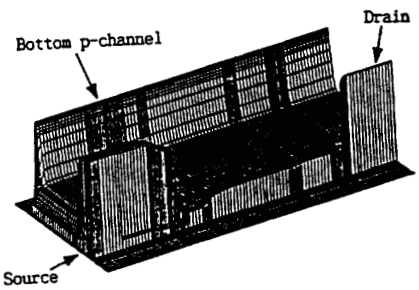


Fig.5 Calculated hole density distribution for IGBT of Fig.4

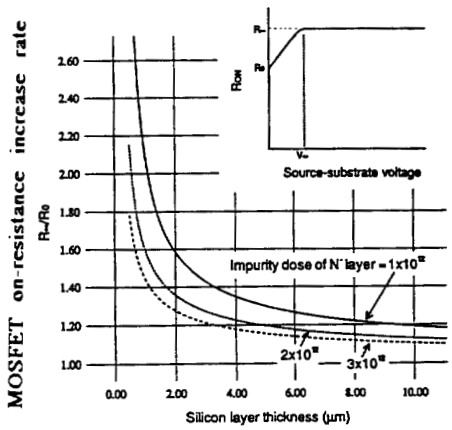


Fig.6 Calculated on-resistance increase rate associated with negative sub. bias as a function of SOI layer thickness with total impurity dose in SOI layer as a parameter.

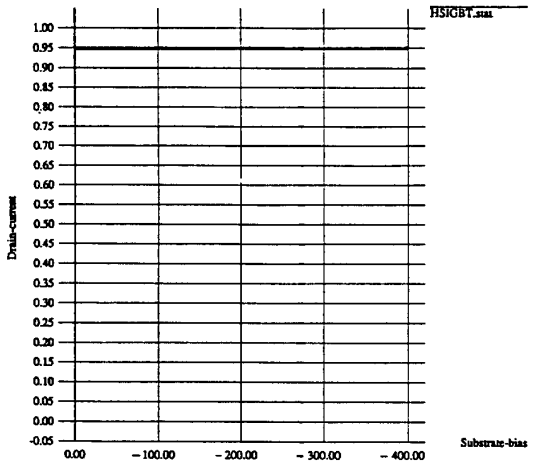


Fig.7 Calculated drain current for 2.8V forward voltage does not change with substrate bias. (15μm SOI IGBT)

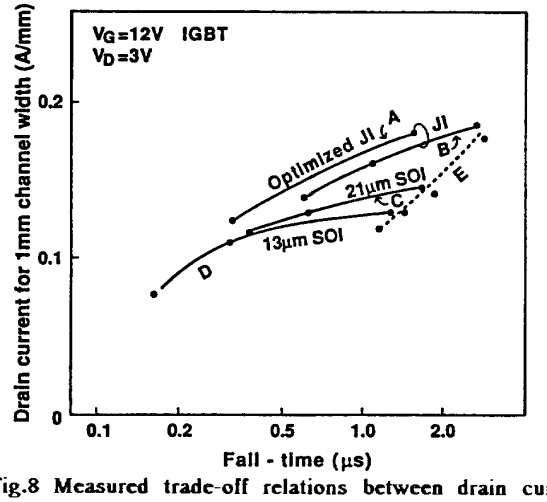


Fig.8 Measured trade-off relations between drain current for 1mm channel width(3V forward voltage) and fall-time.

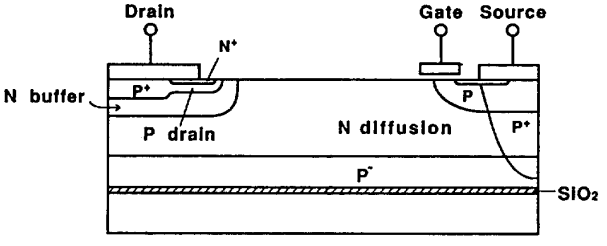


Fig.9 Typical high speed IGBT with new drain structure

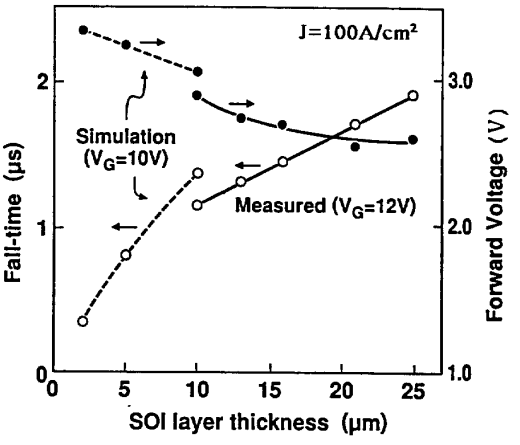


Fig.10 Calculated trade-off relations for less than 10μm SOI . Obtained experimental results for IGBTs on SOI thicker than 10μm are shown together.

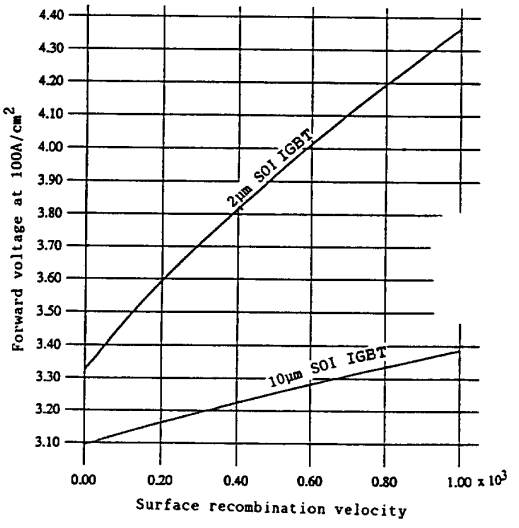


Fig.11 Predicted on-resistance dependence on surface recombination velocity for IGBTs on 2μm thick SOI .