SOI Device Structures Implementing 650 V High Voltage Output Devices on VLSIs

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ABSTRACT

It has been experimentally verified that 650 V breakdown voltage can be realized in lateral devices on a 14 μm thick SOI. The device structure is characterized by a shallow N type diffusion layer on a 3 μm thick bottom oxide film. Trenches will be available for device isolation by using a thin SOI film for a power IC. The combination of high voltage thin SOI device structures and the trench isolation technique will make VLSIs with high-voltage output devices possible.

INTRODUCTION

Dielectric isolation is an ideal technique for high voltage power ICs above 200 V. Conventional dielectric isolation methods (EPIC[1]) have been utilized for such high voltage power ICs. Recently, the thin silicon layer over silicon dioxide (SOI) technology has sufficiently advanced to motivate researchers to try to apply such SOI to high voltage power ICs. A thin SOI will achieve simplified device isolation and high density integration by being combined with trench technology.

One problem is how to attain a high breakdown voltage in a thin SOI. The authors numerically predicted[2] that a high breakdown voltage can be realized even in a thin SOI layer, if a large share of the applied voltage is sustained by a relatively thick bottom isolation oxide. The silicon wafer direct-bonding technique[3] is most promising for providing high quality silicon layers over a thick silicon dioxide film. Further breakdown voltage enhancement was also predicted to occur when an appropriate amount of positive charge is placed on the bottom oxide. A shallow N type diffusion layer on the bottom oxide will serve as such a positive charge layer.

This paper describes experimentally verified predicted results. High breakdown voltages have been achieved for devices fabricated on SOI layers which were sufficiently thin for trench isolation.

DEVICE STRUCTURES

Two types of diodes (A and B) were fabricated and evaluated. Their structures are illustrated in Fig.1. SOI wafers were prepared by the silicon wafer direct-bonding (SDB) method. Individual diodes were isolated by deep trenches. A SIPOS film was used as a resistive field plate between the anode and the cathode. The silicon layer thickness, t_S, for each device was directly measured by observing its cross section after breakdown voltage measurement.

The characteristic features of the diodes are their shallow N type diffusion layer on the bottom thick oxide, which was formed by arsenic ion implantation before directly bonding the wafer to another.

The difference between the two structures A and B is the conduction type of the trench side-wall diffusions. Structure B is superior from the viewpoint of actual BiCMOS IC application (see Fig.2), if the same breakdown voltage as that for structure A is guaranteed. This is because an N type side-wall diffusion can readily be utilized as a collector region in an NPN bipolar transistor on the same chip.

The most natural diode structure for power ICs with N type side-wall diffusion is structure C in Fig.1. However, the breakdown voltage for structure C was predicted to be lower than that for structure A[3], because the electric field is too strong at the foot of the side-wall diffusion layer when a high voltage is applied between the cathode and the grounded substrate.

EXPERIMENTAL RESULTS

Figure 3 shows the measured breakdown voltage as a function of the silicon layer thickness t_S with the impurity dose of the shallow diffusion layer S as a parameter. Structure B had the same high breakdown voltage as that for structure A. The numerically predicted breakdown voltage values are shown together in the same figure. The experimentally measured breakdown voltages were always greater than

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the calculated values.

A linear relationship between the breakdown voltage and the bottom oxide thickness was observed, as shown in Fig.4. The breakdown voltage increased by about 80 V with every 1 μm increase in t_{ox}. A breakdown voltage of 610 V was achieved on a 20 μm thick silicon layer with a 3 μm thick bottom oxide.

A 100 V breakdown voltage enhancement was realized with the adoption of a bottom N-layer. A breakdown voltage of 650 V was achieved in a diode on a 14 μm thick SOI layer on a 3 μm bottom oxide with a bottom N-layer of 1.3×10^{12} cm^{-2} arsenic ion dose, as shown in Fig.5. A too large N-layer impurity dose, S, deteriorated the breakdown voltages.

DISCUSSION

Although structure B involved a low breakdown voltage p-n junction between the anode p region and the n side-wall diffusion, it was found that structure B had the same high blocking capability as structure A. The reason for this is explained as follows. The potential of the side-wall n layer initially follows the cathode potential as the reverse bias becomes larger. However, the depletion region around the anode p region finally merges with the other depletion layer, which appears on the bottom oxide, as seen in Fig.6. This depletion region isolates the n side-wall diffusion from the cathode layer and prevents the potential rise of the side-wall. Accordingly, junction breakdown does not occur in the low breakdown-voltage junction even when the reverse bias becomes large. In order to keep a high breakdown voltage for structure B, its N silicon layer impurity concentration needs to be controlled depending on the vertical distance between the anode p region and the bottom oxide. Structure B is superior from the viewpoint of actual BiCMOS IC application, since structure B has the same high breakdown voltage as structure A.

The breakdown voltage enhancement by the bottom N-layer is explained using Fig.7, which shows the electric field distribution along a symmetry axis through the center of the cathode layer when the reverse bias is 500 V. Breakdown is generally caused by a strong, vertical electric field under the cathode for thin silicon layer devices. A thin positive charge layer on the interface, created by complete depletion of the bottom N-layer, effectively reduces the electric field inside the silicon layer. Accordingly, the electric field within the oxide film is increased, and a larger share of the applied voltage is sustained by the oxide, as seen in Fig.7. The electric field falls rapidly in the N type bottom diffusion layer. If the diffusion layer is thin enough, the high electric field region in the silicon layer is localized at a very narrow portion on the silicon oxide interface, and it contributes little to the avalanche multiplication (or ionization integral). Thus, the device can withstand a higher voltage. However, an excessive dose S, which causes too strong an electric field or prevents complete depletion in the bottom N-layer, results in a low breakdown voltage.

Breakdown voltage increases linearly with an increase in the bottom oxide thickness. This is explained by the uniform electric field inside the oxide.

APPLICATION TO OUTPUT DEVICES

The adopted structures can be easily modified to implement high voltage n- and p-channel lateral MOSFETs (or IGBTs). Examples are shown in Fig.8. An n-channel MOSFET has a different structure from that of a p-channel MOSFET lacking a surface p region, which is expected to serve as a double RESURF for the proposed diode structures. However, the SIPOS resistive field plate will keep the same high breakdown voltage as that of the p-channel MOSFET. For this case, the whole N drift layer can be regarded as a RESURF layer and an appropriate impurity concentration is required for high voltage.

CONCLUSION

A high breakdown voltage of 650 V has been achieved on a thin silicon layer by means of a thick bottom oxide and a bottom n-layer with an appropriate amount of impurity dose. The adopted device structures can be readily transformed to output devices, such as power MOSFETs or IGBTs. These SOI device structures combined with the deep trench technique are promising candidates for future VLSIs with high voltage power functions.

ACKNOWLEDGMENT

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[2]A.Nakagawa et al., IEEE Trans. Electron Devices, vol.ED-38, p.1650, 1991
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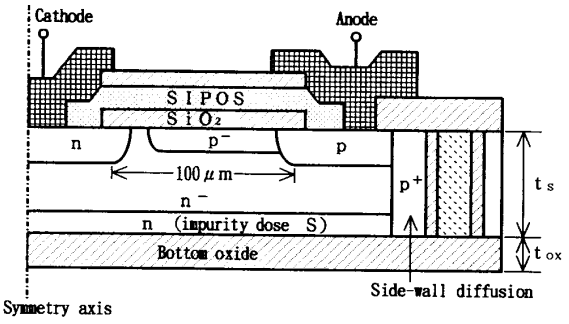
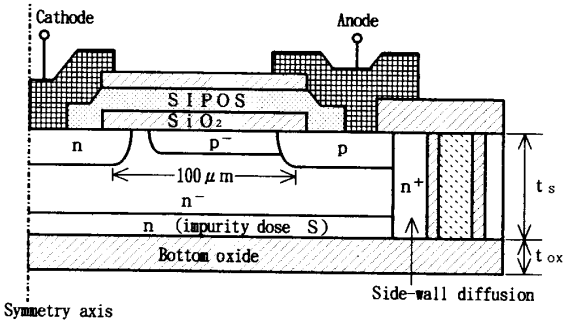
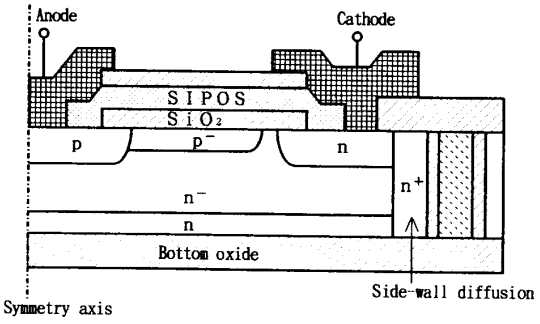


Structure A



Structure B



Structure C

Fig.1 Cross-sectional views for high voltage SOI devices. The difference between the two structures A and B is the conduction type of the side-wall diffusions. Arsenic implantation for the bottom n-layer was carried out before wafer direct-bonding.

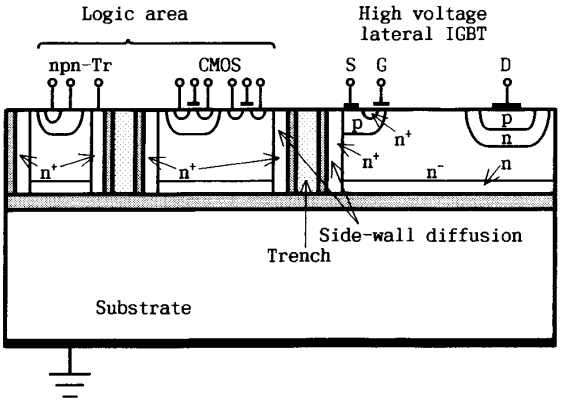


Fig.2 Trench isolated power IC. n^+ side-wall diffusion does not decrease the breakdown voltage for the high voltage lateral IGBT, as seen in Fig.3.

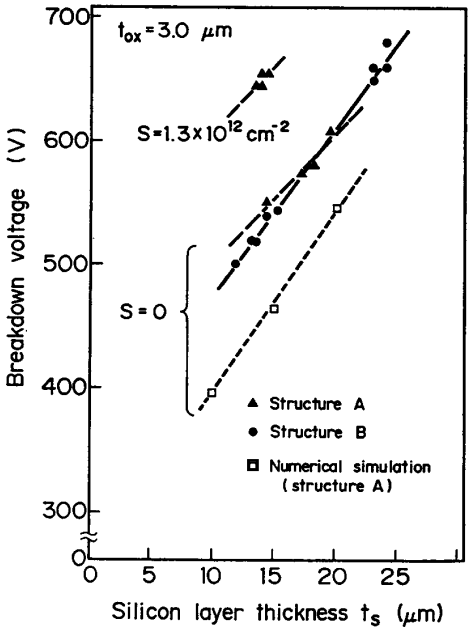


Fig.3 Breakdown voltage vs. silicon layer thickness for SOI structure. S denotes the ion dose for the bottom n-layer. t_{OX} denotes the bottom oxide thickness.

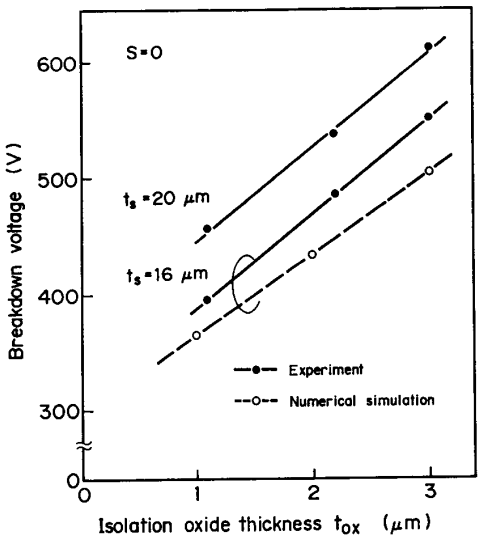


Fig.4 Breakdown voltage vs. isolation oxide thickness

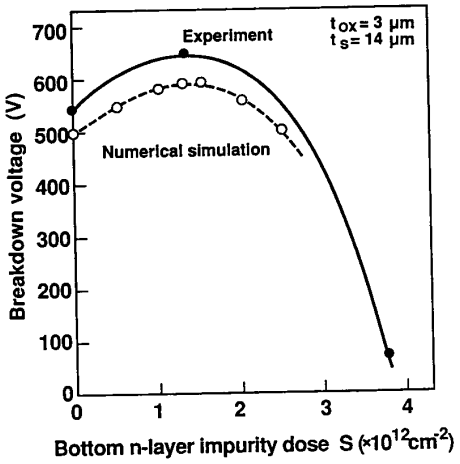


Fig.5 Breakdown voltage vs. bottom n-layer impurity dose

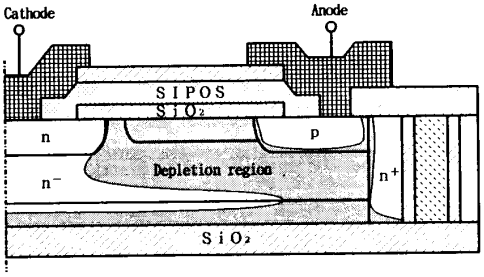


Fig.6 Depletion region in Structure B

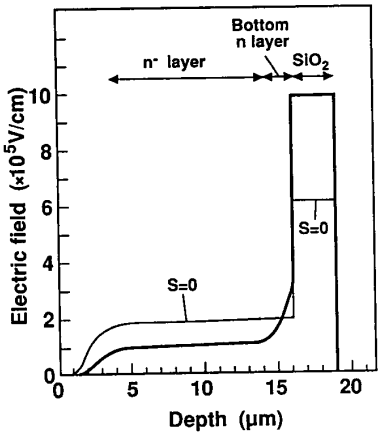
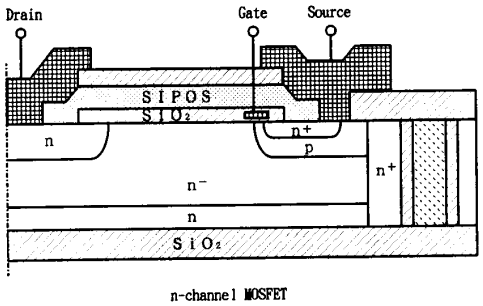
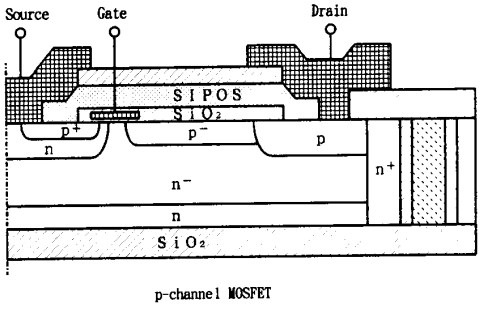


Fig.7 Electric field distribution along symmetry axis



n-channel MOSFET



p-channel MOSFET

Fig.8 High voltage n- and p-channel MOSFETs