Two Types of 500V Double Gate Lateral N-ch Bipolar-Mode MOSFETs in Dielectrically Isolated P^- and N^- Silicon Islands

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ABSTRACT

Two types of 500V double gate lateral N-ch Bipolar-Mode MOSFETs(DGLIGBT), fabricated on dielectrically isolated P^- and N^- silicon islands, were compared. It was found that electrical characteristics for devices on P^- silicon islands are superior to those for counterpart devices on N^- silicon islands. It was also shown that double gate operation improves device trade-off relation, realizing 200ns fall-time and 0.075Ωcm² Ron area product. The developed devices were passivated by SIPOS resistive field plates, which allows series connection by interconnection metal layers without breakdown voltage reduction.

1. INTRODUCTION

Bipolar-Mode MOSFETs[1](IGBTs[2,3]) have been recognized as excellent high voltage power devices because of MOS gate controlled large current capability, simultaneously with a high switching speed. It was experimentally[4] and theoretically[5] shown that the safe operating areas exceed the bipolar transistor theoretical limit. Large current devices such as 400A,500V and 300A,1000V[6] are now available on the market. Lateral devices are also attractive as high voltage output devices for power ICs.[7,8]

This paper compares electrical characteristics for the two types of N-ch Bipolar-Mode MOSFETs fabricated on P^- and N^- silicon islands, which were dielectrically isolated by silicon wafer direct-bonding(DISDB) and V-grooves[9,10]. An approximately 0.9mm² silicon island was completely isolated by 1μm thick oxide film.

Double gate devices[11] were fabricated and demonstrated, for the first time. It was numerically predicted[5,12] that double gate operation would improve device trade-off relation and even make 2500V IGBTs[5] realistic. The n-channel, created beneath the second gate, serves as a so called 'anode short' and inactivates the parasitic PNP transistor.

The SIPOS resistive field plate, combined with a metal field plate, was adopted for junction termination to shield overlying metal interconnection layer influence on the breakdown voltage[10,13].

The developed DG devices can all be formed by diffusions on dielectrically isolated silicon islands, thus, easily being implemented in power ICs and having complete process compatibility with CMOS logics and good noise imunity.

2. DIELECTRIC ISOLATION BY SILICON WAFER DIRECT-BONDING(DISDB) AND DEVICE FABRICATION

Silicon Wafer Direct-Bonding(SDB) technique was tested and applied to actual devices independently by two groups in 1985[14] and 1986[15,16,17]. This section describes an application of dielectric isolation technique based on SDB(DISDB) to a output power device.

Figure 1 briefly shows the fabrication process sequence for the DISDB. Details are seen in the reference[10].

Approximately 0.9mm² silicon islands were dielectrically isolated by this method. More than 800V isolation voltage between a silicon island and the substrate was obtained.

Double gate lateral Bipolar-Mode MOSFETs(0.43mm² active region) were fabricated only by diffusions on the silicon islands. Regarding lateral devices, the double gate structure is easily implemented in actual devices. Figures 2 and 3 show two basic N channel lateral device structures. The difference is which conductivity type is chosen for the starting silicon island.

Figure 4 shows a top view of the fabricated device on P^- silicon island. Basic designs for the diffusion depths and impurity profiles for the base and source layers are the same as those for the vertical devices. The three layers: the drain N^+-layer, drain P^+-layer and the N buffer were formed in a self-aligning manner by using the second gate polysilicon edge in order to easily control the threshould voltage for the second gate.

3. ELECTRICAL CHARACTERISTICS

This section reports electrical characteristics for the DGLIGBTs fabricated on dielectrically isolated silicon islands.

In a double gate device, the first gate is used for an ordinary current control means, whereas the second gate is for controlling the mode of the device operation by creating the N channel, which shunts the N-buffer and the N^+-layer in the P^+-drain layer.

Forward current voltage characteristics for a double gate device on an N^- silicon island(DG/N) continuously changed from those for the bipolar-mode (15ohm on-resistance, 0.43mm² active region) to those for the MOSFET-mode (115ohm on-resistance) as the second gate voltage changes from zero to 15V as shown in Fig.5.

However, the on-resistance change for a double gate device on a P^- silicon island(DG/P) by the second gate was 80% of that for a device on N^-

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silicon islands.

The strategy for a high speed switching using the two gates is as follows.

1) Apply a positive bias to the second gate against the drain to realize 'anode short'.
2) 0.5 or 1 μs later, first gate voltage is reduced to zero.

Figure 6 shows turn-off waveforms for a double gate device on N⁻ silicon island(DG/N). The fall-time can be reduced from 2μs to 0.8μs by operating the second gate.

Regarding double gate devices on P⁻ silicon island(DG/P), fall-time was much shorter than that for DG/N devices: namely, 0.2μs for DG operation and even 0.3μs without second gate operation (see Fig.7).

Figure 8 shows a typical turn-off waveform for a single gate device on a P⁻ silicon island(device E). Generally speaking, devices on P⁻ silicon islands have smaller tail currents and longer storage times, compared with devices on N⁻ silicon islands. This fact will be interpreted later.

Figure 9 shows a typical trade-off relation between current density for 3V forward voltage and fall time for 200mA drain current. Devices labeled B and C have identical source and drain diffusion profiles. Devices A and E have higher impurity concentration N-buffer layers than devices B and D, respectively. In the figure, it is manifest that DG/P devices are superior to DG/N devices. Even single gate devices on P⁻ silicon islands(SG/P) are comparable to DG/N devices.

Switching speed for devices on N⁻ silicon islands can be improved by electron irradiation or a high impurity concentration N buffer as seen in Fig.9. However, this method was not so effective for devices on P⁻ silicon islands. Especially for DG/P devices, electron irradiation simply deteriorated the device on-resistances without significant improvement in the switching speed.

Thus, devices on P⁻ silicon islands are suitable for high voltage power ICs, because they need no lifetime control.

DG devices can also be operated in the reverse direction. This operation mode might be utilized for inherent reverse conducting diodes.

The developed DG devices can all be formed by diffusions, thus,they are easily implemented in power ICs and have complete process compatibility with CMOS logics.

4.DEVICE SIMULATION FOR LATERAL Bipolar Mode MOSFET TURN-OFF PROCESS.

This section proposes a new double gate device structure. Inductive switching characteristics for a device shown in Fig.10 were simulated by a device simulator TONADDEII. The results not only clarified why the devices on P⁻ silicon island are superior to their counterpart devices but also show its possibility for a large current high speed switching lateral device.

Figure 11 shows calculated current voltage characteristics. It was determined from the calculated current voltage curves that the on-resistance for the proposed device is reduced to a half of that for the device shown in Fig.2.

Figure 12 shows inductive turn-off waveforms. The second gate was turned-on 1.5μs before turning-off the first gate. The caiculated fall-time is extremely short: 20ns., showing that the lateral double gate device has a potential for use in high speed switching.

Figure 13 and 14 show hole density distributio for time steps t=0 and 1.59μs, respectively. By comparing the two figures, it is seen that the developed depletion layers beneath the N⁻resurf layer(off-set channel) and under the second gate automatically sweep away most of the stored excess carriers. The important point is that, for the device on a P⁻ silicon island, the depletion layer develops where the largest carrier density exists in the device. Thus, stored carriers are swept away in the storage time period, resulting in a small tail current. For a more detailed explanation on he simulated results, please refer to [12].

5.CONCLUSION

Double gate lateral Bipolar-Mode MOSFETs were successfully realized on dielectrically isolated silicon islands by DISDB, improving the trade-off relation. 500V breakdown voltage could be obtained by SIPOS RFP technique. It was found that N-ch. devices on P⁻ silicon island are superior to counterpart devices on N⁻ silicon islands.

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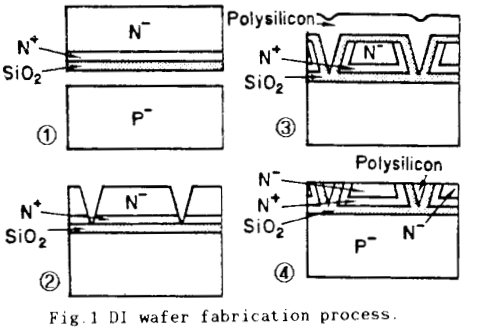


Fig.1 DI wafer fabrication process.

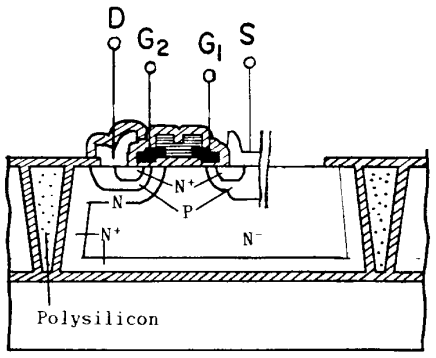


Fig.2 Double gate N ch. device on N^- silicon island.

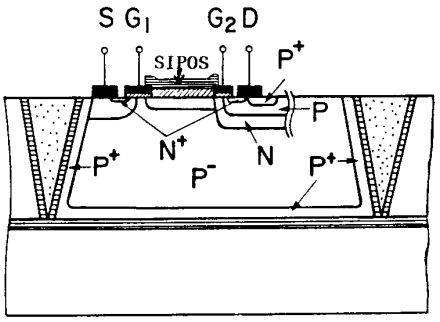


Fig.3 Double gate N ch. device on P^- silicon island.

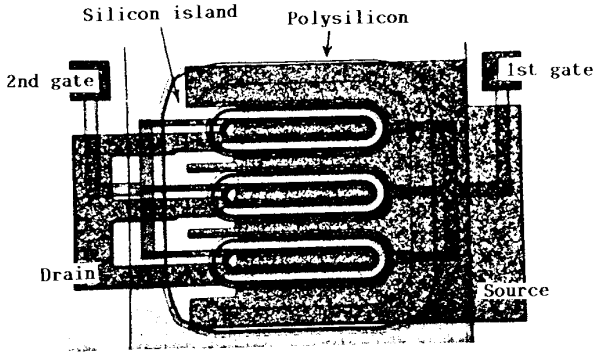


Fig.4 Top view of the fabricated DG device on P^- silicon iland.

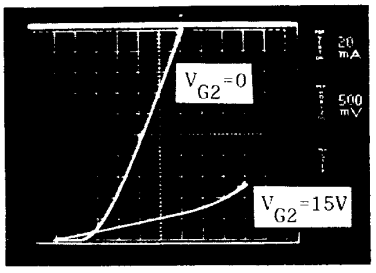


Fig.5

Current voltage characteristics(DG/N devices) for bipolar-mode operation(V_{G1}=15V,V_{G2}=0V) and MOSFET operation (V_{G1}=15V,V_{G2}=15V).

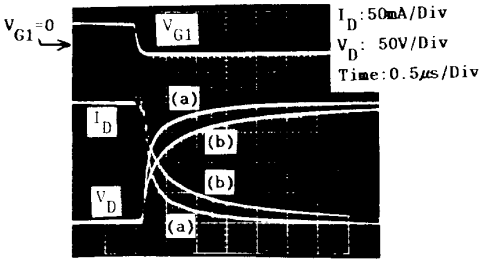


Fig.6

Turn-off waveforms for a DG device on N^- silicon island. (a)15V second gate voltage is applied 1μs before turning-off the first gate. (b)Second gate voltage is kept zero.

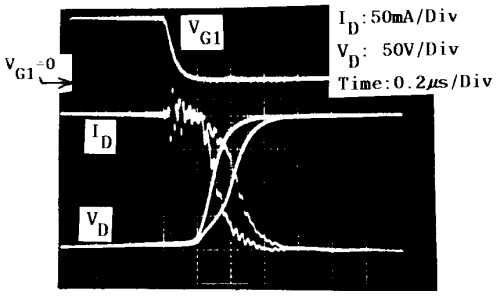


Fig.7 Two turn-off waveforms for a DG device on P^- silicon island with and without 2nd gate operation.

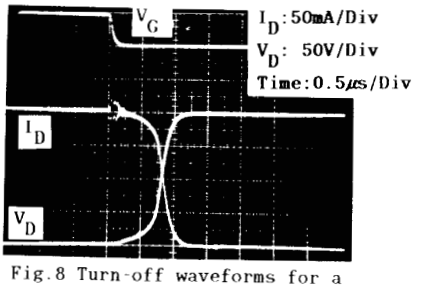


Fig.8 Turn-off waveforms for a single gate device on P⁻ silicon island(SG/P).

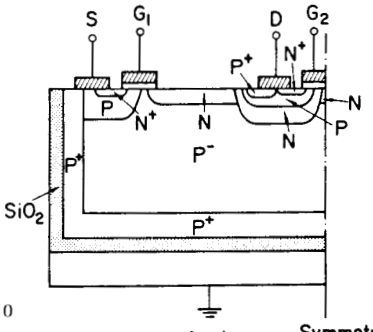


Fig.10

Proposed double gate device for better trade-off relation. Configuration for D and G_2 is different from that for Fig.3.

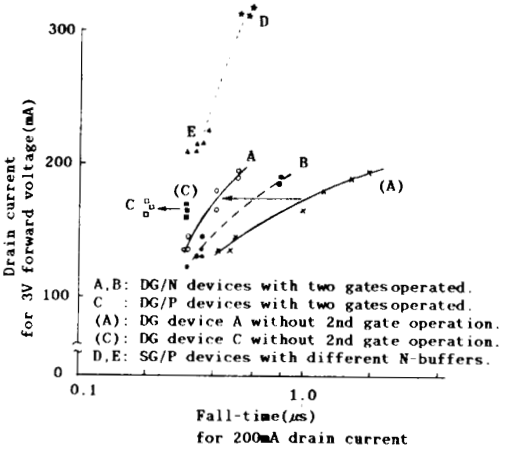


Fig.9 Modified trade-off relation between drain current for 3V forward voltage and fall-time for 200mA drain current. Curves A and B shows the changes with electron irradiation.

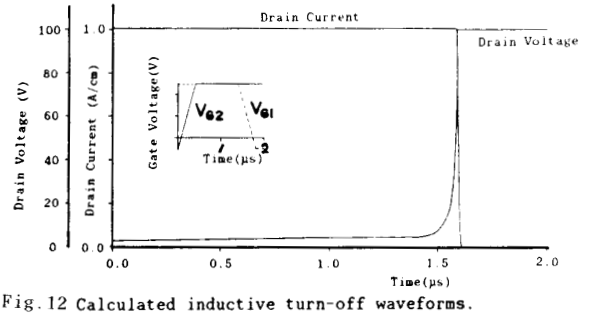


Fig.12 Calculated inductive turn-off waveforms. The second gate is turned-on, 1.5μs before turning-off the first gate.

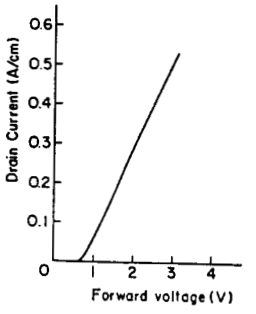
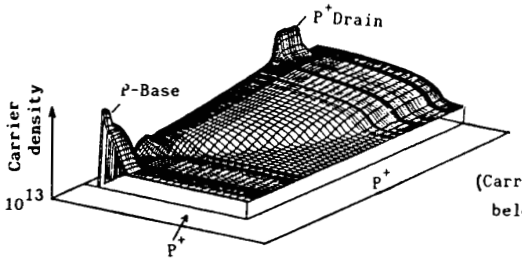


Fig.11 Calculated current voltage curve for the DG device shown in Fig.10.



(Carrier density below 10^{13} is not shown.)

Fig.13 Hole density plot for t=0.

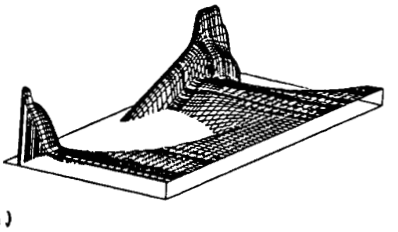


Fig.14 Hole density plot for t=1.59μs. (V_D=100V)